Session 26 Overview:
RF Techniques for Communication and Sensing
RF SUBCOMMITTEE

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Huawei, Mougins, France

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Georgia Institute of Technology, Atlanta, GA

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The increasing need to improve transmitter efficiency, enhance receiver linearity and robustness, and migrate electronic interfaces closer to the antenna continues to stimulate research in advanced RF techniques. The first paper in this session presents a broadband hybrid-coupler circulator for full-duplex operation. The following two papers demonstrate mm-wave antenna and power amplifier co-integration to increase efficiency and reduce cost. Next, we have three papers that advance power-amplifier architectures for 5G and NB-IoT applications. The three papers towards the end of this session demonstrate techniques for high-linearity receivers. A real-time, near-field THz imager concludes the session.

1:30 PM

26.1 A 0.55-to-0.9GHz 2.7dB NF Full-Duplex Hybrid-Coupler Circulator with 56MHz 40dB TX SI Suppression

S. Jain, Oregon State University, Corvallis, OR

In Paper 26.1, Oregon State University presents a balanced hybrid circulator RX that achieves 2.7dB NF, while providing >40dB TX-to-RX baseband isolation across 32MHz BW (56MHz BW for an average of 40dB isolation), and >30dB isolation across 190MHz bandwidth. An on-chip balancing network is not required. The improvement in NF in this work is >3dB, and the isolation bandwidth is increased >2.7× compared to state-of-the-art circulator-based RX.

2:00 PM

26.2 A 62-to-68GHz Linear 6Gb/s 64QAM CMOS Doherty Radiator with 27.5%/20.1% PAE at Peak/6dB-Back-off Output Power Leveraging High-Efficiency Multi-Feed Antenna-Based Active Load Modulation

H. T. Nguyen, Georgia Institute of Technology, Atlanta, GA

In Paper 26.2, Georgia Institute of Technology leverages a high-efficiency multi-feed antenna-based active-load-modulation scheme. The paper reports a multi-feed 65GHz on-chip Doherty radiator in 45nm SOI-CMOS that supports Gb/s modulations and generates 19dBm P_{1dB} with 27.5%/20.1% PAE at 0dB/6dB back-off. The best back-off efficiency enhancement among 60-to-80GHz silicon-based PAs is demonstrated using a new output network.

2:30 PM

26.3 A 69-to-79GHz CMOS Multiport PA/Radiator with +35.7dBm CW EIRP and Integrated PLL

B. Abiri, California Institute of Technology, Pasadena, CA

In Paper 26.3, the California Institute of Technology demonstrates an on-chip multiport radiator and an integrated PLL with a locking range of 69-to-79GHz that is capable of providing a continuous 35.7dBm EIRP and 24.4dBm of total radiated power with 15.2% DC-to-radiation efficiency. The approach is also scalable and extracts high power levels from low-voltage CMOS transistors by combining power from multiple PAs and lowering the radiator driving impedance.

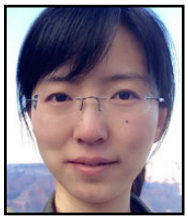
 978-1-5090-4940-0/18/$31.00

2:45 PM

26.4 A 28GHz 41%-PAE Linear CMOS Power Amplifier Using a Transformer-Based AM-PM Distortion-Correction Technique for 5G Phased Arrays

S. N. Ali, Washington State University, Pullman, WA

In Paper 26.4, Washington State University presents a transformer to correct the AM-PM distortion of a Class-AB PA for 5G applications. The 65nm CMOS PA achieves <0.7 degree AM-PM distortion, 41% PAE, and 15.6dBm P_{out} at 28GHz CW. Tested under a 512/256/64QAM signal with a 20/50/340MSym/s data-rate at 28GHz, the PA has a linear PAE at 28GHz of 18.2% for a 64QAM, 340MHz BW signal (P_{avg}=9.8dBm, EVM=-26.4dBc and ACPR=-30dBc).



3:15 PM

26.5 A Compact Dual-Band Digital Doherty Power Amplifier Using Parallel-Combining Transformer for Cellular NB-IoT Applications

Y. Yin, Fudan University, Shanghai, China

In Paper 26.5, Fudan University demonstrates a dual-band high-power digital Doherty PA for cellular NB IoT in 55nm CMOS. The PA reaches 28.9dBm$_{peak}$ P_{out} with 36.8% PAE in the low band and 27dBm$_{peak}$ P_{out} with 25.4% PAE in the high band. For a 12-subcarrier 180kHz NB-IoT signals, P_{out} is 24.4dBm with an average PAE of 29.5% and -21.6dB EVM.

3:30 PM

26.6 A Continuous-Mode Harmonically Tuned 19-to-29.5GHz Ultra-Linear PA Supporting 18Gb/s at 18.4% Modulation PAE and 43.5% Peak PAE

T-W. Li, Georgia Institute of Technology, Atlanta, GA

In Paper 26.6, Georgia Institute of Technology presents a PA that achieves a P_{sat} 1dB bandwidth of 19 to 29.5GHz (43.3%) or S_{21} 3dB BW of 17.7 to 32.3GHz (58.4%) for multiband 5G MIMO. It supports 18Gb/s 64QAM and 8Gb/s 256QAM with >8.7dBm P_{avg}, >16.3% total PAE, and >20% PA PAE under modulation. The design is based on a continuous-mode harmonically tuned linear mm-wave PA that features an ultra-compact on-chip PA output network in only one transformer footprint. The continuous-mode terminations at the fundamental, 2nd, and 3rd harmonics are wideband with no tunable elements or switches.

4:00 PM

26.7 A Coupled-RTWO-Based Subharmonic Receiver Front-End for 5G E-Band Backhaul Links in 28nm Bulk CMOS

M. Vigilante, KU Leuven, Heverlee, Belgium

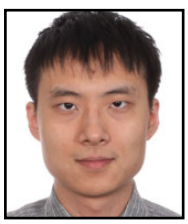
In Paper 26.7, KU Leuven demonstrates an E-Band direct-conversion subharmonic receiver (SHRX) that achieves 8.3dB noise figure, 12.5GHz RF bandwidth, and -25dBm ICP_{1dB}, while consuming <100mW. The receiver leverages on-chip coupled RTWOs to generate 8 differential phases at $f_{LO}=f_{RF}/4$. It is implemented in a 28nm bulk CMOS technology without an ultra-thick top metal.

4:15 PM

26.8 A 12mW 70-to-100GHz Mixer-First Receiver Front-End for mm-Wave Massive-MIMO Arrays in 28nm CMOS

L. Iotti, University of California, Berkeley, CA

In Paper 26.8, the University of California, Berkeley, presents an E-Band mixer-first RX with S_{11}<-10dB, 8-to-12.7dB NF, 19.5-to-25.3dB gain, and -16.8dBm maximum ICP_{1dB} across 70-to-100GHz. The high-input-impedance passive mixer is matched at the RF input using a frequency-translational feedback and a broadband matching network. Power consumption is 12mW.



4:30 PM

26.9 A 13th-Order CMOS Reconfigurable RF BPF with Adjustable Transmission Zeros for SAW-Less SDR Receivers

P. Song, University of Southern California, Los Angeles, CA

In Paper 26.9, the University of Southern California describes a 13th-order CMOS reconfigurable RF bandpass filter that is tunable from 0.8 to 1.1GHz. The IIP3-OOB is +24dBm at a 40MHz offset. The filter has adjustable close-by transmission zeros. The 3dB BW is 30 to 50MHz, tunable, and has a 100dB/100MHz transition-band roll-off that enables close-by blocker rejection.

4:45 PM

26.10 A 128-Pixel 0.56THz Sensing Array for Real-Time Near-Field Imaging in 0.13µm SiGe BiCMOS

P. Hillger, University of Wuppertal, Wuppertal, Germany

In Paper 26.10, the University of Wuppertal presents a silicon-based super-resolved real-time terahertz sensing system that includes THz illumination, detection, evanescent field sensing, and readout on a single chip. It comprises of 128 split-ring-resonator-based 0.56THz near-field sensors. Chopping techniques and an integrated lock-in amplifier are employed to achieve 93dB dynamic range (1Hz BW) in an analog readout mode, and 37dB at 28fps in a digital readout mode.

26.1 A 0.55-to-0.9GHz 2.7dB NF Full-Duplex Hybrid-Coupler Circulator with 56MHz 40dB TX SI Suppression

Sanket Jain, Abhishek Agrawal, Manoj Johnson, Arun Natarajan

Oregon State University, Corvallis, OR

Simultaneous transmit-and-receive (STAR) radios enable higher spectrum efficiency and dynamic spectrum access. The integration of a shared antenna interface is attractive for small system formfactor and MIMO channel estimation and has led to demonstrations of compact reciprocal (electrical balance duplexers (EBD)) and non-reciprocal (circulator) interfaces with self-interference cancellation (SIC) [1-5]. In this paper, we address the challenge of low-noise wideband SIC by demonstrating a wideband hybrid-coupler-circulator antenna interface using N-path mixers that achieves low NF while preserving the linearity of passive-mixer-first RX. The 0.55-to-0.9GHz hybrid-coupler-based circulator-RX achieves 2.7dB NF at 750MHz with +14dBm OOB IIP3 as part of an antenna interface that achieves 2.6-to-4.1dB TX→ANT insertion loss (IL) from 550 to 900MHz. The wideband coupler approach provides >40dB TX-to-RX baseband (BB) isolation across a 32MHz BW (56MHz BW for averaged 40dB isolation) and >30dB isolation across a 190MHz bandwidth without an on-chip balancing network, representing a >3dB improvement in NF and >2.7× increase in cancellation bandwidth compared to previously published circulator-RX.

Magnetic-free integrated circulators, based on the phase non-reciprocal behavior of two-port N-path filters embedded in a transmission-line (t-line) structure, have been demonstrated in [2,3]. The architecture has been extended to mm-wave using a wideband gyrator in [4]. However, intrinsic asymmetry in the t-line structure leads to amplitude and phase imbalance, which can limit both the TX SIC nulls as well as the TX SIC bandwidth. A balance network has been demonstrated to increase SIC, but the resulting increase in quadrature imbalance can lead to NF degradation [2]. The requirements placed on an additional balancing network can be considerably relaxed if the intrinsic quadrature balance in the passive structure is improved. Figure 26.1.1 shows the baseband voltage for a two-port N-path filter, driven by quadrature clocks, as a function of phase difference, θ, between the input signals. The N-path mixers constructively combine signals at the LO frequency with $\theta = -90°$ while rejecting all other signals (ignoring harmonics) and specifically nulling signals with $\theta = 90°$ at the LO frequency. The proposed balanced 90° hybrid-coupler-based non-reciprocal structure is shown in Fig. 26.1.1 in which the two-port N-path mixer driven by quadrature clocks is connected to the thru and coupled ports while the TX and ANT signals are applied to the input and isolation ports. Signals from the TX and ANT ports are in quadrature at the thru and coupled ports but with opposite phase progressions (Fig. 26.1.1). The phase non-reciprocal two-port N-path mixer nulls the TX signal creating a reflective short at the thru and coupled ports with respect to the TX signal. This leads to the TX signal propagating to the antenna port. On the other hand, signals from the ANT port see a high impedance at the thru and coupled ports leading to RX reception on the baseband capacitors. Notably, the impedance translation of N-path structures ensures a short for all signals from the TX port and for out-of-band signals at the RX port, thereby providing TX as well as OOB rejection. Achieving quadrature phase and amplitude balance is critical for wideband nulling. As shown in Fig. 26.1.1, 90° hybrid coupler can achieve wideband quadrature balance enabling wideband TX nulling. The TX-to-ANT IL depends upon hybrid-coupler IL and mixer-switch R_{SW}. Given compact commercial SMD couplers with 0.2dB IL [6] and CMOS switches with R_{SW} ~ 1.6Ω, the proposed approach can simultaneously achieve wide SIC bandwidth and low IL while ensuring small formfactor and simplified packaging.

Additionally, the potential for achieving low RX NF using an integrated circulator structure is presented in Fig. 26.1.2. Similar to the structure in [2], the two-port N-path circuit constructively combines the ANT signals arriving at the thru and coupled ports on the baseband capacitors. The down-converted RX signal is hence available on the N-path capacitors, which serves as the RX baseband port. This is equivalent to a circulator operating with the RX port mismatched to a high impedance. Therefore, power matching for the ANT port is provided by the TX port termination. If the TX port is terminated in 50Ω, a wideband RX match (limited by coupler bandwidth) is achieved. However, ANT→TX isolation is no longer present since the ANT port is matched by the TX port impedance. Importantly, noise emanating from the TX termination is cancelled at the RX port, similar to other wideband noise-cancelling LNAs. In addition, the hybrid-coupler structure results in a passive voltage gain at the RX port. Since the baseband RX can be designed without matching considerations, it is feasible to achieve low NF by reducing the input-referred noise of the baseband circuits while preserving the linearity of passive-mixer-first RX. Finally, quadrature balance in the hybrid-coupler enables TX SIC without the balancing network in [2], avoiding the associated degradation in RX gain and NF.

The schematic of the implemented hybrid-circulator receiver is shown in Fig. 26.1.2. The 65nm CMOS implementation includes 8-phase N-path switches and baseband inverter-based G_M-cells that drive off-chip TIA and summing amplifiers. Dual-edge-triggered flip flops are used to generate the 8-phase non-overlapping pulses for I and Q LO signals from a 4× LO. The switch drain and source voltages are biased to improve switch linearity and the clock drive is AC coupled to the mixer gates. The IC is implemented in 65nm CMOS and occupies 1mm^2. The IC is packaged with a commercial wideband 700MHz SMD hybrid coupler (5.1mm × 6.4mm) [6] using a chip-on-board packaging approach.

The measured S-parameters with respect to the TX (Port 1) and ANT (Port 2) ports is shown in Fig. 26.1.3. A wideband input-match from 300MHz to 1GHz is observed with IL of 2.6dB, 3.1dB, and 4.7dB at 550MHz, 700MHz, and 900MHz, respectively (LO at 770MHz). As expected, the high impedance at the RX port results in lack of isolation for ANT→TX. In this design, the N-path capacitors are sized for 80MHz RF BW. The expected phase asymmetry due to the non-reciprocal structure can be seen in Fig. 26.1.3. The RX conversion gain and linearity are measured with the G_M cells loaded with 50Ω. The measured NF (with G_M cells driving 50Ω to exclude the TIA impact) at 750MHz LO is shown in Fig. 26.1.3. The passive-mixer-first circulator-RX provides high-linearity of +14dBm with respect to out-of-band signals. The high-impedance baseband approach leads to the RX achieving 2.7dB NF (Fig. 26.1.3) and demonstrating the feasibility of achieving low NF with shared antenna interface functionality. The RX can achieve 0.2dB improved NF in TDD mode if switch drive settings are optimized for NF rather than TX→ANT IL.

TX SIC measurements are carried out for a LO of 770MHz with an impedance tuner providing <1.2 VSWR transformation on the ANT port that is fixed across frequency. The small-signal and large-signal TX→RX BB isolation (referred to the ANT port) are shown in Fig. 26.1.4. The ANT port VSWR and LO I/Q phase settings are optimized for +5.5dBm TX power. The symmetric hybrid-coupler approach results in wide SIC bandwidths for circulator-RX without the need for balancing networks that degrade RX NF or IL. Measurements show >20dB SIC across >400MHz BW and >30B SIC across 160MHz BW for small-signal and large-signal TX. In the case of +5.5dBm TX, SIC > 40dB is achieved for 32MHz BW while average SIC > 40dB is achieved across 56MHz BW.

The passive-mixer-first RX architecture, accompanied by a 40dB wideband SIC, supports high linearity with respect to the TX port while only placing the typical 50Ω matching constraint on the TX. The measured RX 1dB compression due to in-band TX signal is shown in Fig. 26.1.4 and demonstrates blocker P1dB of +5.5dBm. The TX→ RX BB SIC results in lower inter-mod products due to the TX. A two-tone TX input shows an effective small-signal IB-IIP3 of 4dBm referred to the ANT port (Fig. 26.1.4). Two-tone tests show TX→ANT IIP3 of 25dBm (Fig. 26.1.4), which is in-line with expectations due to the high isolation.

The impact of varying ANT VSWR on SIC is measured using a manual impedance tuner. SIC is a function of the magnitude and angle of the load reflection coefficient with >20dB cancellation for VSWR < 1.35. The efficacy of the proposed structure in rejecting modulated TX signals is also shown in Fig. 26.1.5. A modulated multi-tone signal with a null-to-null BW of ~20MHz is applied at the TX port. Figure 26.1.5 shows the normalized baseband signal at 3.5dBm and -11.5dBm input power. While the higher power level leads to increased inter-mod products, the measured signal power at baseband demonstrates >40dB RF SIC across high power levels for the wideband signal.

The measured performance of the proposed structure is compared to prior works in Fig. 26.1.6 while the die micrograph is shown in Fig. 26.1.7. The hybrid-circulator RX achieves significantly improved NF compared to prior antenna-interface RX while also providing wideband SIC and scalability to higher frequencies.

Acknowledgements:
This project was funded by the DARPA ACT program and NSF #1554720.

References:

[1] B. van Liempd et al. "A +70dBm IIP3 Single-Ended Electrical Balance Duplexer in 0.18μm SOI CMOS," *ISSCC*, pp. 32-33, Feb. 2016.
[2] N. Reiskarimian et al. "Highly-Linear Integrated Magnetic-Free Circulator-Receiver for Full-Duplex Wireless," *ISSCC*, pp. 316-318, Feb. 2017.
[3] J. Zhou et al. "RX with integrated magnetic-free N-path-filter-based non-reciprocal circulator and baseband SI cancellation for FD wireless," *ISSCC*, pp. 178-180, Feb. 2016.
[4] T. Dinc and H. Krishnaswamy "A 28GHz magnetic-free non-reciprocal passive CMOS circulator based on spatio-temporal conductance modulation", *ISSCC*, pp. 294-295, Feb. 2017.
[5] D. Yang et al. "A Wideband Highly Integrated and Widely Tunable Transceiver for In-Band Full-Duplex Communication," *IEEE JSSC*, vol. 50, no. 5, pp 1189-1202, May 2015.
[6] Anaren, "Hybrid Coupler 3 dB 90°," Model X3C07P1-03S Datasheet, Rev C. Accessed on July 24, 2017.
[7] T. Zhang et al. "A 1.7-to-2.2GHz Full-Duplex Transceiver System with >50dB Self-Interference Cancellation over 42MHz Bandwidth," *ISSCC*, pp. 314-316, Feb. 2017.
[8] D. Broek et al. "An In-Band FD Radio RX With a Passive Vector Modulator Downmixer for SI Cancellation," *IEEE JSSC*, Vol. 50, No. 12, Dec. 2015.

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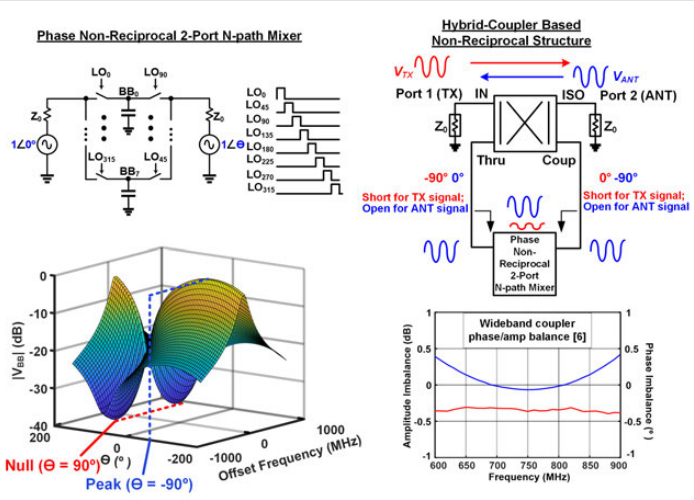

Figure 26.1.1: The 2-port N-path structure combines signals with θ = -90° while nulling signals with θ = 90°. Embedding this structure in a 90° hybrid coupler results in wideband TX signal nulling at mixer capacitors.

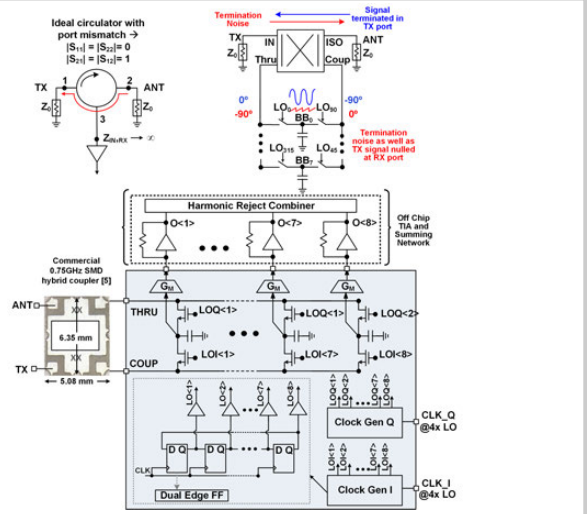

Figure 26.1.2: The 2-port N-path capacitors serve as the high-impedance RX port in circulator RX. Noise and signal from the TX port are nulled at the RX port. Schematic of the proposed hybrid-coupler circulator-RX.

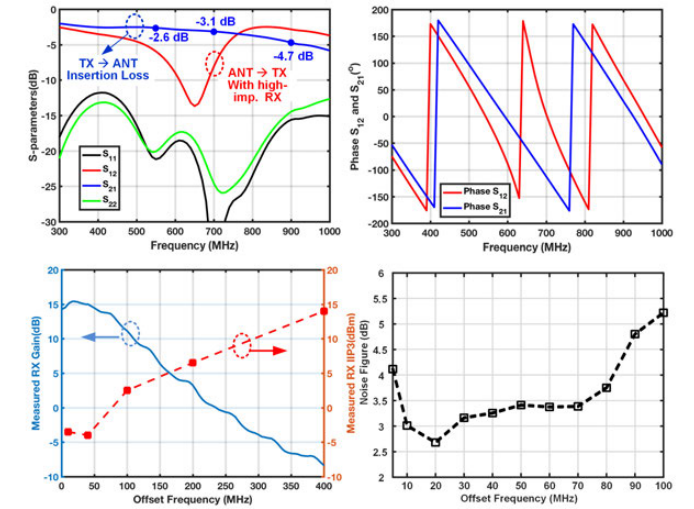

Figure 26.1.3: Measured S-parameters showing input power match and TX-to-ANT insertion loss. Measured in-band and out-of-band IIP3 and measured NF demonstrates passive-mixer-first type linearity with low NF.

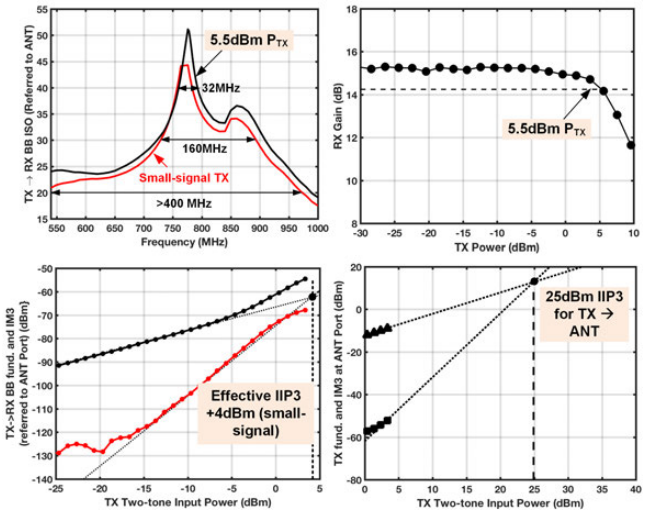

Figure 26.1.4: Measured TX-to-BB isolation (referred to the ANT port) shows wideband cancellation. Measured blocker-1dB tests show +5.5dBm TX power handling. Measured two-tone TX test shows +25dBm IIP3 for TX-to-ANT path.

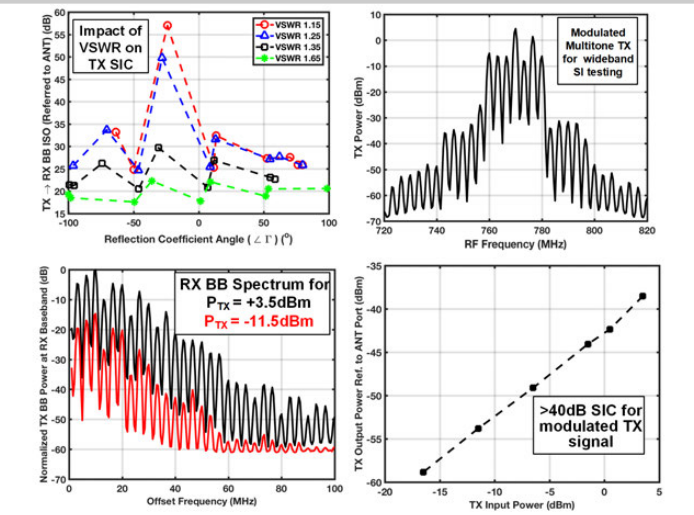

Figure 26.1.5: Measured cancellation across the ANT port VSWR. Wideband SI cancellation testing using a modulated multi-tone input shows approximately linear increase in SI power and >40dB TX-to-BB isolation (ref. to ANT).

Specification	This Work	ISSCC 2017 [2]	ISSCC 2017 [7]	ISSCC 2016 [3]	JSSC 2015 [5]	JSCC 2015 [8]
Arch.	Hybrid-Coupler based N-path Circulator RX	T-line based N-path Mixer Circulator RX	Dual Path Adaptive Filter	T-line based N-path Mixer Circulator RX	Mixer-First TRX with Baseband Duplexing	Mixer First SI-cancelling VM-down mixer
Frequency	0.55-0.9GHz	0.61-0.975GHz	1.7-2.2GHz	0.6-0.8GHz	0.1-1.5GHz	0.15-3.5GHz
Antenna Interface	Yes	Yes	No	Yes	Yes	No
RX Gain (dB)	15dB	28-43dB	20-35dB	42dB	53dB	24dB max.
RX NF	**2.7dB**	6.3dB	4dB	5-8.4dB	5-8dB	6.3dB
In-band IIP3	-4dBm @ 15dB gain	-18.4dBm at 28 dB gain	NR	-33dBm at 42dB gain	-38. 7dBm at 53dB gain	+9/+19dBm (-ve cond. on/off)
OOB IIP3	+14dBm	+15.4dBm	NR	+19dBm	+22.5dBm	+22dBm
Analog SIC Domain	RF	RF	RF + BB	RF + BB	BB	RF
RF/Analog SI suppression	**40dB ave. SIC across 56MHz BW; >40dB 32MHz BW >30dB 190MHz BW**	40dB SIC across 20MHz BW[a]	>30dB RF SIC over 40MHz; > 50dB SIC RF & BB: 42MHz	42dB SIC across 12MHz BW[a]	33dB across 300KHz TX BW	27dB SIC across 16.25 MHz
TX Port Power Handling	+5.5dBm	+7	NR	-7dBm	-17.3	N/A
TX → ANT IL	2.6dB @ 550MHz 3.1dB @ 700MHz 4.7dB @ 900MHz	1.8dB to 3.2dB	NA	1.7dB-3.2dB	NA	N/A
Effective IIP3 with respect to TX power	+4dBm small-signal	-10dBm small-signal	NR; canceller IIP3 26.5dBm[b]	+1dBm at 42dB gain	0dBm at 43/53dB gain	1.5dBm
RX + SI Canceller Power	25mW	72mW[d]	33.5mW	100mW[e]	43-56mW incl. TX	23-56mW
Antenna Interface Power	24mW	36mW[c] at 0.7GHz	N/A	59mW[c] at0.7GHz	RX power incl. interface	N/A
Technology	65-nm CMOS	65-nm CMOS	40-nm CMOS	65-nm CMOS	65-nm CMOS	65-nm CMOS

[a]additional digital SI cancellation also demonstrated; [b]linearity of canceller reported; IIP3 with respect to TX at BB not reported; [c]includes on-chip phase control, [d] includes two-stage baseband amplification; [e] includes BB canceller

Figure 26.1.6: Performance summary and comparison with the prior recent full-duplex/shared antenna-interface RXs.

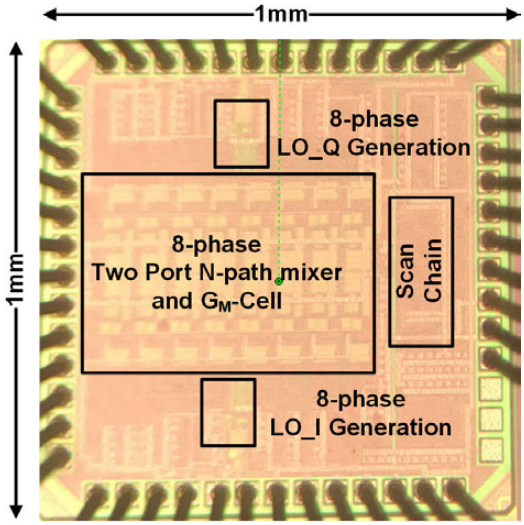

Figure 26.1.7: Die micrograph of the IC (occupying 1mm² in 65nm CMOS) packaged with a 90° hybrid coupler (not shown).

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26.2 A 62-to-68GHz Linear 6Gb/s 64QAM CMOS Doherty Radiator with 27.5%/20.1% PAE at Peak/6dB-Back-off Output Power Leveraging High-Efficiency Multi-Feed Antenna-Based Active Load Modulation

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Extreme throughput requirements on future mm-wave systems, e.g., 5G links, necessitates the use of spectrum-efficient modulations that often come with high peak-to-average power ratios (PAPRs). Therefore, there is an increasing need for mm-wave power amplifiers (PAs) with high power back-off (PBO) efficiency, so that wideband large-PAPR signals can be transmitted with high energy efficiency. Among various PA PBO efficiency-enhancement techniques, Doherty PAs feature wideband modulations and low baseband DSP overhead, making them particularly promising candidates for high-speed mm-wave systems.

William H. Doherty, back in 1936, proposed two generic PA architectures employing either parallel or series combiners to realize active load modulations for PA PBO efficiency enhancement [1]. Different from parallel Doherty combiner that intrinsically scales up the load impedance, series Doherty combiner naturally down-scales the load and is particularly appealing for high-power PAs in voltage-limited Si processes. However, mm-wave series Doherty combiners entail various practical design challenges (Fig. 26.2.1). For example, transformer series combiners face compromised performance at high mm-wave and degraded balancing due to strong coil-coil capacitive coupling, while λ/4 transmission-line (T-line) approaches are area-consuming and cannot easily support differential PAs. Existing on-chip series combiners also exhibit poor passive efficiency that substantially reduces the Doherty PBO efficiency enhancement in practice.

Several Si-based mm-wave Doherty PAs are reported [2,3]. However, the PA PBO efficiency increase is marginal compared to Class-B PA, or there is significant degradation on the peak PA efficiency, both of which are mainly due to the lossy Doherty combiners and imperfect main/auxiliary PAs cooperation.

We propose a mm-wave Doherty radiator topology that exploits a multi-feed on-chip antenna to achieve antenna-based close-to-ideal series power combining and thus high-performance Doherty operation. Merging the series Doherty combiner with the antenna also yields a compact radiator design within a single-antenna footprint and reduced on-chip passive networks, making it especially suitable for massive MIMOs. Moreover, different from spatial outphasing or spatial I/Q power combining [4,5], our radiator directly achieves its Doherty operation on the antenna before any radiation, ensuring a consistent Doherty performance and undistorted modulations over a wide field of view (FoV). In addition, GHz-bandwidth adaptive biasing is employed in the auxiliary path to enhance Doherty main/auxiliary PA cooperation.

To construct an on-antenna series power combiner, we select two symmetrical locations on a one-λ wire loop antenna to form two ports (Fig. 26.2.1). The driving impedance of this 2-port loop antenna can be analyzed using its [Y] matrix. When port 1 is excited with a voltage V_e and port 2 is short-circuited, a standing wave current is established on the antenna. Assuming no loss for simplicity, the one-λ total loop length and symmetry ensure that the two currents I_1 and I_2 are equal in both magnitude and phase. Consequently, the 2-port one-λ loop-antenna [Y] matrix is identical to that of an ideal series combiner, so that it realizes on-antenna series power combining and simultaneously radiates out the combined power (Fig. 26.2.1). Moreover, as the power is combined directly on the antenna, it typically offers lower loss than conventional on-chip power combining structures.

To complete the series Doherty combiner, the auxiliary path adopts a λ/4 impedance inverting network as a capacitively loaded T-line, so that the T-line length is only 35° for size reduction. We also shape the antenna ground to increase the instantaneous bandwidth of the on-chip antenna. 3D EM simulations show that the antenna-based Doherty network achieves the desired Doherty load modulation (Fig. 26.2.2) with a total passive efficiency of 76% including antenna radiation efficiency on high resistivity SOI substrate.

For robust wireless communication, the antenna radiation pattern and the gain of the proposed Doherty radiator must not change during the Doherty operation over the antenna FoV. Otherwise, spatially dependent AM-AM/AM-PM errors will appear to corrupt the transmitted modulations. We set up a 3D EM simulation to model the full wireless communication link, where our Doherty radiator acts as a transmitter, and two far-field receiver dipoles are placed with one in the boresight ($\varphi = 0°$, $\theta = 180°$) and the other in a non-boresight ($\varphi = 0°$, $\theta = 225°$) direction (Fig. 26.2.2). Assuming main/auxiliary PAs follow the idealistic Class-B operation, the received signals in both directions show excellent large-signal linearity with <0.2dB AM-AM and <1.5° AM-PM variations through the Doherty operation (Fig. 26.2.2).

In the active circuit designs, we use an identical two-stage PA design for the main and auxiliary PAs, each consists of a common-source driver and a cascode PA. Compact transformer matching is used at the input and inter-stage. We also employ two high-Q T-line inductors to resonate out the PA device output capacitance. In parallel, we design a high-speed adaptive biasing in the auxiliary path to improve main/auxiliary PA cooperation. It is worth mentioning that using the adaptive biasing only at the auxiliary PA is often inadequate. Even at deep PBO, the auxiliary driver output can be sufficiently large to unwantedly turn on the auxiliary PA. In this work, we apply the adaptive biasing to both the auxiliary driver and the PA to ensure that the auxiliary path is completely turned off below 6dB PBO and is rapidly turned on above 6dB PBO. At 0dB PBO, the auxiliary PA gate bias is raised to the similar value as the main PA (0.3V).

The 62-to-68GHz Doherty radiator is implemented in a 45nm CMOS SOI process, occupying 1.7×1.9mm² including the antenna. The IC is flip-chip packaged on a Roger CLTE-AT™ laminate to perform back-side radiation. We first characterize its continuous wave performance using a horn antenna and a power sensor at the far field. The output power (P_{out}) of the Doherty radiator is the measured EIRP minus the antenna gain. A separate on-chip antenna test structure is used to measure the antenna gain. At 65GHz, the measured antenna gain is 4.5dBi. Next, the Doherty radiator EIRP is measured, based on which the Doherty radiator P_{out} is obtained and summarized in Fig. 26.2.4. Desired Doherty PBO PAE enhancement and linear large-signal performance are consistently achieved across the operation frequency. At 65GHz, the measured saturated EIRP/P_{sat}/P_{1dB} are 23.9/19.4/19.2dBm in the main lobe direction. The measured total PAE at peak/6dB PBO are 27.5/20.1% respectively including the adaptive biasing circuits power consumption, demonstrating 1.46× PAE enhancement at 6dB PBO over an idealistic Class-B PA. At 62 to 68GHz, the Doherty PAE enhancement at 6dB PBO is 1.45 to 1.53× over an idealistic Class-B PA. Next, we characterize the dynamic performance of the Doherty radiator. Figure 26.2.5 shows the 64-QAM complex-modulation tests over the antenna FoV. Without digital pre-distortion (DPD), at the average EIRP/P_{out} of +19/14.5dBm, the measured EVM and ACPR are respectively -28dB and -26.97dBc in the boresight directions for 3Gb/s 64-QAM modulation, and consistent EVMs are observed over the antenna FoV (approx. -60° to +60°), verifying its spatially consistent Doherty PBO efficiency enhancement and linear transmission.

Compared with the reported 60-to-80GHz silicon PAs/transmitters [2-8] in Fig. 26.2.6, this work achieves the best PAE PBO enhancement ratio at 6dB PBO, the highest PAE at 6dB PBO, and the highest average PAE for 3Gb/s and 6Gb/s 64-QAM modulation transmission, demonstrating the PBO efficiency advantage of Doherty architecture.

Acknowledgements:
We would like to thank GlobalFoundries for chip fabrication and members of Georgia Tech GEMS group for their technical supports.

References:

[1] W. Doherty, "A New High Efficiency Power Amplifier for Modulated Waves", *Proc. of IRE*, vol. 24, no. 9, pp. 1163-1182, Sept. 1936.
[2] K. Greene et al., "A 60-GHz Dual-Vector Doherty Beamformer", *IEEE JSSC*, vol. 52, no. 5, pp. 1373-1387, May 2017.
[3] E. Kaymaksut et al., "Transformer-Based Doherty Power Amplifiers for mm-Wave Applications in 40-nm CMOS," *IEEE TMTT*, vol. 63, no. 4, pp. 1186-1192, Apr. 2015.
[4] C. Liang and B. Razavi, "Transmitter Linearization by Beamforming," *IEEE JSSC*, vol. 46, no. 9, pp. 1956-1969, Sept. 2011.
[5] J. Chen et al., "A Digitally Modulated mm-Wave Cartesian Beamforming Transmitter with Quadrature Spatial Combining," *ISSCC*, pp. 232-233, Feb. 2013.
[6] T. Chi et al., "A 60GHz On-Chip Linear Radiator with Single-Element 27.9dBm Psat and 33.1dBm Peak EIRP Using Multifeed Antenna for Direct On-Antenna Power Combining", *ISSCC*, pp. 296-297, Feb. 2017.
[7] K. Khalaf et al., "Digitally Modulated CMOS Polar Transmitters for Highly Efficient mm-Wave Wireless Communication," *IEEE JSSC*, vol. 51, no. 7, pp. 1579–1592, July 2016.
[8] A. Komijani and A. Hajimiri, "A Wideband 77-GHz, 17.5-dBm Fully Integrated Power Amplifier in Silicon," *IEEE JSSC*, vol. 41, no. 8, pp. 1749-1756, Aug. 2006.

 978-1-5090-4940-0/18/$31.00

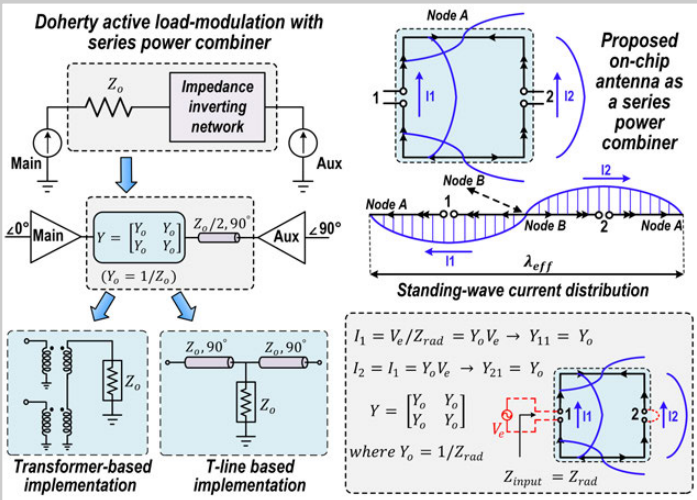

Figure 26.2.1: The realization of a Doherty power amplifier with a series power combiner, proposed on-chip one-λ wire loop antenna as series combiner, and [Y] matrix derivation of the proposed antenna-based series combiner.

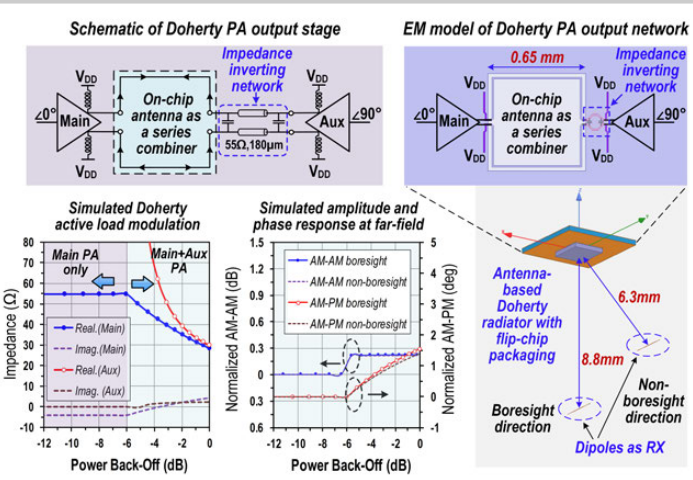

Figure 26.2.2: Proposed antenna-based Doherty PA output stage, 3D EM model of the proposed Doherty-radiator output stage, simulated Doherty active load modulation, and simulated amplitude and phase response received by far field dipoles assuming Main/Auxiliary PAs follow an ideal Class-B PA.

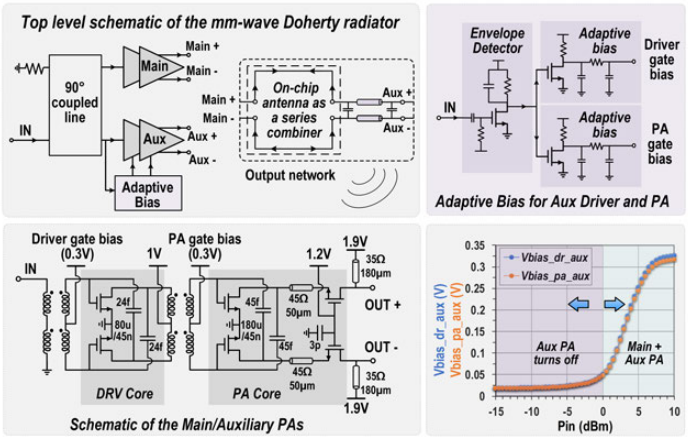

Figure 26.2.3: Top-level schematic of the proposed Doherty radiator, schematic of the Main/Auxiliary PAs, schematic of high-speed adaptive bias circuit for the auxiliary Driver and PA, and performance of adaptive bias outputs versus input power.

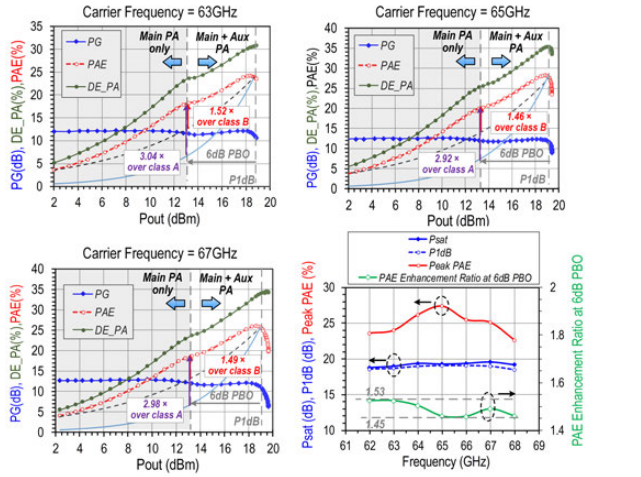

Figure 26.2.4: CW measurement of the proposed Doherty radiator at 63/65/67GHz and the CW performance summary from 62 to 68GHz (the PAE enhancement ratio at 6dB PBO is compared to an idealistic Class-B PA with the same PAE at P_{1dB}).

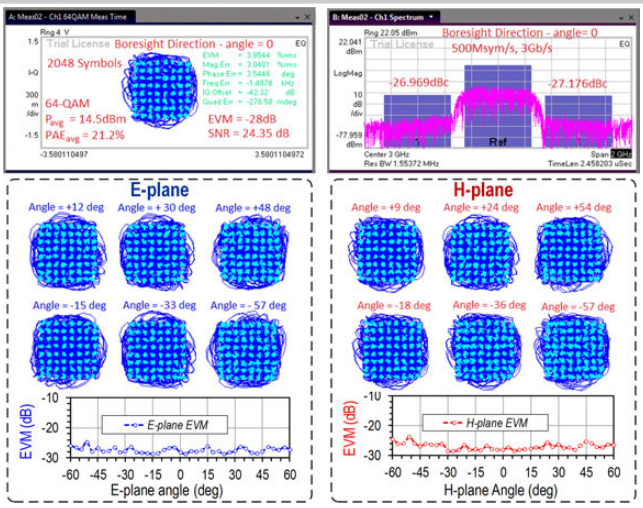

Figure 26.2.5: Modulation results of the Doherty radiator with 64-QAM modulation at 0.5Gsym/s at boresight direction and in various directions over the antenna Field-of-View.

	This work	[2] Greene, JSSC' 17	[3] Kaymaksut, TMTT'15	[5] Chen, ISSCC' 13	[6] Chi, ISSCC' 17	[7] Khalaf JSSC'16	[8] Komijani JSSC'07
Architecture	Antenna-based Doherty	Doherty	Doherty	Spatial IQ combining	On antenna power combiner	Digital Polar Tx	Class AB
Frequency (GHz)	65	62	72	60	60	60	77
V_{DD} (V)	1 (Driver) 1.9 (PA)	2.8 (Driver) 3.6 (PA)	1.5	1	1 (Driver) 2 (PA)	0.9	1.8
P_{sat}(dBm)	19.4	17.5*	21	9.6	27.9	10.8	17.5
P_{1dB} (dBm)	19.2	17.1	19.2	9.6	25	7.4	14.5
Peak PAE	28.3%	23.7%*	13.6%	28.5%	23.4%	29.8%	12.8%
PAE @ P_{1dB}	27.5%	23.7%	12.4%	28.5%	16.2%	15% *	11.8%*
PAE @ 6dB PBO	20.1%	13%	7%	14.25%*	6%*	4.5% *	3%*
PAE Enhancement Ratio at 6dB PBO**	1.46	1.10	1.13	1	0.74	0.6	0.51
Mod. Scheme Data Rate EVM P_{avg} PAE_{avg}	64-QAM 3Gb/s -28dB EVM 14.5dBm 21.2% / 64-QAM 6Gb/s -26.7dB EVM 14.2dBm 20.2%	N/A	64-QAM 0.6Gb/s -25.6dB EVM +15.9dBm 7.2% PAE	16-QAM 6Gb/s -16.2dB EVM +6dBm* 16.5% PAE	64-QAM 4.8Gb/s -25.4dB EVM +19.3dBm --	16-QAM 6.7Gb/s -18.1dB EVM +3.6dBm --	N/A
Technology	45nm CMOS SOI	130nm SiGe BiCMOS	40nm CMOS	65nm CMOS	45nm CMOS SOI	40nm CMOS	120nm SiGe BiCMOS

* Estimated from reported figures

** Compared to an idealistic class-B PA with the same PAE at P_{1dB}

Figure 26.2.6: Table of comparison with prior PAs/transmitters operating from 60 to 80GHz.

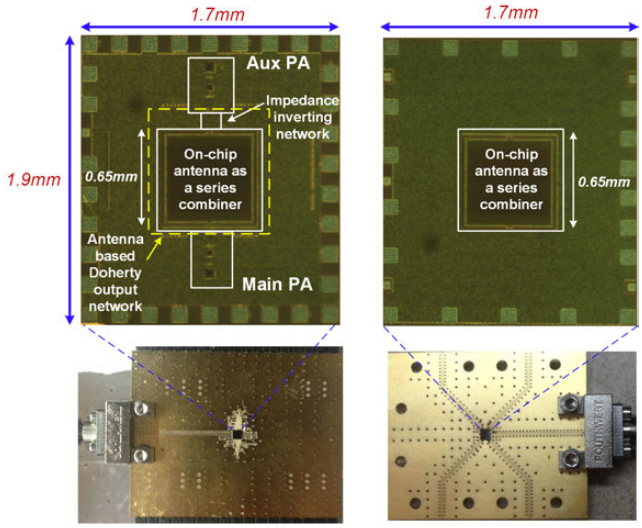

Figure 26.2.7: Die micrographs of the Doherty Radiator, the antenna test structure, and photos of the flip-chip packaged PCBs.

978-1-5090-4940-0/18/$31.00

26.3 A 69-to-79GHz CMOS Multiport PA/Radiator with +35.7dBm CW EIRP and Integrated PLL

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Low-cost mm-wave silicon integrated signal generation and processing enable many applications, such as silicon-based automotive radars for self-driving cars and wireless communications. Some challenges encountered in commercialization of such systems are the high packaging and testing costs and high sensitivity to antenna parameters, which can diminish the advantage of integrated silicon solutions. On-chip antennas have been proposed as a solution to reduce the packaging costs [1,2]. Link budget analysis of systems (e.g., radar) necessitates high-power (high EIRP) transmitters while system resolution analysis suggests higher frequency of operation for better spatial resolution. The scaling of CMOS transistors facilitates the latter requirement, but, unfortunately, the lower breakdown voltage of the transistors reduces their maximum power handling capabilities at a given radiator impedance. Several approaches have already been implemented to address this issue, each with its own shortcoming. Power-combining multiple PA outputs with passive on-chip power combiners [3] adds extra loss and reduces the overall efficiency, spatial power combining using phased arrays [4] consumes a large die area. Power combining at the antenna [5,6] has been proposed as an approach to address these challenges. In this paper, we propose a spatial PA/radiator power combining approach with optimal PA-load design using strongly coupled antennas in close proximity. This approach utilizes techniques of power combining in free space resulting in favorable drive-point impedance design and using on-chip PAs and radiators to achieve high radiated output power.

Figure 26.3.1 shows the concept of the proposed strongly coupled radiator and its associate impedance scaling. A single slot antenna has a radiation impedance of around 520Ω and thus only radiates around 1mW if driven with a 1V swing. If a second strongly coupled slot in close proximity to the first one is driven in phase, the total radiated power increases fourfold; similarly, three slots radiate 9mW, and the quadratic trend holds up for slots placed in such fashion so long as the overall dimension is smaller than roughly one wavelength. The quadratic increase in radiated power is due to the simultaneous reduction of the drive-point impedance and the increased number of the power sources. The addition of a strongly coupled slot radiator increases the total radiated power not only by increasing the number of power sources but also by increasing the radiated power of each slot through lowering the drive-point impedance. Unlike previous spatial power-combining methods, the proposed array of slots does not significantly change the radiation pattern compared to a single-element antenna.

We implemented a 16-element slot array of the proposed radiator in the top aluminum layer of a 65nm bulk CMOS process. Figure 26.3.2 shows the dimensions of the implemented radiator as well as the topology of 8 PAs and their transistor sizing. Each PA is a pseudo-differential cascode stage with a 24pH shunt inductor to resonate the parasitic capacitance of the cascode node and drives two slots by utilizing a virtual ground between them, as shown Fig. 26.3.2. By properly designing the slot length, we are able to completely absorb the parasitic capacitance of the PA output node into the antenna structure. The antenna also provides the DC power to the PA, eliminating the need for RF chokes and improving the PA efficiency. All the PAs are driven in-phase through a differential 77GHz binary-tree clock-distribution network.

To allow for FMCW operation, a PLL with a multiplication ratio of 32 was implemented to generate a 10GHz BW chirp using a synthesized 2.156-to-2.469GHz reference signal. The block diagram of the PLL is shown in Fig. 26.3.3. The closed loop BW of the PLL is higher than 20MHz, allowing fast chirp rates. The VCO has a tuning range of 67.9 to 80.6GHz, while the PLL locking range was 69 to 79GHz. The measured phase noise of the PLL is -96.4dBc/Hz at 1MHz offset. This is obtained by downconverting the radiated power using the 5th harmonic of PMP MOD-WM harmonic mixer.

Electromagnetic simulations indicate that the radiation efficiency of the radiator can be improved from 46% to 52% by using a low-cost 6.35mm diameter alumina hemispherical lens, which increases the directivity of the antenna from 5 to 10dBi and also improves heat dissipation. Full 3D pattern measurements of the radiator with the lens were performed over the full frequency span from which the directivity of the radiator was obtained. Figure 26.3.4 shows the highlights of these measurements.

The EIRP of the radiator at broad side was measured using Agilent V8486A and W8486A power sensors with 15dBi WR-15 and 25dBi WR-12 standard horns, respectively. The calculated gain of the horn antennas vs. frequency [7] matches the datasheet at provided frequency points. Total radiated power (TRP) was calculated from the measured EIRP and measured radiator directivity. The PA efficiency and total output power can be calculated from TRP and the simulated antenna efficiency. Figure 26.3.5 shows these measurement results. The radiator achieves a peak EIRP of +35.7dBm at 71.25GHz when running continuously from a V_{DD}=1.8V supply and consumes 1006mA of current. The measurements correspond to a maximum TRP of +24.4dBm with a peak directivity of 12.2dBi. The combined PA peak output power is +27.4dBm with a drain efficiency of 30.8%. Simulations indicate that the output power varies by less than 20% across the PAs due to presence of edge effects in the structure.

A comparison table provided in Fig. 26.3.6 summarizes the results of this work and compares them against other works.

Acknowledgment:
The authors would like to thank Dr. Florian Bohn for helpful discussions and Dr. Amirreza Safaripour for assistance in testing. This work was supported by Caltech Innovation Initiative (CI^2) research grant.

References:
[1] S. Bowers et al., "An integrated traveling-wave slot radiator," *IEEE RFIC*, pp. 369-372, June 2014.
[2] A. Babakhani et al., "A 77GHz 4-Element Phased Array Receiver with On-Chip Dipole Antennas in Silicon," *ISSCC*, pp. 629-638, Feb. 2006.
[3] C. Chappidi and K. Sengupta, "A Frequency-Reconfigurable mm-Wave Power Amplifier with Active-Impedance Synthesis in an Asymmetrical Non-Isolated Combiner", *ISSCC*, pp. 344-345, Feb. 2016.
[4] W. Shin et al., "A 108–114 GHz 4×4 Wafer-Scale Phased Array Transmitter with High-Efficiency On-Chip Antennas," *IEEE JSSC*, vol. 48, no. 9, pp. 2041-2055, Sept. 2013.
[5] A. Natarjan et al., "A 77GHz Phased-Array Transmitter with Local LO-Path Phase-Shifting in Silicon," *ISSCC*, pp. 639-648, Feb. 2006.
[6] T. Chi et al., "A 60GHz On-Chip Linear Radiator with Single-Element 27.9dBm Psat and 33.1dBm Peak EIRP Using Multifeed Antenna for Direct On-Antenna Power Combining," *ISSCC*, pp. 296-297, Feb. 2017.
[7] RF Wireless World, "Horn Antenna Calculator, Accessed on Aug. 10, 2017, <http://www.rfwireless-world.com/calculators/Horn-Antenna-Calculator.html>
[8] B. Sadhu et al., "A 60GHz Packaged Switched Beam 32nm CMOS TRX with Broad Spatial Coverage, 17.1dBm Peak EIRP, 6.1dB NF at < 250mW," *IEEE RFIC*, pp. 342-343, May 2016.
[9] P. N. Chen et al., "A 94GHz 3D-Image Radar Engine with 4TX/4RX Beamforming Scan Technique in 65nm CMOS," *ISSCC*, pp. 146-147, Feb. 2013.

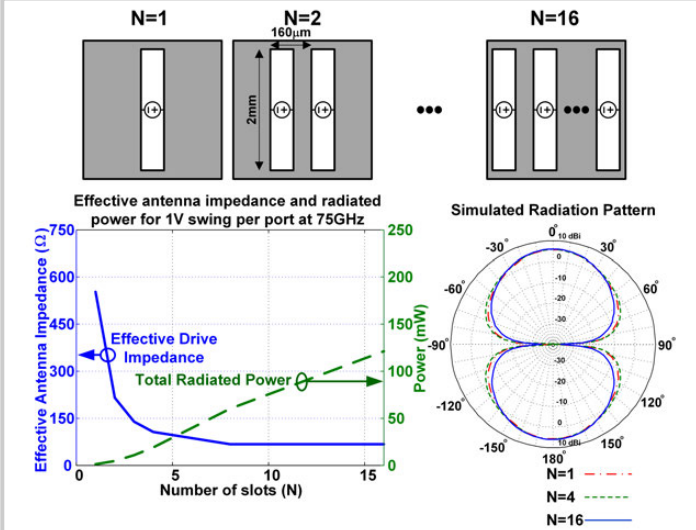

Figure 26.3.1: Impedance- and radiated-power scaling of tightly coupled slot array antennas.

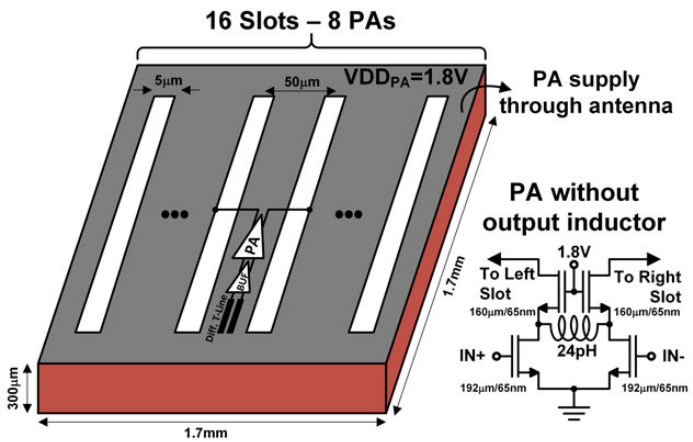

Figure 26.3.2: Eight differential cascode PAs drive 16 slots. The radiator is designed to absorb the parasitic capacitance of PA output.

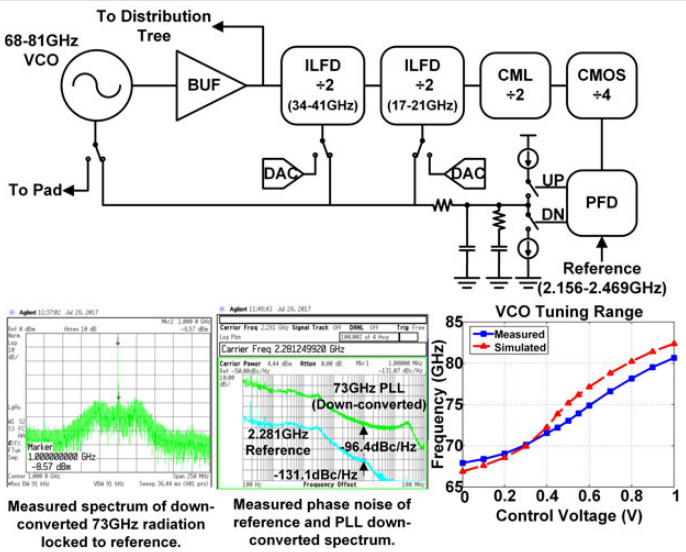

Figure 26.3.3: PLL block diagram and measurement results.

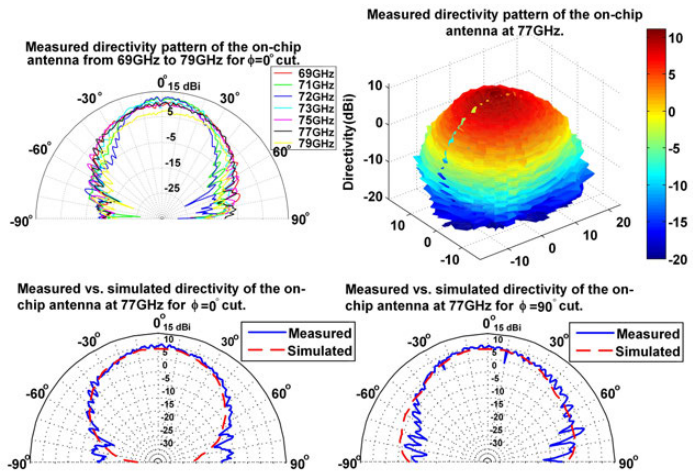

Figure 26.3.4: Measured and simulated radiation pattern of the radiator.

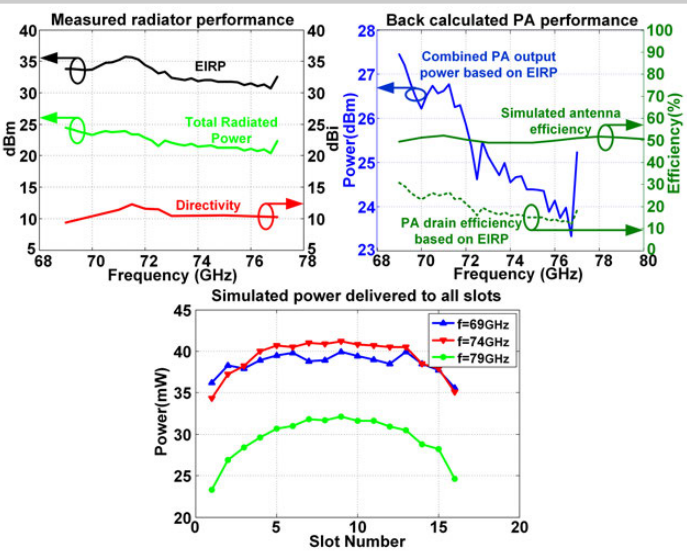

Figure 26.3.5: Radiator and PA performance.

	This Work	[1]	[4]	[6]	[8]	[9]
Process	**65nm CMOS**	32nm SOI	180nm SiGe	45nm SOI	32nm SOI	65nm CMOS
Frequency(GHz)	**69-79**	134.5	108-114	53-63	58.3-60.5	88-99
EIRP(dBm)	**35.7**	6.0	24.5	33.1	17.1	35
On Chip Antenna	**YES**	YES	NO	YES	NO	NO
Radiator Directivity (dB)	**12.2**	7.1	17	6.9	32.5	36 (Dish Ant.)
Tot. Rad. Power (dBm)	**24.4**	-1.3	7.5	26.2	N/A	0
Antenna Efficiency	**52%**	39%	45%	74.5% (Uses High Res. Sub.)	N/A	N/A
PA P_{sat}(dBm)	**27.4**	N/A	11	27.9	N/A	N/A
PA Efficiency	**30.8% (Drain Eff.)**	N/A	N/A	23.4% (PAE)	N/A	N/A
Phase Noise (dBc/Hz)	**-96.4@1MHz**	N/A	N/A	N/A	-113 @10MHz	-85.6 @1MHz
Total DC Power(W)	**PA+PLL/Distrib 1.81+0.55=2.36**	0.17	3.4	N/A	0.23	0.6
Chip Area(mm^2)	**2.9**	1.2	39	10.5	9 (RX+TX)	4.32 (RX+TX)

Figure 26.3.6: Comparison with other works.

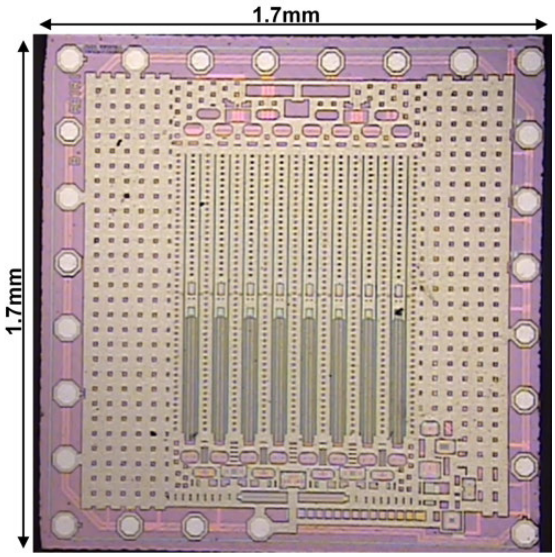

Figure 26.3.7: Die micrograph.

978-1-5090-4940-0/18/$31.00

26.4 A 28GHz 41%-PAE Linear CMOS Power Amplifier Using a Transformer-Based AM-PM Distortion-Correction Technique for 5G Phased Arrays

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[1]Washington State University, Pullman, WA, [2]MaxLinear, San Diego, CA

To fulfill the insatiable demand for high data-rates, the millimeter-wave (mmW) 5G communication standard will extensively use high-order complex-modulation schemes (e.g., QAM) with high peak-to-average power ratios (PAPRs) and large RF bandwidths. High-efficiency integrated CMOS power amplifiers (PA) are highly desirable for portable devices for improved battery life, reduced form factor, and low cost. To meet simultaneous requirements for high efficiency and reasonable linearity, PAs intended for use with complex modulation are often operated in Class-AB mode [1,2]. For small input amplitude in Class-AB, the device is turned-on and has an input capacitance (C_{gs}) of ~$(2/3)WLC_{ox}$. As the input amplitude becomes large, the device turns-off for part of the RF cycle, thus reducing its effective input capacitance. This input capacitance-modulation effect creates an input-amplitude-dependent phase shift in Class-AB mode resulting in an amplitude-modulation to phase-modulation (AM-PM) distortion [2]. Consequently, it degrades linearity metrics (e.g., error vector magnitude (EVM), adjacent channel power ratio (ACPR)) in complex-modulation systems. External linearization techniques (e.g., digital pre-distortion) are often used in transmitters to meet linearity requirements, but they are complex in nature and expensive to implement. Apart from these, few works at low-GHz frequencies are reported to improve the PA's intrinsic linearity using a varactor- or PMOS-based AM-PM correction methods [1,2]. These works reduce the design overhead of external linearization systems; however, the inclusion of additional capacitive element to correct AM-PM degrades gain and efficiency, which is not optimal for mmW frequencies [1,2].

To address linearity, without degrading performance or introducing dramatic design complexity, we propose a 2-stage linear PA architecture where a compensation transformer is integrated into the amplifier chain to correct AM-PM distortion while maintaining high power efficiency. Figure 26.4.1 shows the conceptual architecture and waveforms of the proposed technique. The 1st and 2nd amplifiers are driver (DA) and power (PA) stage, respectively, and both are biased at Class-AB. A harmonically tuned, continuous Class-F load network is used in the 2nd-stage for high efficiency [3]. The transformer (T_C) acts as an analog pre-distortion network, which is used to compensate for the AM-PM phase shift from the 2-stage amplifier. The proposed T_C samples the RF signal from the input of the DA and generates a nonlinear phase response of θ_C. The magnitude response of the θ_C is designed to be larger than the inherent phase response of the DA, θ_{DA} (i.e. $|\theta_C| > |\theta_{DA}|$). The 2nd stage has a phase response of θ_{PA}, and the design conditions (such as device size, bias level etc.) of this stage are set such that $\theta_{PA}=-\theta_{S1}$, where $\theta_{S1}=\theta_C+\theta_{DA}$. Thus, the net AM-PM distortion is reduced.

Figure 26.4.2 shows the complete schematic of the proposed architecture. The primary coil of the transformer is connected at the input signal path, while the secondary coil of the transformer is connected to an NMOS switch (M_{sw}). The gate terminal of the M_{sw} taps into the gate of the DA's device (M_1), while the drain and source nodes are connected to a large-resistor for well-defined dc bias. As the input power (P_{in}) rises in magnitude (large-signal), the net impedance of T_C primary coil creates an inverse characteristic in comparison to the net impedance created by C_{gs1} in the DA. By appropriately selecting the size of T_C and thereby controlling the net impedance change across P_{in}, a desired phase shift of θ_{S1} can be generated at the output of DA. The layout and the equivalent circuit of the transformer for M_{sw} on and off are shown in Fig. 26.4.2. If M_{sw} is off, there is no current flow in the secondary coil of T_C; therefore, the net inductance in primary coil remains unchanged (i.e. $L_{eq,off} = L_{cp}$). Conversely, when M_{sw} is on, the secondary coil develops an opposing net current of i_{cs}, which reduces the net inductance to a lower value in primary coil, $L_{eq,on} = L_{cp}(1-k_c^2)$. The net impedance waveform for a large signal is shown in Fig. 26.4.2 for both T_C and C_{gs1} across P_{in}.

The proposed AM-PM correction technique offers three key benefits for enhancing PA large-signal performance. First, the control signal of the transformer is directly tapped from the input of the DA's gate terminal, thus there is no need to implement any additional control circuitry. Since the tapped signal is in RF domain the correction process is instantaneous and synchronized with the DA's large-signal behavior, unlike the phase adjusting method in [2] limited to baseband operation. Second, designers can allow lower quiescent bias current in the DA thus generating higher efficiency in contrast to typically designed low-efficiency Class-A DA. Finally, due to the inductive linearization, the net capacitive impedance at the input of the DA reduces; hence, high gain and efficiency can be achieved in the DA compared to other capacitive-based linearization methods as in [1].

To demonstrate the proposed technique, a PA prototype is fabricated in a 65nm CMOS process. Deeply scaled CMOS process used in moderate-to-high $P_{o,sat}$ (e.g., >10dBm) levels pose stability concerns due to an increased Miller effect from a large gate-drain capacitance (C_{gd}). Hence, PAs often need to operate at compromised performance levels. To cope with this adverse effect, we integrate a tunable gate-drain transformer (T_{N1} and T_{N2}) feedback neutralization network as implemented in [4], in both stages using a switched-substrate-shield layout (SSL) technique [5]. The continuous Class-F output matching network is designed using a multi-order tuned network consisting of 3rd-order harmonic matching [3]. Furthermore, a tunable inductor (L_{int}) using the SSL technique is integrated into the inter-stage matching network. These tunable components (T_{N1}, T_{N2}, and L_{int}) provide flexibility to compensate PVT variations and mismatch, ensuring high performance.

Results of the AM-PM phase distortion at the 1st (DA), 2nd (PA), and 2-stage amplifier are shown in Fig. 26.4.3. Less than 0.7° measured phase distortion is achieved at P_{1dB} for the 2-stage amplifier at 28GHz. The distortion is about 1.3° near P_{sat} at 28GHz, enabling amplification of large PAPR signals like 64/256-QAM with low EVM. The PA achieves <1° measured phase distortion at P_{1dB} across 27 to 31GHz. The large-signal performance for 1-tone signals are presented in Fig. 26.4.4. A PAE_{sat} of 41% at 28GHz for $P_{o,sat}$ of 15.6dBm is achieved. The PAE_{sat} varies between 38 and 41% from 26 to 29GHz while maintaining P_{sat}>15dBm. The PA is tested under 64/256/512-QAM signals with 340/50/20MSym/s data-rate with measurement results summarized in Fig. 26.4.5. Due to the low AM-PM distortion at P_{1dB} to P_{sat} level, the PA shows high average power-efficiency for high-order-QAM signals without any external phase pre-distortion, while maintaining excellent EVM and ACPR results. The proposed technique dramatically improves the PA large-signal performance while reducing the complexity and implementation cost as compared with traditional works.

Figure 26.4.6 summarizes recently reported silicon PAs intended for 5G band. At 28GHz, the proposed linear PA amplifies a 340MSym/s 64-QAM signal with –26.4dB EVM and –30dBc ACPR while achieving PAE of 18.2% at +9.8dBm of $P_{o,avg}$. Figure 26.4.7 shows the die micrograph of the PA with an active area of only 0.24mm^2.

Acknowledgements:
This work was supported in part by the U.S. NSF under Grant CNS-1705026, CNS-1564014, the Joint Center for Aerospace Technology Innovation (JCATI), and the NSF Center for Design of Analog–Digital Integrated Circuits (CDADIC). We also thank Keysight Technologies for measurement support.

References:

[1] C. Wang et al., "A Capacitance-Compensation Technique for Improved Linearity in CMOS Class-AB Power Amplifiers," *IEEE JSSC*, vol. 39, no. 11, pp. 1927-1937, Nov. 2004.

[2] Y. Palaskas et al., "A 5-GHz 20-dBm Power Amplifier with Digitally Assisted AM-PM Correction in a 90-nm CMOS Process," *IEEE JSSC*, vol. 41, no. 8, pp. 1757-1763, Aug. 2006.

[3] S.N. Ali et al., "A 42–46.4% PAE Continuous Class-F Power Amplifier with C_{gd} Neutralization at 26–34 GHz in 65 nm CMOS for 5G Applications," *IEEE RFIC*, pp. 212-215, June 2017.

[4] S.N. Ali et al., "Reconfigurable High Efficiency Power Amplifier with Tunable Coupling Coefficient Based Transformer for 5G Applications," *IEEE IMS*, pp. 1177-1180, June 2017.

[5] P. Agarwal et al., "Switched Substrate-Shield-Based Low-Loss CMOS Inductors for Wide Tuning Range VCOs," *IEEE TMTT*, vol. 65, no. 8, pp. 2964-2976, Aug. 2017.

[6] S. Shakib et al., "A Highly Efficient and Linear Power Amplifier for 28-GHz 5G Phased Array Radios in 28-nm CMOS," *IEEE JSSC*, vol. 51, no. 12, pp. 3020-3036, Dec. 2016.

[7] S. Hu et al., "A 28GHz/37GHz/39GHz multiband linear Doherty power amplifier for 5G massive MIMO applications," *ISSCC*, pp. 32-33, Feb. 2017.

[8] B. Park et al., "Highly Linear mm-Wave CMOS Power Amplifier," *IEEE TMTT*, vol. 64, no. 12, pp. 4535-4544, Dec. 2016.

[9] M. Vigilante and P. Reynaert, "A 29-to-57GHz AM-PM compensated class-AB power amplifier for 5G phased arrays in 0.9V 28nm bulk CMOS," *IEEE RFIC*, pp. 116-119, June 2017.

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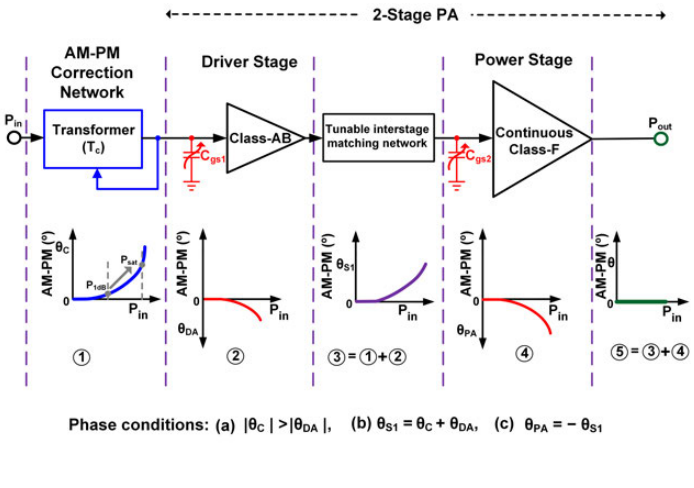

Figure 26.4.1: Architecture of the proposed AM-PM-distortion correction technique for mmW CMOS PA.

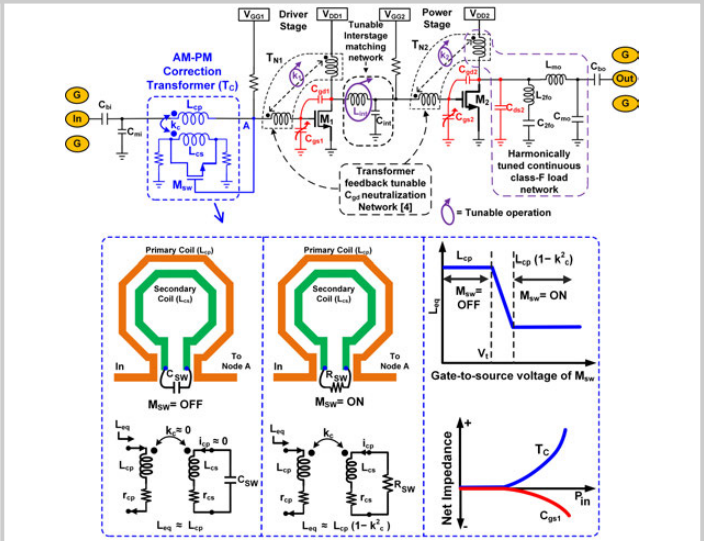

Figure 26.4.2: Schematic of the proposed 2-stage linear PA network incorporating a transformer based AM-PM-distortion correction network.

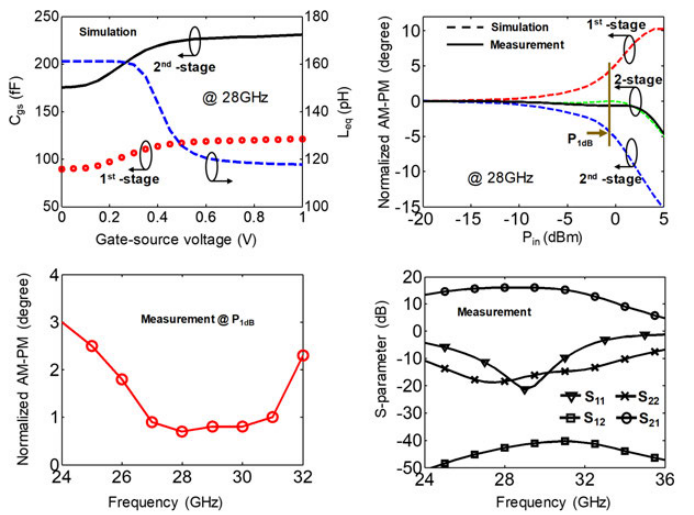

Figure 26.4.3: Results of C_{gs}, L_{eq}, AM-PM, and small-signal S-parameters.

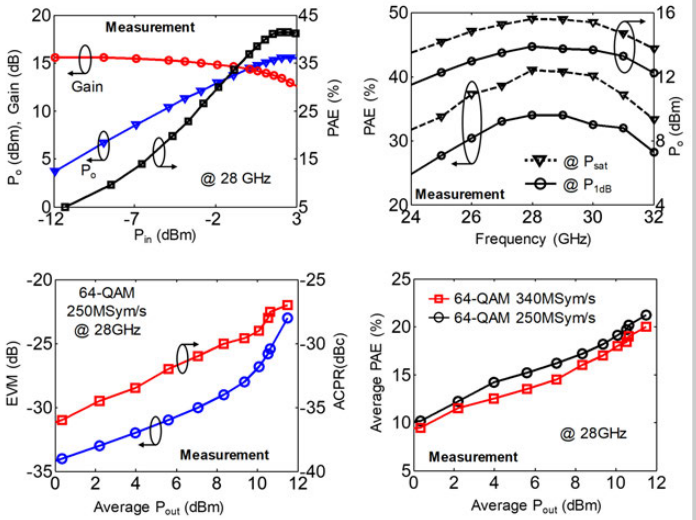

Figure 26.4.4: Measurement results of large-signal and linearity metrics.

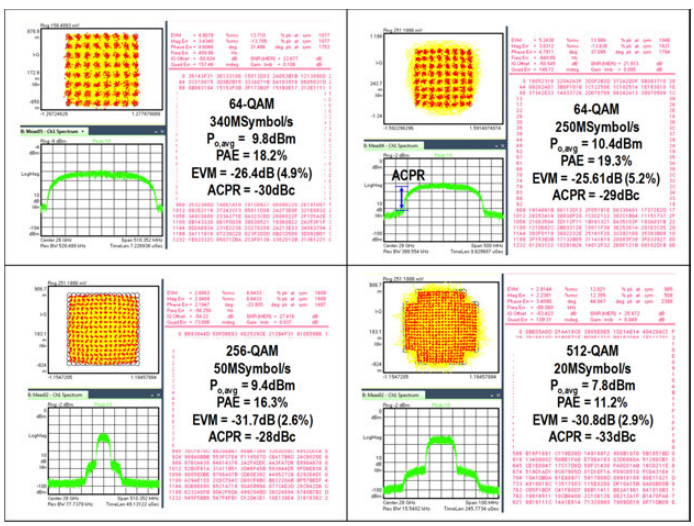

Figure 26.4.5: Measurement results of demodulated signals at 28GHz.

Ref.	This Work	JSSC'16 [6]	ISSCC'17 [7]	TMTT'16 [8]	RFIC'17 [9]
Tech.	65nm CMOS	28nm CMOS	130nm SiGe	28 nm CMOS	28nm CMOS
Freq. (GHz)	28	30	28	28	34
V_{DD} (V)	1.1	1.0	1.5	1.1	0.9
Gain (dB)	15.8	15.7	18.2	10	20.8
$P_{o,1dB}$ (dBm)	14	13.2	15.2	14	13.4
$P_{o,sat}$ (dBm)	15.6	14	16.8	14.8	16.6
PAE_{1dB} (%)	34.7	34.3	19.5	35.2	12.6
PAE_{max} (%)	41	35.5	20.3	36.5	24.2
AM-PM (deg.) @P_{1dB}	0.7	NA*	NA	NA	1.1#
Modulated Signal Measurement Results	64-QAM 340Msym/s +9.8dBm -26.4dB EVM -30dBc ACPR 18.2%PAE	64-QAM 250Msym/s +4.2dBm -25dB EVM -26.4dBc ACPR 9%PAE	64-QAM 500Msym/s +9.2dBm -27dB EVM -28.4dBc ACPR NA	64-QAM 80Msym/s +6.8dBm -27.4dB EVM -34dBc ACPR 16.5% PAE	64-QAM 337Msym/s +10.1dBm -25dB EVM -32.1dBc ACPR 5.8% PAE
	256-QAM 50Msym/s +9.4dBm -31.7dB EVM -28dBc ACPR 16.3%PAE	NA	NA	NA	NA
Active Area (mm^2)	0.24	0.16	1.76**	0.28	0.16
Topology	Transformer based AM-PM correction	Inductive source degeneration	Doherty	2nd harmonic short, common-source	PMOS varactor based AM-PM compensation

*Including pads (total area). *Not available. #Estimated from graph

Figure 26.4.6: Comparison with mmW silicon PAs.

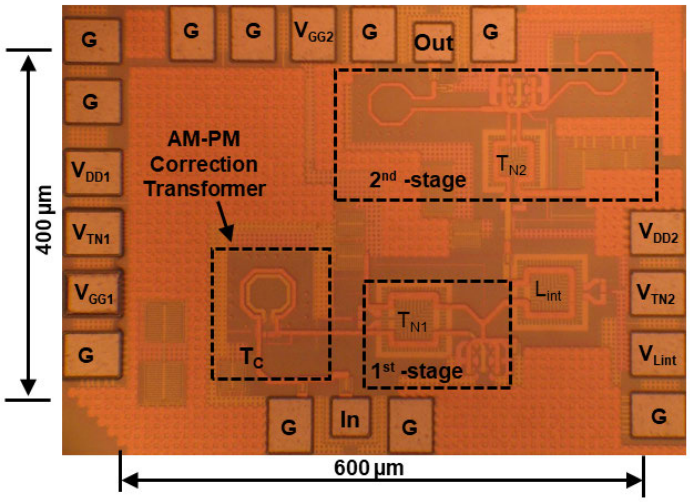

Figure 26.4.7: Die micrograph in a 65nm CMOS technology.

978-1-5090-4940-0/18/$31.00

26.5 A Compact Dual-Band Digital Doherty Power Amplifier Using Parallel-Combining Transformer for Cellular NB-IoT Applications

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Narrowband Internet-of-Things (NB-IoT) is a newly developed 3GPP protocol optimized for low-power wide-area IoT applications and is evolving toward the future fifth-generation (5G) mobile communication. It specifies at least 23dBm maximum output power for long-range communication, stringent emission mask compatible with guard-band or in-band scenarios, and it supports multiple operation bands from 699 to 915MHz (LB) and from 1710 to 1980MHz (HB). For cost reduction, longer battery life, and fast time to market, the integration of high-power high-efficiency power amplifiers (PAs) on-chip is greatly demanded. To benefit from advanced CMOS technology, the digital polar transmitter has become a very attractive architecture for NB-IoT applications [1]. To simultaneously support dual bands for user flexibility, the traditional solution is to implement two separately optimized PAs [2], which requires extra design effort and increases die area. An ultra-compact single-transformer-based parallel power combiner proposed in [3] provides optimum load transformation in the two operation bands. Moreover, to support higher throughputs and achieve better spectral efficiency, high peak-to-average-power-ratio (PAPR) multi-subcarrier modulation is adopted in NB-IoT, which requires the PA to be efficient not only at peak power but also at power back-off (PBO) to extend battery life. Efficiency boosting techniques of digital Doherty PAs have been shown in [4-6], but two transformers are needed in the passive network. In this work, a high-power digital Doherty PA for NB-IoT applications is proposed and introduces a parallel-combining-transformer (PCT) power combiner for dual-band coverage, back-off efficiency enhancement, and ultra-compact implementation.

Figure 26.5.1 illustrates the operations of proposed Doherty PA through a PCT combiner. The 3-coil current-mode combiner acts as a 4-way power combiner, where the two primary coils are driven by two differential PA pairs to collect their output currents and provide optimum load transformation. The transformer combiner is configured as shown in Fig. 26.5.1 to maintain both PA pairs quasi-differential and close to each other, which is critical to minimize differential mismatch and to reduce effective ground parasitics. At peak power, both PAs are fully switched on and the currents flow through the two primary coils in-phase at full amplitude. Here, the single-ended impedance seen by each PA is 50Ω. In the case where both PAs are controlled synchronously, load impedance of each PA stays the same when output power is gradually backed off from peak. If operated as Class-B mode, at 6dB PBO, the DC power consumption is only reduced by half, which suffers from 50% efficiency degradation. In this work, each PA pair is controlled independently to perform as a Doherty PA. With output power decreased, output power from PA2 is gradually reduced, and the single-ended impedance seen by PA1 starts to increase until it reaches 100Ω. Then, an efficiency peaking at 6dB PBO is achieved when PA2 is fully switched off, thereby enhancing the average efficiency.

Figure 26.5.2 shows the block diagram of proposed digital Doherty PA. The switched-capacitor digital PA is employed due to its good linearity and efficiency. To meet the stringent NB-IoT emission mask, a total resolution of 10 bits is adopted, where PA1 and PA2 are identical 9b sub-PAs. To minimize layout mismatch and achieve better resolution, each sub-PA is constructed using a hybrid unary and binary array. The sub-PA is divided into 16 groups with the 4 MSBs, where each group consists of 7 thermometer-coded cells and 2b LSB binary-coded cells. A cascode inverter Class-D topology is employed in the unit PA cell to distribute $2\times V_{DD}$ voltage stress among 4 transistors and provide high output power. Single-ended PM signal is converted by an S-to-D block to generate differential signals, which are further level-shifted to two voltage domains. At off-state, the differential outputs of the unit PA are both connected to ground to avoid different fluctuations between supply and ground. Besides, metal-oxide-metal (MOM) switched capacitors formed by middle metal layers are used to reduce parasitic capacitors. In the floorplan, each sub-PA is arranged in order of groups and the "snake" traverse movements are performed among groups to improve the differential nonlinearities (DNL).

Figure 26.5.3 shows the implementation of dual-band passive matching network. The 3-coil parallel-combining transformer is implemented within a compact single-transformer footprint. PA1 and PA2 are placed at the same side of the transformer to maintain good differential symmetry. The output currents from PA1 and PA2 flow in parallel direction in the two primary coils, which achieves magnetic enhancement and increases the effective primary inductance, thus contributing to further size reduction and lower loss. This is important for on-chip matching design at sub-GHz. The passive matching network of the PA device parasitic capacitors, switched capacitors (C_0), a 3-coil transformer, and 3 capacitors (C_1 and C_2) transforms the optimum load for PA1 and PA2, which realizes two power peaks over LB and HB. The total passive loss from sub-PA to 50Ω load is less than 1.6dB over a wide frequency range. The balun function is implemented on-chip with a single-ended output pad. In this work, a total of 1.2nF decoupling capacitors are integrated to attenuate supply and ground ringing while improving the linearity and noise performance.

The proposed dual-band digital Doherty PA is implemented in a 55nm CMOS process (Fig. 26.5.7) and occupies an area of $1.26\times0.88mm^2$ including all decoupling capacitors and ESD I/O pads. The PA is packaged in a QFN package and surface mounted on an evaluation PCB board with a single-ended LO input and an RF output. The chip operates with dual power supplies of 2.4V and 1.2V, and the power consumption of all IO buffers, LO distribution drivers, logic blocks, and PAs is included in the PAE calculation. The measured dual-band continuous-wave (CW) results are shown in Fig. 26.5.4, where the LB achieves 28.9dBm peak power with 36.8% peak PAE, and the HB obtains 27.0dBm peak power with 25.4% peak PAE. The relatively flat output power is achieved over LB and HB, respectively, with the maximum power deviations of 0.3dB and 0.2dB within the frequency bands. Owing to the Doherty load, the PAE of 29.9% and 16.8% is achieved at 6dB PBO for 850MHz and 1.7GHz, respectively, showing the average efficiency enhancement.

In modulation tests, memoryless digital pre-distortion look-up tables are utilized to linearize the PA. With the 12-subcarrier NB-IoT signals, the PA output spectrum meets the stringent NB-IoT emission-mask requirements across both LB/HB bands, as demonstrated in Fig. 26.5.5. With -21.6dB EVM, the PA achieves the P_{avg} of 24.4dBm with average PAE of 29.5% at 850MHz, and the P_{avg} of 23.0dBm with average PAE of 17.9% at 1.7GHz. Moreover, this PA can be applied to wideband communication, such as WLAN and LTE. With 20MHz 64-QAM/256-QAM WLAN signals, the PA obtains 22.9dBm P_{avg}, 26.1% average PAE, -25.3dB EVM and 20.8dBm P_{avg}, 22.7% average PAE, -30.5dB EVM, respectively. The measured performance of proposed PA is summarized in Fig. 26.5.6 and compared with prior works. This work delivers a close-to-Watt-level peak output power and the best average PAE with on-chip matching at sub-GHz among results in Fig. 26.5.6. By using a parallel-combining-transformer power combiner, the dual-band frequency coverage, high output power, and backoff efficiency enhancement are simultaneously achieved with the smallest footprint, thus well-fitting low-cost NB-IoT applications.

Acknowledgements:
The authors would like to thank the State Key Laboratory of ASIC and System at Fudan University for measurement support.

References:
[1] Z. Song et al., "A Low-Power NB-IoT Transceiver with Digital-Polar Transmitter in 180-nm CMOS," *IEEE TCAS-I*, vol. 64, no. 9, pp. 2569-2581, Sept. 2017.
[2] J. Moreira et al., "A Single-Chip HSPA Transceiver with Fully Integrated 3G CMOS Power Amplifiers," *ISSCC*, pp. 162-163, Feb. 2015.
[3] J. Park et al., "A Highly Linear Dual-Band Mixed-Mode Polar Power Amplifier in CMOS with an Ultra-Compact Output Network," *IEEE JSSC*, vol. 51, no. 8, pp. 1756-1770, Aug. 2016.
[4] S. Hu et al., "Design of A Transformer-Based Reconfigurable Digital Polar Doherty Power Amplifier Fully Integrated in Bulk CMOS," *IEEE JSSC*, vol. 50, no. 5, pp. 1094-1106, May 2015.
[5] V. Vorapipat et al., "A Class-G Voltage-Mode Doherty Power Amplifier," *ISSCC*, pp. 46-47, Feb. 2017.
[6] H. Xu et al., "Systems and Methods for Combining Power through A Transformer," US Patent 9,306,503, Apr. 2016.

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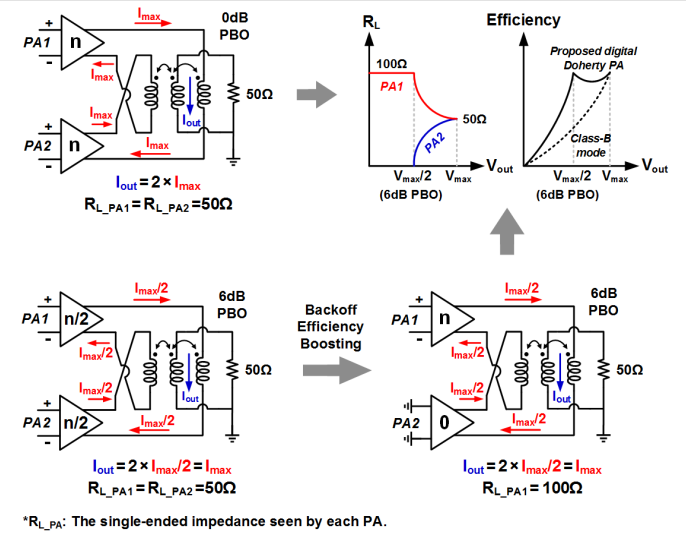

Figure 26.5.1: Digital Doherty PA operation at 0dB/6dB PBO using parallel combing transformer.

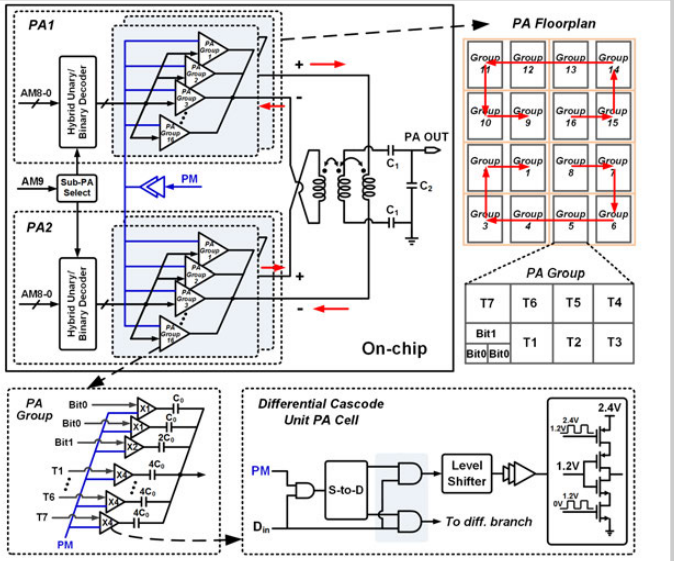

Figure 26.5.2: Block diagram of the proposed dual-band digital Doherty PA.

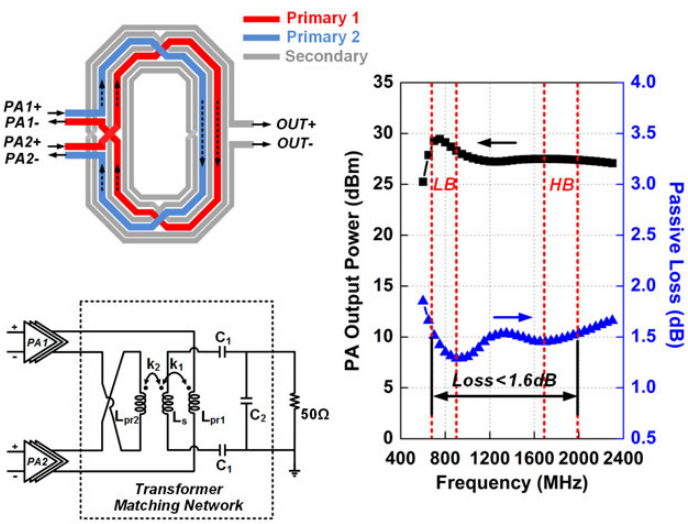

Figure 26.5.3: Implementation of dual-band passive matching network and its simulation results.

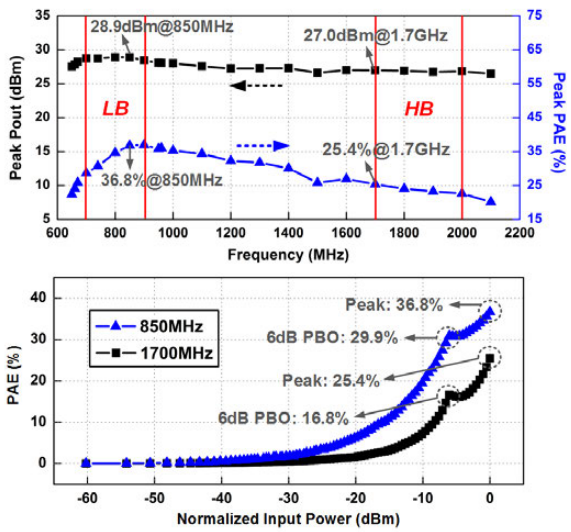

Figure 26.5.4: Measured dual-band CW results of output power, PAE and frequency response.

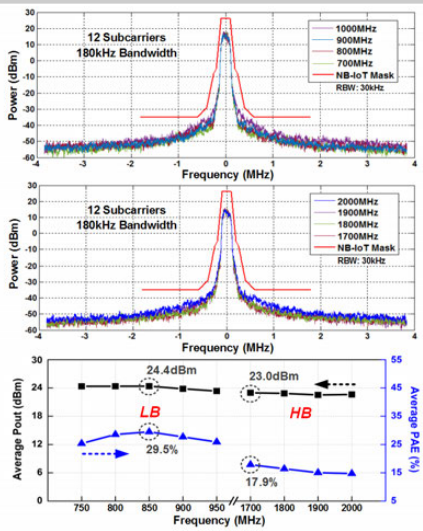

Figure 26.5.5: Measured PA NB-IoT output spectrums and its average P_{out} and PAE versus frequency.

	This work		TCAS-I 2017 [1]†	ISSCC 2015 [2]	JSSC 2016 [3]*	JSSC 2015 [4]*	ISSCC 2017 [5]*
Freq. (GHz)	0.85/1.7		0.891	0.95/1.95	2.6/4.5	3.82	3.5
On-chip Balun	Yes (1 transformer)		No (Off-chip matching)	Yes (2 transformer)	Yes (1 transformer)	Yes (2 transformer)	Yes (2 transformer)
Peak Pout (dBm)	28.9/27.0		23.2	32	28.1/26.0	27.3	25.3
Peak PAE (%)	36.8/25.4		44.5	-	35/21.2	32.5 (DE)	30.4
6dB PBO PAE (%)	29.9/16.8		-	-	-	22 (DE)**	25.3
Modulation	12 Subcarriers 180kHz NB-IoT	20MHz 64QAM/256QAM WLAN @LB	Single Carrier, 3.75kHz NB-IoT	HSPA	8MS/s 256QAM	500kS/s 16QAM	32 Carriers, 10MHz 256QAM
Pavg (dBm)	24.4/23.0	22.9/20.8	18.87	>26/>26	20.37/18.53	21.8	19.0
PAE (%)	29.5/17.9	26.1/22.7	33.4	23.7/23.8	16.26/13.42	22.1 (DE)	24.0
EVM (dB)	-21.6	-25.3/-30.5	-28.2	-26.6/-23.2	-36.3/-34.6	-25.0	-35.0
Supply (V)	1.2/2.4		2	3	1.5/3	1.2/3	1.2/2.4
Chip Size (mm²)	1.11		1.75	3‡	2.25	2.09	1.2
Technology	55nm CMOS		180nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	45nm CMOS SOI

†Results from the second prototype. ‡Estimated total area of RF DACs, LB PA and PA from chip micrograph.
*Results measured with GSG probe. **Estimated from Fig. 13 in [4].

Figure 26.5.6: Performance summary and comparison with prior works.

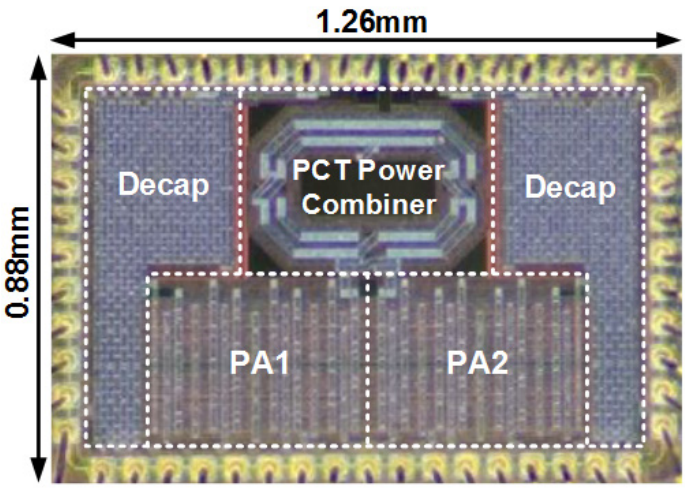

Figure 26.5.7: Die micrograph.

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26.6 A Continuous-Mode Harmonically Tuned 19-to-29.5GHz Ultra-Linear PA Supporting 18Gb/s at 18.4% Modulation PAE and 43.5% Peak PAE

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The 5th generation (5G) mm-wave systems are expected to support wideband spectrum-efficient modulations (e.g., 64-QAM or 256-QAM) to achieve Gb/s-link-throughput revolution. These complex modulation schemes, however, often come with high-density constellations that demand stringent linearity, i.e. AM-AM and AM-PM, on the mm-wave front-end circuits, in particular, the power amplifiers (PAs). In addition, to support future massive MIMOs, the mm-wave front-ends should be ultra-efficient in both their energy efficiency and area usage, posing even more constraints on the PA designs [1-5].

Practical mm-wave PAs, especially silicon-based PAs, always face a steep trade-off between the PA efficiency and linearity. Conventional linear PAs, e.g., Class-AB PAs, offer design simplicity and good linearity. However, their over-simplified output harmonic terminations often limit the peak efficiency. Millimeter-wave time-domain switching PAs, e.g., Class-E PAs, show high peak efficiency but poor linearity. They cannot support complex modulations without major digital pre-distortion (DPD) computations, which require substantial power and complexity at Gb/s speeds. An alternative is to use overdriven linear PAs with harmonic terminations. Multiple designs recently show that Class-J or Class-F/Class-F^{-1}-like harmonic terminations of linear PAs can boost their peak efficiency and still preserve high linearity. However, these designs either have limited bandwidth due to narrowband harmonic terminations or require area-consuming passive networks, constraining their use in broadband massive MIMO systems.

We propose a two-stage differential continuous-mode harmonically tuned ultra-linear mm-wave PA that achieves wideband operation (19 to 29.5GHz, 43.3%), high peak PAE (43.5%), high modulation PAE (18.4% for 3GSym/s 64-QAM and 16.3% for 1GSym/s 256-QAM), and high average output power P_{out} (9.8dBm for 3GSym/s 64-QAM and 8.7dBm for 1GSym/s 256-QAM). Our PA realizes an on-chip continuous-mode wideband harmonic-termination output network, simultaneously for the fundamental, 2nd-, and 3rd-order harmonics, with only one transformer footprint and no need for any tunable elements or switches, which achieves an ultra-compact PA design for broadband 5G massive MIMOs (Fig. 26.6.1).

Unlike conventional single-frequency-PA harmonic tuning, the continuous-mode PA substantially expands the frequency range over which the desired PA output harmonic terminations can be achieved for efficiency enhancement. However, most existing continuous-mode PA output networks require multiple passive components and transmission lines for multi-resonance tuning [6-8], inevitably increasing the network complexity, losses, and size. Our PA output network exploits and enhances parasitic elements in an on-chip transformer to achieve continuous-mode harmonic tuning at both differential- and common-mode with substantial network simplification and area-saving. It consists of one 1:1 transformer and three harmonic tuning capacitors ($2\times C_d$ and C_c). Also, it utilizes two symmetrically embedded branches L_d inside the transformer for the 3rd-order harmonic impedance tuning in differential-mode, and two extended branches L_{c1} and L_{c2} for the 2nd-order harmonic impedance tuning in common-mode (Fig. 26.6.1). The schematic of our PA and the EM model and the simplified circuits of the proposed PA output network are shown in Fig. 26.6.1. To ensure PA linearity, a harmonic trap network is added at the PA input to provide a low 2nd-order harmonic source impedance.

Next, the PA output harmonic termination network is explained. In Fig. 26.6.2, L_{dm1}/L_{cm1} and L_{dm2}/L_{cm2} are the differential-/common-mode half-circuit inductances of the transformer, and the output leads are absorbed into the transformer secondary coil. Also, L_{m1} and L_{k1} are the magnetizing and leakage inductances of the transformer in differential-mode half-circuit. In the differential mode, the center-tap of the transformer is virtual ground, so L_{c1}/L_{c2} and C_c do not affect the fundamental and 3rd-order harmonic termination. C_d-L_d-L_{dm2} form a multi-resonance tank Z_1 with high-frequency resonance. At the fundamental frequency, the series network C_d-L_d behaves as a small capacitor, which presents a high impedance to the transformer. The transformer performs its matching with the PA output capacitance C_{out} and provides the desired fundamental load impedance to the PA. At the 3rd-order harmonic, the series network C_d-L_d is slightly below their series resonance, which shorts out L_{dm2} and forms a series resonance of C_d-L_d-L_{m1}-L_{k1} to produce a desired low impedance. In the common-mode half-circuit, the network of $C_c/2$, $2L_{c1}$, and $2L_{c2}$ forms a multi-resonance tank Z_2. At the 2nd-order harmonic, Z_2 provides a high impedance, and the remaining series tank of C_d-L_d behaves as a capacitor. Therefore, with proper tuning, the 2nd-order harmonic impedance is dominated by C_{out}, L_{cm1} and the effective capacitance due to series C_d-L_d, which achieve desired continuous-mode 2nd-order harmonic impedance. The trajectories of half-circuit load impedance at fundamental, 2nd-, and 3rd-order harmonics with the PA output capacitance C_{out} are shown on the Smith Chart in Fig. 26.6.2.

The PA continuous-mode harmonic terminations are further explained (Fig. 26.6.2). The fundamental load impedance is mostly inductive for lower frequency ($0\leq\xi\leq1$) and capacitive for higher frequency ($-1\leq\xi\leq0$), and vice versa for the 2nd-order harmonic impedance. The fundamental and the 2nd-order harmonic impedances of the upper operation bandwidth follow the constant conductance circles, while the 3rd-order-harmonic impedance is kept low. These aspects verify that the PA achieves a continuous-mode Class-F^{-1}-like harmonic terminations for its fundamental, 2nd-, and 3rd-order impedances [6]. In addition, the harmonic trap and the inter-stage network together provide a low 2nd-order-harmonic source impedance for the PA to ensure its linearity.

Our proposed PA is implemented in a 0.13µm SiGe BiCMOS process with a $0.91\times0.32mm^2$ core area excluding pads, as shown in Fig. 26.6.7. The small-signal and the continuous-wave (CW) large-signal measurements are shown in Fig. 26.6.3. At 28.5GHz, it achieves P_{sat} of 17dBm and P_{1dB} of 15.2dBm, the power gain G_p of 20dB, peak PAE_{total} of 43.5%, and peak PAE_{PA} of 50%. For a fair comparison with reported 2-stage and 1-stage PAs, we use PAE_{total} to represent the overall PAE of the 2-stage PA including both the driver and PA output stage, while PAE_{PA} stands for the 1-stage PA PAE, i.e. the PA output stage only. The measured P_{sat} is 16.4 to 17.4dBm for 19 to 29.5GHz, achieving a 43.3% large-signal P_{out} 1dB bandwidth. Figure 26.6.3 also shows the AM-PM distortion of only 3° and the AM-AM gain peaking within 0.43dB up to P_{1dB} at 28.5GHz.

Our proposed PA is first measured using 64-QAM signals at 1GSym/s (6Gb/s), 1.5GSym/s (9Gb/s), 2.5GSym/s (15Gb/s), and 3GSym/s (18Gb/s) at the carrier frequency ($f_{carrier}$) of 28.5GHz, as shown in Fig. 26.6.4. With no DPD, the measured EVM is below <-25dB for all data rates. At 3GSym/s (18Gb/s), the EVM is –25dB with the average output power P_{avg} of 9.8dBm and PAE_{total} of 18.4%. Next, the PA is measured using 256-QAM signals at 0.5GSym/s (4Gb/s), 0.8GSym/s (6.4Gb/s), and 1GSym/s (8Gb/s) at carrier frequency ($f_{carrier}$) of 28.5GHz, as shown in Fig. 26.6.5. The EVM is kept below -30dB for all data rates. At 1GSym/s (8Gb/s), the EVM is –30dB with P_{avg} of 8.7dBm and PAE_{total} of 16.3%.

Compared with the reported silicon-based PAs at similar frequencies in Fig. 26.6.6, our proposed PA demonstrates the highest data rate (18Gb/s 64-QAM and 8Gb/s 256-QAM), the highest peak PAE (2-stage PAE_{total}=43.5% and 1-stage PAE_{PA}=50%), the highest modulation PAE (18.4% for 3GSym/s 64-QAM and 16.3% for 1GSym/s 256-QAM), and a wide P_{out} 1dB bandwidth (19 to 29.5GHz, 43.3%). The continuous-mode harmonically tuned output PA network only occupies one on-chip transformer footprint for an ultra-compact PA design.

Acknowledgements:
We thank GlobalFoundries for chip fabrication.

Reference:
[1] S. Hu et al., "A 28GHz/37GHz/39GHz Multiband Linear Doherty Power Amplifier for 5G Massive MIMO Applications," *ISSCC*, pp. 32-33, Feb. 2017.
[2] S. Shakib et al., "A Wideband 28GHz Power Amplifier Supporting 8×100MHz Carrier Aggregation for 5G in 40nm CMOS," *ISSCC*, pp. 44-45, Feb. 2017.
[3] P. Indirayanti and P. Reynaert, "A 32 GHz 20 dBm-PSAT Transformer-Based Doherty Power Amplifier for Multi-Gb/s 5G Applications in 28 nm bulk CMOS," *IEEE RFIC*, pp. 45-48, June 2017.
[4] M. Vigilante and P. Reynaert, "A 29-to-57GHz AM-PM Compensated Class-AB Power Amplifier for 5G Phased Arrays in 0.9V 28nm bulk CMOS," *IEEE RFIC*, pp. 116-119, June 2017.
[5] B. Park et al., "Highly Linear mm-Wave CMOS Power Amplifier," *IEEE TMTT*, vol. 64, no. 12, pp. 4535-4544, Dec. 2016.
[6] V. Carrubba et al., "On the Extension of the Continuous Class-F Mode Power Amplifier," *IEEE TMTT*, vol. 59, no. 5, pp. 1294-1303, May 2011.
[7] K. Chen and D. Peroulis, "Design of Broadband Highly Efficient Harmonic-Tuned Power Amplifier Using In-Band Continuous Class-F^{-1}/F Mode Transferring," *IEEE TMTT*, vol. 60, no. 12, pp. 4107-4116, Dec. 2012.
[8] S. Ali et al., "A 42–46.4% PAE Continuous Class-F Power Amplifier with Cgd Neutralization at 26–34 GHz in 65nm CMOS for 5G Applications," *IEEE RFIC*, pp. 212–215, June 2017.

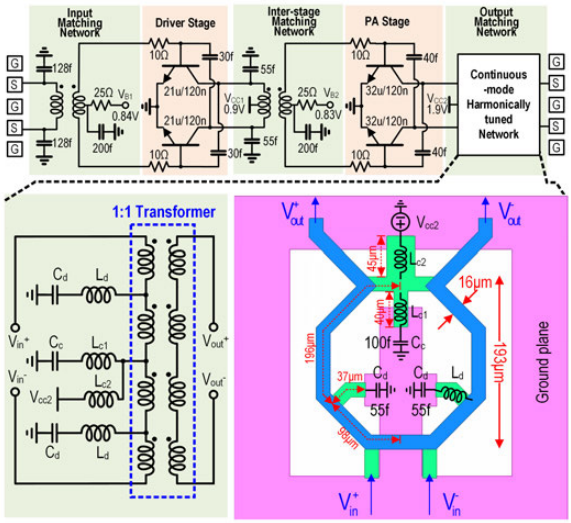

Figure 26.6.1: The schematic of the proposed PA and the continuous-mode harmonically tuned output matching network.

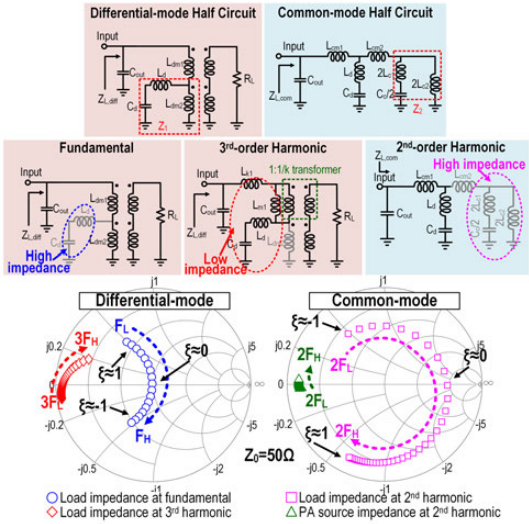

Figure 26.6.2: The simplified differential-/common-mode half circuits of the output network, and the load impedance trajectories.

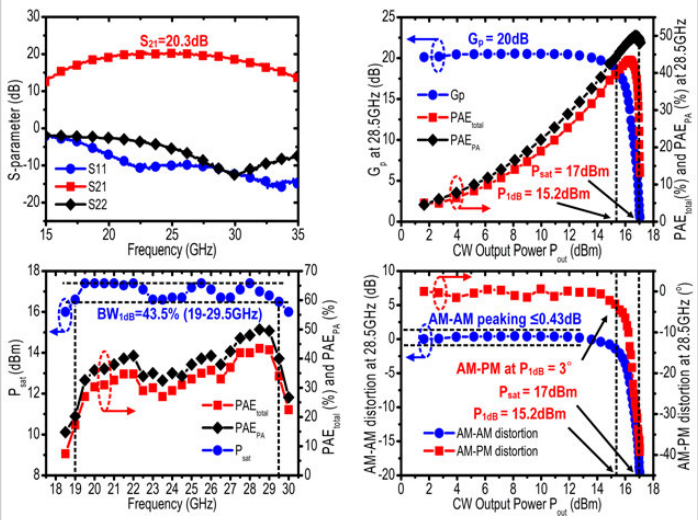

Figure 26.6.3: The measured S-parameters and the CW large-signal performance vs. output power and carrier frequency.

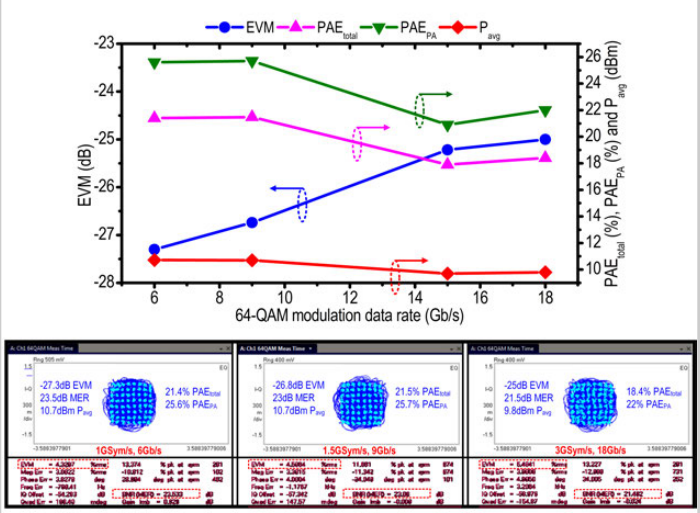

Figure 26.6.4: The 64-QAM modulation measurement results ($f_{carrier}$=28.5GHz) at 1GSym/s, 1.5GSym/s and 3GSym/s.

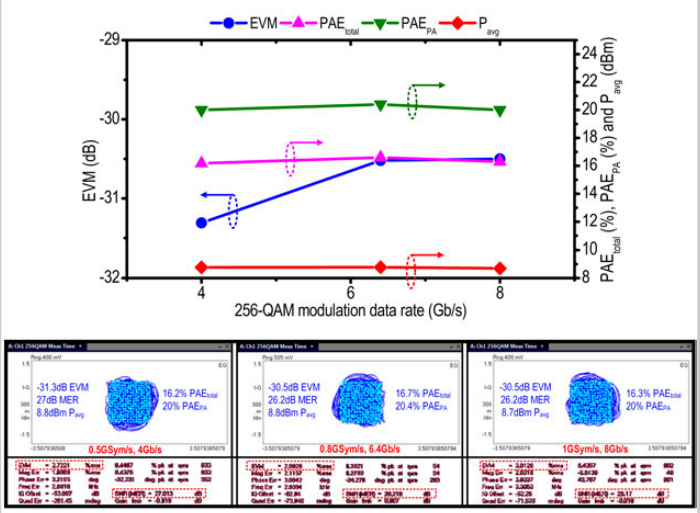

Figure 26.6.5: The 256-QAM modulation measurement results ($f_{carrier}$=28.5GHz) at 0.5GSym/s, 0.8GSym/s and 1GSym/s.

	This work			[8] RFIC 17	Sarkar T-MTT 17	[2] ISSCC 17	[1] ISSCC 17	[5] T-MTT16	[3] RFIC 17	[4] RFIC 17
Technology	130nm SiGe			65nm CMOS	130nm SiGe	40nm CMOS	130nm SiGe	28nm CMOS	28nm CMOS	28nm CMOS
PA supply (V)	1.9			1.1	3.6	1.1	1.5	2.2	1	0.9
P_{out} 1dB Frequency (GHz)	19-29.5			26-34	27-29	27-30#	28-42	26.5-29#	28-33#	25-48#
P_{out} 1dB Bandwidth	43.3%			26.7%	7.1%	10.5%#	40%	10.7%#	22.2%#	63%#
Gain (dB)	20			10	15.5	22.4	18.2	13.6	22	20.8
P_{sat} (dBm)	17			14.8	18.8	15.1	16.8	19.8	19.8	16.6
P_{1dB} (dBm)	15.2			13.2	15.9	13.7	15.1	18.6	16	13.4
PAE_{total} (%)* (2-stage PA)	43.5			-	-	33.7	22.6	-	21	24.2
PAE_{PA} (%)** (1-stage PA)	50			46.4	35.3	-	-	43.3	-	-
PAE_{total}@P_{1dB} (%)	39.2			-	-	31.1	21.6	-	12.8	12.6
PAE_{PA}@P_{1dB} (%)	43			39#	31.5	-	-	41.4	-	-
Modulation scheme	64-QAM		256-QAM	-	16-QAM OFDM	64-QAM OFDM	64-QAM	64-QAM WLAN	64-QAM	64-QAM
Data rate (Gb/s)	6 9 18	4 6.4 8		-	3.2	4.8	6	0.48	15	6
EVM (dB)	-27.6 -26.8 -25	-31.3 -30.5 -30.5		-	-22	-25	-26.6	-27.5	-25	-25
P_{out}@EVM (dBm)	10.7 10.7 9.8	8.8 8.8 8.7		-	-	6.7	7.2	10.97	11.7	5.9
PAE_{total}@EVM (%)	21.4 21.5 18.4	16.2 16.7 16.3		-	-	11	7.5#	17.3	5.75	2.3
PA core size (mm²)	0.29			0.12	0.27	0.23	1.76	0.28	0.59	0.16
Topology	Differential 2-stage Continuous-mode Harmonically-tuned			Single-ended 1-stage Continuous-mode Class-F	Single-ended 1-stage Cascode Continuous-mode Class-AB	Single-ended 3-stage Class-AB	Single-ended 2-stage Doherty	Single-ended 1-stage 2-stacked Harmonically-tuned Class-AB	Single-ended 2-stage Doherty	Single-ended 2-stage Class-AB with Output Power Combiner

*PAE_{total} includes the DC power consumption of both driver and PA stage
**PAE_{PA} includes the DC power consumption of the output PA stage only
#Graphically estimated from reported figures

Figure 26.6.6: The comparison table of silicon-based mm-wave PAs at related operation frequencies.

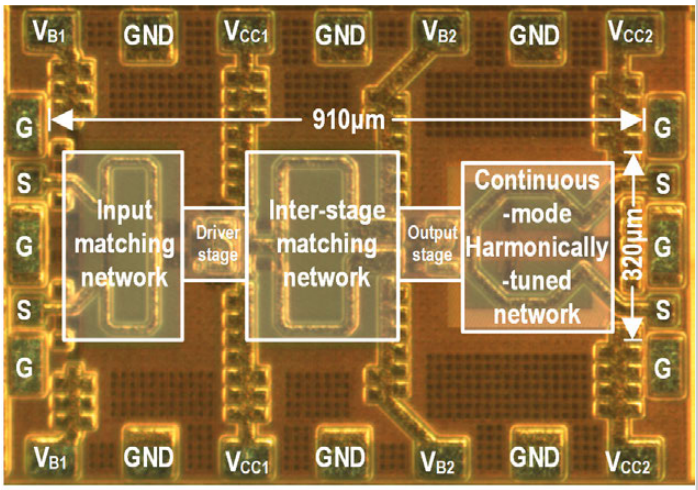

Figure 26.6.7: The PA die micrograph.

978-1-5090-4940-0/18/$31.00

26.7 A Coupled-RTWO-Based Subharmonic Receiver Front-End for 5G E-Band Backhaul Links in 28nm Bulk CMOS

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A fully integrated receiver for high-capacity 5G E-Band Backhaul links (71 to 76GHz and 81 to 86GHz) needs a local-oscillator (LO) distribution network with >19% tuning range (TR) and accurate quadrature phases. Further, the LO phase noise (PN) at 10MHz offset should be as low as -119dBc/Hz to impair the SNR of the received 64-QAM signal by <1dB at 10^{-6} BER [1]. Silicon-based solutions reported so far either do not meet such stringent requirements [1-4] or demand large power consumption in the LO distribution network [5].

We propose a direct-conversion I/Q subharmonic-receiver (SHRX) architecture that leverages on-chip coupled rotary traveling-wave oscillators (RTWOs) to generate N=8 differential phases at $f_{LO}=2f_{RF}/N$, a quadrature-correction circuit to realize accurate I/Q phases, and current-mode passive mixers (MXs) to allow low-V_{DD} operation and to greatly simplify the layout. The subharmonic architecture is well known and provides several benefits. (1) The oscillators enjoy superior FOM for given PN and TR [1-6]. (2) The RTWOs are able to directly drive the MXs reducing the LO distribution network to bare minimum, further saving power consumption [6]. (3) There is no need for image-rejection filters and IF gain stages [5,6]. (4) Typical key limitations of direct conversion TRXs, such as LO feedthrough and PA pulling, are greatly mitigated [2,6].

Despite the aforementioned advantages, no mm-wave SHRX implementation with sufficient performance was found to date in open literature, with the remarkable exception of [6]. In [6], half-harmonic operation (i.e. $f_{LO}=f_{RF}/2$) at 24GHz is reported by leveraging a double quadrature lumped-element LC VCO. In this work, we demonstrate that 8 differential phases can be effectively generated by distributed oscillators, while circuit and layout techniques are studied to achieve superior phase accuracy. Implemented in a 28nm bulk CMOS technology without an ultra-thick top-metal option, the realized prototype SHRX front-end achieves quarter-harmonic operation (i.e. $f_{LO}=f_{RF}/4$) in the E-Band and exhibits low PN and FOM and wide TR. The measured minimum noise figure (NF) is 8.3dB and varies less than 2dB over the 12.5GHz 3dB RF bandwidth.

Figure 26.7.1 shows the simplified schematic and the layout implementation of the proposed coupled RTWOs and SHMXs. Two RTWOs are coupled to achieve 3dB lower PN with negligible FOM penalty [1], while generating the required N=8 differential phases. The MXs are conveniently laid out inside the transmission-line (TL) ring, maximizing symmetry and minimizing the length of the LO interconnections, key features to ensure phase accuracy and low power consumption. The conversion gain (CG) of a SHMX degrades in presence of phase error (φ_{err}), and the larger N the larger the degradation. It can be shown that when $\varphi_{err}=8°$ is considered, the CG reduces by ≈0.08dB for N=4 and ≈0.94dB for N=8 (worst case scenario). The RTWOs are designed with 16 stages (see Fig. 26.7.1). Each stage employs a back-to-back inverter negative G_m (W_N=4×1.06µm, W_P=6×1.06µm, L=28nm), a 6b MOM capacitor bank, a small A-MOS varactor for continuous tuning, and a small A-MOS varactor for I/Q phase error compensation as first proposed in [7] for LC quadrature VCOs. Benefited by the 4× lower frequency of operation, (1) the capacitive part of the TL losses is reduced and (2) a larger number of stages can be laid out in the RTWO ring. This permits the circuit to impose an almost square voltage waveform at 20GHz, further improving the CG of the MX. It is worth mentioning that the RTWOs should be coupled with differential connections at least in two points (as in Fig. 26.7.1) to avoid mode ambiguity and ensure proper quadrature operation.

The 4-stage LNA in Fig. 26.7.2 provides ≈30dB gain to compensate for the losses of the SHMXs. Neutralized common-source (CS) amplifiers are used as transconductance stage in the RF signal path ($W_{CS,deg}$=40×1.06µm, W_{CS}=24×1.06µm, L=28nm), providing high gain and excellent reverse isolation at mm-wave [2,8]. An inductor is added at the source of the 1st stage of the LNA to lower its input impedance and realize broadband matching to 50Ω [6]. Transformer based 4th-order filters are largely employed to serve as a balun and ESD protection at the LNA input [2] and for gain-bandwidth enhancement and power division in the inter-stage matching networks [8].

The BB current at the SHMX output (W_{MX}=24×1.06µm, L=28nm) is converted to a voltage by a TIA (Fig. 26.7.2). The TIA provides ≈56Ω input impedance and is followed by a buffer to drive the 50Ω measurement equipment. For testing purposes frequency divide-by-4 and divide-by-16 are also implemented on-chip, and the RTWOs can be locked by an off-chip PLL.

The SHRX with integrated RTWOs was realized in a 28nm bulk CMOS process (Fig. 26.7.7). The core area is 1760µm×620µm. Figure 26.7.3 shows the measured DC power consumption of the coupled RTWOs and the power breakdown between the blocks. The RTWOs run at $f_{LO}=f_{RF}/4$ and draw 67.4mA and 57.7mA from a 1.3V supply at the lowest and highest oscillation frequency, respectively. $P_{DC,RTWOs}$ decreases almost linearly with frequency. The transconductance stages in the RF path and the BB TIAs consume 69.8mA and 16.1mA from a 0.9V supply, respectively. Benefited by the proposed architecture, the total power consumption of the LO generation and distribution network never exceeds the 53% of the full system. The oscillators are tunable from 16.1 to 19.8GHz, corresponding to 20.5% TR. The center frequency is ≈1.8GHz lower than expected due to an underestimation of the layout parasitics during the design phase. The PN is measured at the frequency divide-by-4 output and reported to the carrier, assuming negligible phase-noise degradation from the divider. Figure 26.7.4 shows the measured PN and FOM of the free-running coupled RTWOs at 10MHz offset from the carrier against the oscillation frequency. The PN ranges from -131.2 to -132.8dBc/Hz (1.6dB variation) over the TR, with a corresponding FOM from -176.7 to -179.5dBc/Hz. The measured and simulated $|S_{11}|$, CG, and NF are reported in Fig. 26.7.5. The input power match is better than -9.3dB from 65.7 to 99GHz, the CG is 28dB over a 12.5GHz BW_{3dB} limited by the on-chip LO TR. The NF, measured with a SAGE STZ-12-I1 E-Band noise source and an R&S spectrum analyzer, reaches a minimum of 8.3dB and varies less than 2dB over the RF BW_{3dB}. The measured I/Q mismatch shown in Fig. 26.7.5 is <7.1° over the TR and can be made negligible by the discussed on-chip phase-correction circuitry. By varying $V_{cor,I}$ from 0 to 1.1V and $V_{cor,Q}$ (in Fig. 26.7.1) from 1.1 to 0V, the I/Q phases can be corrected by ±7.5° to ±9.3° at the lowest and highest oscillation frequency respectively. The effect of the phase correction on the measured PN at 10MHz offset is <1dB. Figure 26.7.5 reports also the large signal CW measurements at 81.4GHz, showing an ICP_{1dB} of -25dBm.

Experimental results are summarized and compared to recently published E-Band RXs in Fig. 26.7.6. The proposed coupled-RTWO-based SHRX significantly advances the state-of-the-art of the CMOS designs in Fig. 26.7.6 in terms of PN, TR, and FOM. Relative to the 0.13µm SiGe solution in [5], this work achieves comparable PN and TR, while saving >4.6× power in the LO path. Moreover, the proposed SHRX achieves state-of-the-art NF and linearity, while reporting the widest RF BW_{3dB} among the designs in the comparison table. In summary, this work proves the viability of fully integrated coupled-RTWO-based subharmonic RXs for high-capacity 5G E-Band backhaul links.

Acknowledgements:
This work was supported by Analog Devices Inc, Limerick, Ireland. The authors wish to thank Mike Keaveney, Mike O'Shea, Niall McDermott and Andrew Cunnane from Analog Devices for providing technology access and support with measurements.

References:

[1] L. Iotti et al., "Insights into Phase-Noise Scaling in Switch-Coupled Multi-Core VCOs for E-Band Adaptive Modulation Links," *IEEE JSSC*, vol. 52, no. 7, pp. 1703-1718, July 2017.

[2] D. Guermandi et al., "A 79 GHz 2 × 2 MIMO PMCW Radar SoC in 28 nm CMOS," *IEEE JSSC*, vol. 52, no. 10, pp. 2613-2626, Oct. 2017.

[3] D. Guermandi et al., "A 79GHz binary phase-modulated continuous-wave radar transceiver with TX-to-RX spillover cancellation in 28nm CMOS," *ISSCC*, pp. 354-355, Feb. 2015.

[4] T. Fujibayashi et al., "A 76- to 81-GHz Multi-Channel Radar Transceiver," *IEEE JSSC*, vol. 52, no. 9, pp. 2226-2241, Sept. 2017.

[5] R. Levinger et al., "High-Performance E-Band Transceiver Chipset for Point-to-Point Communication in SiGe BiCMOS Technology," *IEEE TMTT*, vol. 64, no. 4, pp. 1078-1087, Apr. 2016.

[6] A. Mazzanti et al., "A 24GHz Sub-Harmonic Receiver Front-End with Integrated Multi-Phase LO Generation in 65nm CMOS," *ISSCC*, pp. 216-608, Feb. 2008.

[7] V. Szortyka et al., "A 42 mW 200 fs-Jitter 60 GHz Sub-Sampling PLL in 40 nm CMOS," *IEEE JSSC*, vol. 50, no. 9, pp. 2025-2036, Sept. 2015.

[8] M. Vigilante and P. Reynaert, "A 68.1-to-96.4GHz Variable-Gain Low-Noise Amplifier in 28nm CMOS," *ISSCC*, pp. 360-362, Feb. 2016.

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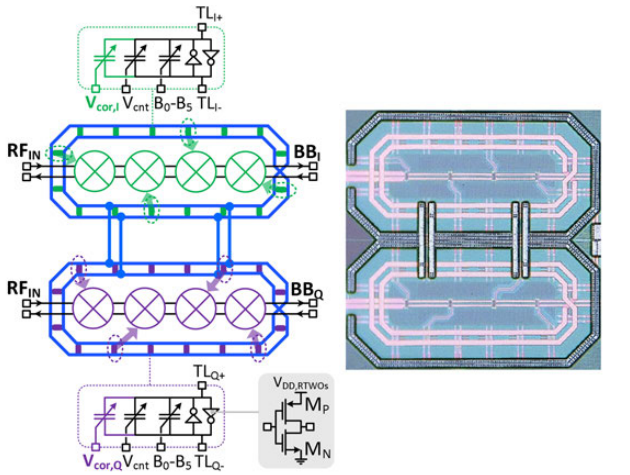

Figure 26.7.1: Simplified schematic of the coupled RTWOs and subharmonic mixers, with highlighted number of stages, tuning elements, and proposed I/Q phase-correction circuits (left). Layout details of the 28nm CMOS implementation (right).

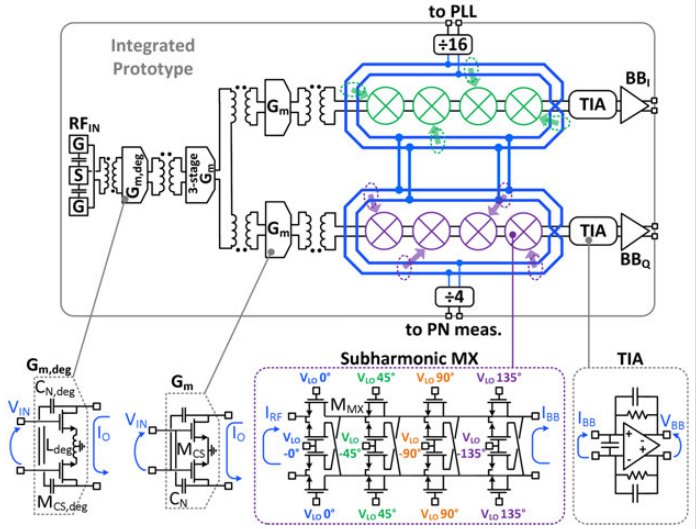

Figure 26.7.2: Simplified block diagram of the integrated coupled-RTWO-based subharmonic receiver.

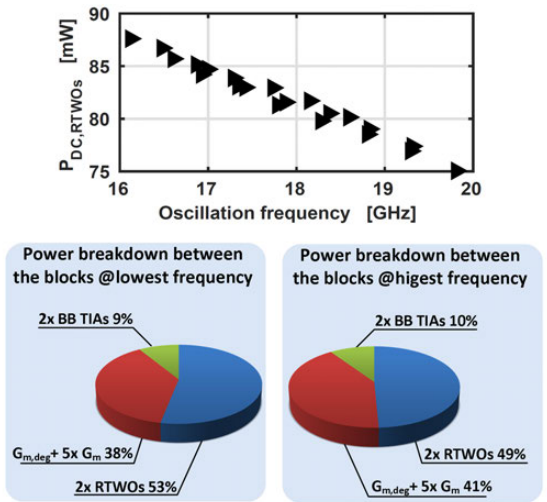

Figure 26.7.3: Measured DC power consumption of the coupled RTWOs (top) and measured power breakdown between the blocks at the tuning range edges (bottom).

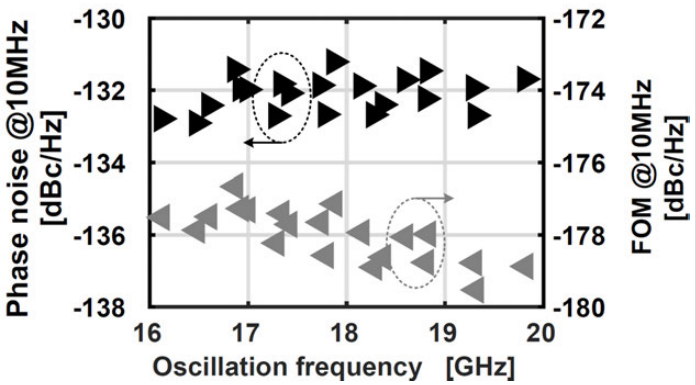

Figure 26.7.4: Measured phase noise (black triangles) and the figure of merit (gray triangles) at 10MHz offset from the carrier versus the oscillation frequency of the free-running coupled RTWOs. Benefited by the subharmonic architecture the RTWOs oscillate at $f_{LO}=f_{RF}/4$.

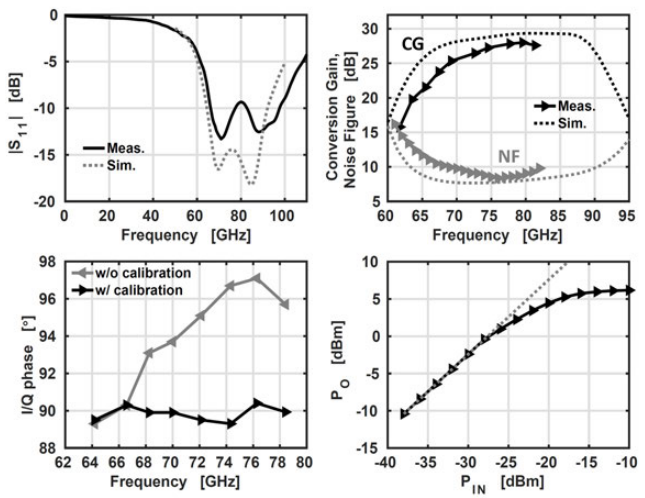

Figure 26.7.5: Measured input power match, conversion gain, noise figure, I/Q phase versus frequency, and measured output power (P_O) versus input power (P_{IN}) at 81.4GHz.

Reference	This work	Guermandi JSSC17 [2]	Guermandi ISSCC15 [3]	Fujibayashi JSSC17 [4]	Levinger TMTT16 [5]	
Technology	28nm CMOS	28nm CMOS	28nm CMOS	0.13μm SiGe	0.13μm SiGe	
Architecture	Subharmonic Direct Conversion 2 Coupled RTWOs	Direct Conversion VCO + SH-QILO5	Direct Conversion SH-QILO5	Direct Conversion VCO + Quadrupler + Hybrid Coupler	Sliding-IF VCO + Quadrupler + Divide-by-2	
f_c [GHz]	75.1	82.5	79	78.5	73	83
Gain [dB]	28	31	35	15	70	70
RF-BW	12.5GHz* (16.7%*)	9GHz (10.9%)	8GHz (10.1%)	7GHz (9%)	5GHz (6.9%)	5GHz (6%)
NF [dB]	8.3-10	12#	6.2-7	7-8	6-7	6-7
ICP_{1dB} [dBm]	-25	-28	-32.5	1	-19.6*	-21.6*
RX P_{DC} [mW]	77.3	68	59	197.5	222	222
On-chip LO?	YES	YES	NO	YES	YES	
LO freq. [GHz]	16.1-19.8	78-87	NA	74-82.4	15.6-19.3	
LO TR [%]	20.5	11	NA	12	21.2	
LO P_{DC} [mW]	87.6-75	100	NA	NA	405^	
PN @10MHz [dBc/Hz]	-131.2/-132.8 (-119.1/-120.7)ᵛ	-116	NA	-119/-120**	-133 (-120)ᵛ	
LO FOM [dBc/Hz]	-176.7/-179.5	-174.3	NA	NA	-171.5^	

*Limited by on-chip LO TR #Including flip chip assembly and module loss *Estimated from reported IIP3
^DC power consumption of the LO frequency divide-by-2 not included **Estimated from the reported PN @1MHz offset ᵛEquivalent @f_{RF}

Figure 26.7.6: Performance summary and comparison with prior works. Designs implemented in bulk CMOS technology are highlighted.

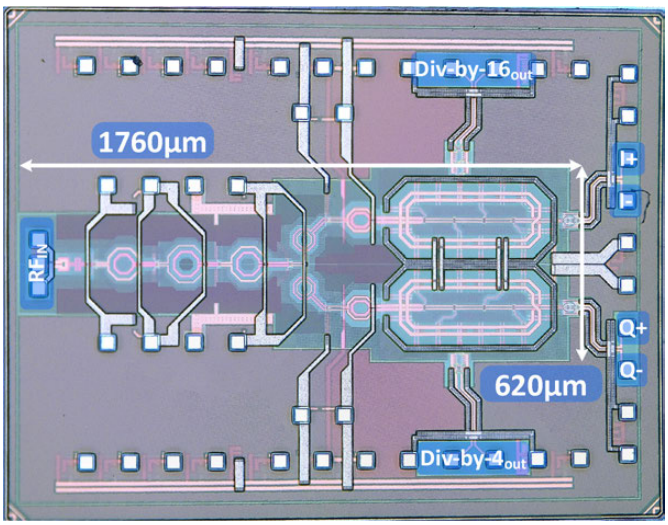

Figure 26.7.7: Die micrograph. The core area is 1760µm × 620µm. The total area is 1950µm × 1500µm.

978-1-5090-4940-0/18/$31.00

26.8 A 12mW 70-to-100GHz Mixer-First Receiver Front-End for mm-Wave Massive-MIMO Arrays in 28nm CMOS

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Multi-user multiple-input multiple-output (MIMO) systems are promising enablers for high-capacity wireless access in next-generation mobile networks. Leveraging antenna arrays at the access point, narrow beams can be steered to different users simultaneously, enhancing spectral efficiency through spatial multiplexing. By employing a number of array elements, M, much larger than the number of users, K, (i.e. massive MIMO), simple linear beamforming algorithms can achieve nearly optimal operation [1]. Operating massive MIMO systems at mm-waves results in compact antenna arrays and wide channel bandwidths. Within the available spectrum, the E-Band communication bandwidth (71 to 76GHz, 81 to 86GHz, and 92 to 95GHz) has recently gained attention for both access and wireless backhaul, due to low oxygen attenuation.

Hardware implementation of mm-wave massive MIMO systems poses several challenges and opportunities. On one hand, array gains allow one to relax the performance of the individual transceiver element, e.g., RX noise figure (NF) and TX power [1]. On the other hand, per-element area and power consumption have to be minimized. RF-signal and local-oscillator (LO) phase shifting and combining are popular in single-beam mm-wave phased arrays [2]. However, in a multi-beam system M×K mm-wave phase shifters would be required, resulting in significant area and power overhead. A baseband-combining architecture, as shown in Fig. 26.8.1, is hence more suitable for massive MIMO receivers, as compact analog or digital Cartesian beamformers can be employed [2]. As a drawback, since spatial filtering is performed after the RX front-end, high linearity is required to cope with interferers.

In this paper, we propose an E-Band mixer-first RX front-end, minimizing area and power consumption without sacrificing linearity and bandwidth. Most wideband mm-wave receivers employ magnetically or capacitively coupled multi-stage LNAs [3]. However, compensating losses in interstage networks requires significant power consumption. Since power reduction, rather than noise-figure minimization, is key in massive MIMO front-ends, a mixer-first receiver can be adopted instead. A 60GHz passive mixer presented in [4] achieves >30% power-matching bandwidth and 11-to-14dB NF. However, it employs wide MOS transistors (i.e. 64µm/60nm) for ideal-switch operation. At mm-waves, these require significant LO power to be driven, thus lowering the transceiver power efficiency. In [5], a low-power 5GHz mixer-first receiver is proposed, featuring small mixer switches that present a high input impedance and are matched to the antenna through a 1-to-6 transformer. The input matching network provides passive voltage gain, resulting in moderate noise figure (~5.3dB) in spite of high mixer series resistance. Unfortunately, high-turn-ratio transformers cannot be implemented at mm-waves due to low-frequency self-resonance.

The proposed RX front-end is shown in Fig. 26.8.2. A passive quadrature downconverter is followed by open-loop differential baseband amplifiers. Neglecting the mixer input capacitance, the input impedance of a capacitively loaded passive mixer ($Z_{IN,MIX}$) has a peak centered around the LO frequency (f_{LO}), whose bandwidth is set by the mixer load capacitance. The in-band impedance is proportional to the mixer-switch series resistance [5]. In the proposed mixer, small switches (6µm/30nm) are employed, resulting in ~400Ω in-band $Z_{IN,MIX}$ when the mixer is driven by a $600mV_{diff,0\text{-}pk}$ sinusoidal 80GHz quadrature LO. Matching this impedance to 50Ω would require a high-Q passive network, preventing wideband operation. Hence, frequency-translational feedback is employed to reduce $Z_{IN,MIX}$. Auxiliary feedback mixers are placed between the baseband amplifier output and the mixer input. Feedback switches are sized to obtain loop gain $G_{LOOP}\approx1$, resulting in $Z_{IN,MIX}$ being decreased by a factor of two within the loop bandwidth, as shown in Fig. 26.8.2. Since the baseband amplifier contributes to G_{LOOP}, the feedback switches can be considerably downsized compared to the mixer, hence contributing to only ~10% capacitance overhead. Since $G_{LOOP}\approx1$, the feedback does not lead to stability concerns.

The remaining input-impedance matching is performed by a wideband transformation network, combining an L-match and an input shunt resonator, as shown in Fig. 26.8.2. The input resonator not only neutralizes the pad capacitance, but also improves the matching bandwidth. DC bias and ESD protection are placed on the negative terminal of the shunt inductance, which is AC shorted to ground. The network provides ~6dB passive voltage gain, hence amplifying the signal before it enters the noisy passive mixer. Simulated RX noise figure is ~8dB, 3dB higher than [5] due to higher losses at mm-waves, unavailability of a 25% duty cycle LO, and ~1dB noise penalty due to the feedback. The baseband amplifier is designed to provide 13dB gain with 2mA current consumption. Gate-drain neutralization is employed to reduce the input capacitance, so that the dominant pole is located at the amplifier output.

Neutralized differential LO buffers with resonant loads, shown in Fig. 26.8.3, were co-designed with the mixer to provide 7dB maximum gain. Given the small mixer size, the buffer load impedance magnitude is ~500Ω, resulting in only 2mA nominal current consumption for each buffer. An LC series trap, tuned at ~85GHz, and a choke inductor were added to improve common-mode rejection at f_{LO}. A differential transformer-coupled quadrature hybrid is employed to generate the quadrature LO.

A prototype was realized in 28nm CMOS without ultra-thick metal (see Fig. 26.8.7). The RX core area, including input pad, LO buffers, and quadrature hybrid, is only $0.085mm^2$. The front-end is followed by a VGA and a matched output buffer for measurement purposes. The die was wire-bonded to a PCB, and high-frequency probes were used for the RF and LO pads. The LO was generated off-chip, and a constant $300mV_{diff,0\text{-}pk}$ swing was provided at the LO buffer input. Figure 26.8.4 shows measured S_{11} for different values of f_{LO}. Wideband power matching with S_{11}<-10dB over 74 to 94GHz is achieved, and the bandwidth is improved to 70 to 100GHz when the LO buffer current is increased to 4 mA to compensate losses at the edge of the buffer bandwidth.

NF, conversion gain, and input-referred 1dB compression point (ICP1dB) at 100MHz offset from f_{LO} are shown in Fig. 26.8.5. Gain and ICP1dB were measured using a frequency-translational VNA, whereas a W-Band noise source and a spectrum analyzer were used to evaluate NF with the Y-factor method. The RX front-end achieves 19.5 to 25.3dB voltage gain and 8 to 12.7dB NF over a wide operation range, ultimately limited by the LO chain bandwidth. Conversion gain increases at high frequency due to a rise in the matching-network voltage gain. Linearity gets worse at the bandwidth edges, since the reduced LO swing results in soft switching in the mixer. The baseband bandwidth is 1.8GHz, when driving a 100fF differential load. The flicker noise corner, set by the baseband amplifier, is at 10MHz.

Measurement results are compared to low-power CMOS mm-wave receivers in Fig. 26.8.6. The proposed receiver covers the licensed E-Band communication spectrum with -24dBm worst-case ICP1dB, 9.5dB worst-case NF, and only 12mW power consumption including the LO buffers. Ultra-low-power operation and small footprint, together with linearity comparable with prior works in Fig. 26.8.6, suggest the use of the proposed front-end for massive MIMO mm-wave arrays.

Acknowledgements:
This work was partly funded by the Intel Connectivity SRS program and the NSF EARS program (grant #1642920). The authors acknowledge the TSMC University Shuttle program for chip fabrication, Keysight Technologies for measurement support, and Integrand EMX for electromagnetic simulation. Thanks to Dr. Christopher Hull and Dr. Steven Callender from Intel Labs for the fruitful discussions, Suren Singh from Keysight for assistance during measurements, Prof. Francesco Svelto from University of Pavia for supporting the project, and Berkeley Wireless Research Center faculty, students, staff and sponsors.

References:
[1] E. Larsson et al., "Massive MIMO for Next Generation Wireless Systems," *IEEE Commun. Mag.*, vol. 52, no. 2, pp. 186-195, Feb. 2014.
[2] S. Kundu and J. Paramesh, "A Compact, Supply-Voltage Scalable 45–66 GHz Baseband-Combining CMOS Phased-Array Receiver," *IEEE JSSC*, vol. 50, no. 2, pp. 527-542, Feb. 2015.
[3] M. Vigilante and P. Reynaert, "On the Design of Wideband Transformer-Based Fourth Order Matching Networks for E-Band Receivers in 28-nm CMOS," IEEE JSSC, vol. 52, no. 8, pp. 2071-2082, Aug. 2017.
[4] A. Moroni and D. Manstretta, "A Broadband Millimeter-Wave Passive CMOS Down-Converter," *IEEE RFIC*, pp. 507-510, June 2010
[5] A. Homayoun and B. Razavi, "A Low-Power CMOS Receiver for 5 GHz WLAN," *IEEE JSSC*, vol. 50, no. 3, pp. 630-643, Mar. 2015.
[6] M. Khanpour et al., "A Wideband W-Band Receiver Front-End in 65-nm CMOS," *IEEE JSSC*, vol. 43, no. 8, pp. 1717-1730, Aug. 2008.

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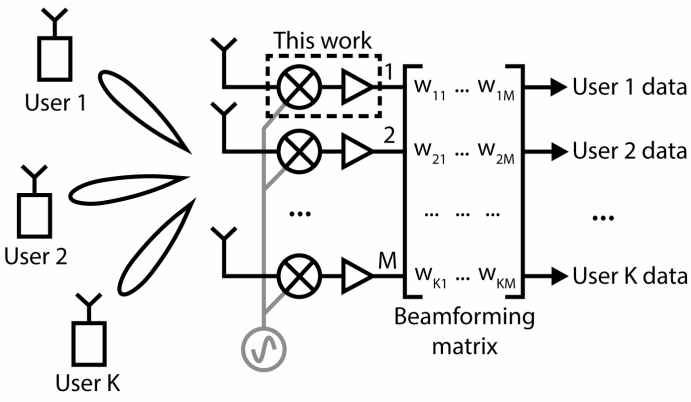

Figure 26.8.1: Multi-user MIMO receiver architecture with baseband signal combining.

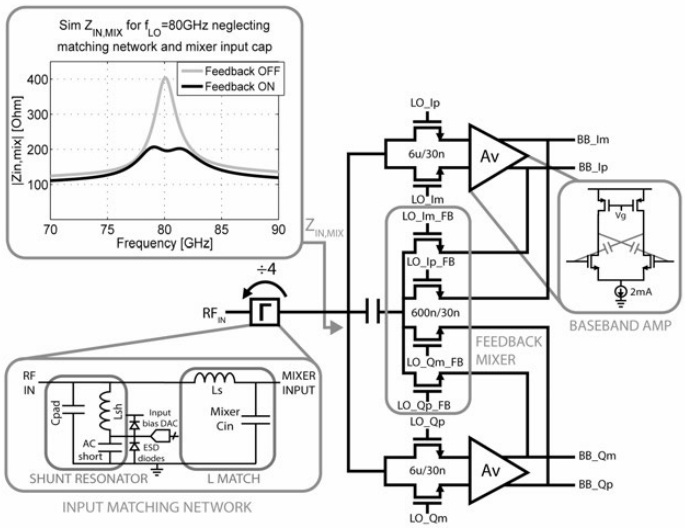

Figure 26.8.2: Receiver schematic and simulated mixer input impedance.

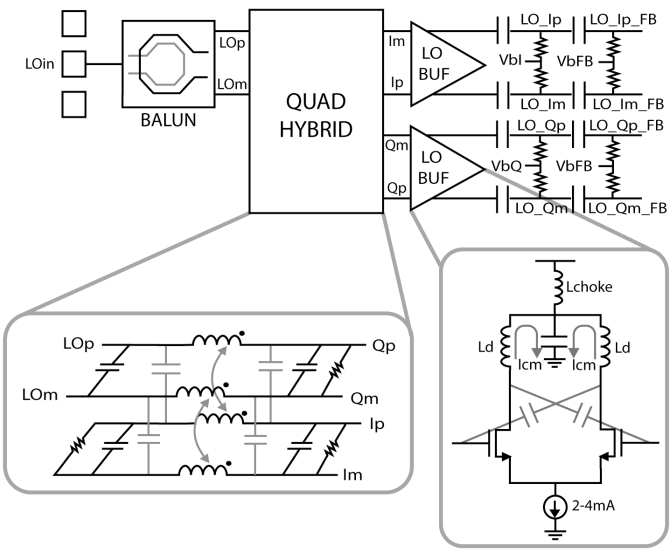

Figure 26.8.3: LO distribution chain.

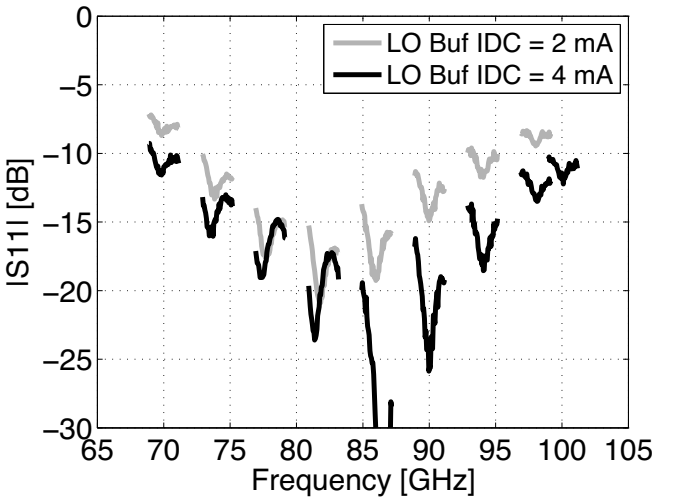

Figure 26.8.4: Measured S_{11} magnitude when sweeping the RF frequency within ±1GHz around the LO frequency.

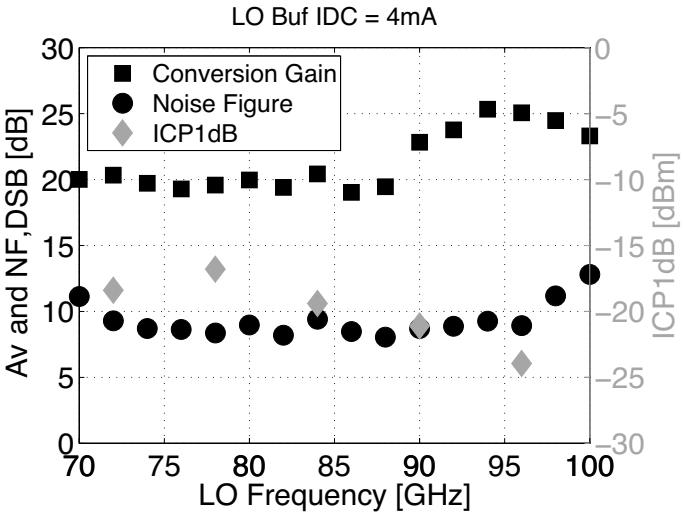

Figure 26.8.5: Measured DSB noise figure, conversion voltage gain, and input-referred 1dB compression point at 100MHz offset for different values of f_{LO}.

	This work		[3]		[6]	[2]		[4]
Technology	28nm CMOS		28nm CMOS		65nm CMOS	45nm CMOS SOI		65nm CMOS
Architecture	Mixer-first direct conv		Sliding IF heterodyne		Direct conv	Direct conversion		Mixer-first direct conv
Vdd [V]	1		0.9		1.8	0.6	1.1	1.2
Center freq [GHz]	84	85	75		83	55		58
Fractional RF BW	26.5%	35.3%	36.7%		19%	38%		>31%
Baseband BW [GHz]	1.8	1.8	N/A	N/A	9	1.2		0.32
Av (lowest) [dB]	21	19.5	//	//	//	//	//	//
Av (highest) [dB]	26	25.3	23.6	30.8	13	20.2°	26.2°	13
NF,DSB (best) [dB] §	8.2	8	7.3	9.5	5.5	7.7	5.5	11
NF,DSB (worst) [dB]	10.8	12.7	9.1	12.9	7.5	12^°	10^°	14
ICP1dB (best) [dBm] §	-18	-16.8	-25	-20	-16	-28°	-27°	-12
ICP1dB (worst) [dBm]	-26.5	-24	-30.7^	-25.3^	//	//	//	//
Pdc [mW]	8	12	57		89 +	14°	30°	14
Area [mm²]	0.085		0.675		0.23 +	0.225°		0.18 *

+ no quadrature output
^ estimated from plot
° per element
* estimated from chip photo
§ best and worst performance reported over operating frequency range

Figure 26.8.6: Performance summary and comparison with prior integrated mm-wave receivers.

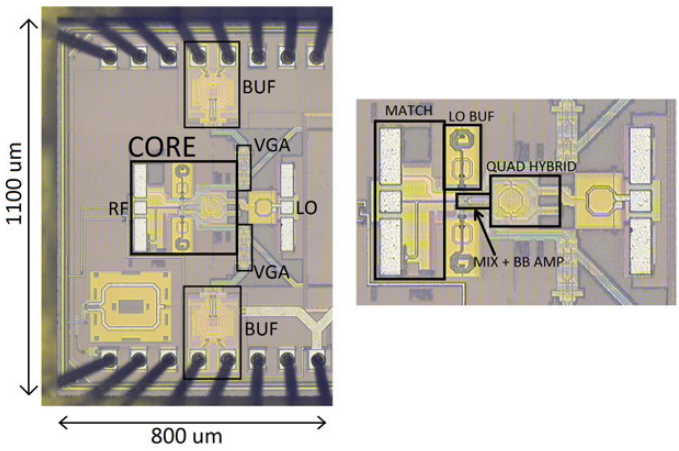

Figure 26.8.7: Die micrograph and detailed view of the RX front-end layout.

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26.9 A 13th-Order CMOS Reconfigurable RF BPF with Adjustable Transmission Zeros for SAW-Less SDR Receivers

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Current cellular receivers often employ acoustic filters (SAW or BAW) for each communication band due to their high selectivity, low insertion loss, and small formfactor. The need to support multiple communication bands, multi-input multi-output (MIMO) communications, and carrier aggregation necessitates the use of several such acoustic filters with a large overall footprint. These acoustic RF filters employ several high-Q acoustic resonators to create several poles and transmission zeros in a high-order transfer function to achieve low insertion loss within a nearly flat passband, fast roll-off, and highly attenuated stopband. The low quality factor of integrated passive components, specifically inductors, leads to a significant increase of insertion loss (proportional to the filter order and inversely proportional to the component quality factor) and poor stopband rejection for an equivalent RF filter.

On-chip N-path filters mimic the functionality of high-Q second-order bandpass resonators with a clock-controlled tunable center frequency. Single- and multi-resonator N-path tunable bandpass RF filters (Fig. 26.9.1(a) and (b)) have been reported [1]. Same order of filtering has also been reported in charge domain [2]. In order to increase the filter selectivity (steeper transition-band roll-off and higher stopband attenuation), transmission zeros (TZ) may be added to the filter transfer function. Recently, combination of active transconductance cells and passive N-path resonators [3,4], and filtering-by-aliasing [5] have been investigated to create BPFs with transmission zeros at the cost of lower passband bandwidth. In summary, a reconfigurable integrated bandpass RF filter with sufficiently high passband bandwidth and selectivity has not been found by the authors in literature. This paper presents a 13th-order monolithic reconfigurable bandpass filter prototype with tunable transmission zeros achieving 30-to-50MHz tunable BW_{3dB} and a steep 100dB/100MHz transition-band roll-off enabling close-by-blocker rejection.

In a coupled-resonator bandpass filter, transmission zeros in either side of the passband may be introduced by adding inductors and capacitors in series with the coupled resonators (Fig. 26.9.1(c)). Given that the resonators are replaced with N-path circuitry that are driven by the same clock frequency, it is important that the filter design uses resonators that have the same resonant frequency. One challenge associated with capacitively coupled N-path resonators is the undesired charge sharing between the capacitors of the coupled N-path resonators, thereby reducing the effective quality factor of the N-path resonators. Furthermore, the coupling network affects the passband shape and bandwidth. The proposed bandpass filter (Fig. 26.9.1(d)) utilizes three resonators that are coupled through inductive and inductive-plus-capacitive networks. The capacitor (inductor) in series with the leftmost (rightmost) resonator creates a transmission zero to the left (right) of the filter passband. The values of the passive coupling components together with all coupled resonant tanks determine the filter specifications such as bandwidth, transition-band roll-off, etc. In the implemented filter, the coupled resonators are replaced with N-path resonators while all coupling and series capacitors are variable and realized as a bank of switched capacitors enabling filter reconfigurability beyond clock-frequency tuning (Fig. 26.9.2). The values of switched capacitors in the N-path filters depend on the number of non-overlapping clock phases (4 phases in this prototype). In order to reduce the power consumption of the multi-phase clock distribution network, the multi-phase generation circuitry is local to each of the N-path resonators. Due to the isolation provided by the coupling inductors, each N-path resonator can be treated separately, and the three local 4-phase non-overlapping clock generators need not be synchronized in phase. The inductors are realized as on-chip spirals. The low quality factor of coupling inductors does not degrade the filter response.

The performance of an N-path system can be degraded by a few practical non-idealities. First, the clock signals that are used to drive the CMOS switches have a finite rise/fall time as determined by the power budget and technology parameters. Second, the parasitic capacitance of MOS switches contributes to unwanted charge sharing between switched capacitors of adjacent clock phases. Both effects decrease the equivalent quality factor (Q) of the N-path resonators, and subsequently degrade the response of the high-order BPF that is based on these resonators. The reduced quality factor of the N-path resonator, effectively modeled with a parallel resistor, may be enhanced by adding a negative parallel resistor realized as a cross-coupled differential pair. To maintain the desired DC bias voltage of 0.5V across each N-path filter and suppress the gain at even harmonics, complementary cross-coupled differential pairs are used. 2.5V NMOS and PMOS I/O transistors are used for the cross-coupled pairs to allow larger voltage swings and, hence, to enhance system linearity. Binary-weighted arrays of complementary cross-coupled differential pairs are employed to control the value of Q-boosting negative resistances to realize different filter responses.

The proposed differential filter has been fabricated in the TSMC 65nm CMOS technology (Fig. 26.9.7). To facilitate single-ended measurements, two off-chip baluns are used at the input and output. The insertion loss due to the baluns is de-embedded and measurement results are referred to the chip input and output. Figure 26.9.3 shows a representative measured filter frequency response with f_{LO}= 875MHz, passband bandwidth of 40MHz, and transition band roll-off slope of 100dB/100MHz. In this specific configuration, transmission zeros are placed at around 835MHz and 910MHz resulting in >17dB and >19dB blocker rejection at these two close-in frequencies, respectively. It is seen that the gain at the second harmonic is significantly suppressed thanks to the differential clocking scheme. To accommodate different filtering requirement, filter bandwidth and locations of transmission zeros can be tuned by changing discrete capacitor values and equivalent negative resistances. As shown in Fig. 26.9.3, tunable bandwidth from 30 to 50MHz is achieved while maintaining roll-off slope >100dB/100MHz and in-band input/output return loss larger than 7dB. Figure 26.9.4 demonstrates that the filter response with a bandwidth of 40MHz, the roll-off slope of 100dB/100MHz, and return loss larger than 7dB can be replicated across a wide spectrum from 800MHz to 1.1GHz. Figure 26.9.5 shows linearity measurement results for filter centered on f_{LO}= 875MHz, with a passband bandwidth of 40MHz. It is important to mention that maintaining a similar filter response at different center frequencies requires adjusting the values of tunable capacitors, as well as value of Q-boosting negative resistances as the LO frequency changes. The measured in-band IIP3 (IIP3-IB) is 25dBm, with two tones separated by 1MHz, and in-band 1dB compression point (ICP_{1dB}) is 7dBm as shown in Figs. 26.9.5(a) and (b), respectively. Figure 26.9.5(c) demonstrates the filter linearity performance as a function of the blocker offset frequency Δf. The blocker-induced 1dB compression point (B_{1dB}) achieves 9dBm, with a blocker only 40MHz away from test signal. In a two-tone test, a 24dBm out-of-band IIP3 (IIP3-OOB) is measured with two blockers only 40MHz apart. Performance summary and comparison with previous works are shown in Fig. 26.9.6. Compared to prior art this work achieves simultaneous wide passband bandwidth and sharp roll-off slope across a wide spectrum while maintaining comparable NF, system linearity, and power consumption.

Acknowledgements:
This work is partially supported by DARPA through the RF FPGA program and NSF through the EARS program.

References:
[1] R. Chen and H. Hashemi, "Passive Coupled-Switched-Capacitor-Resonator-Based Reconfigurable RF Front-End Filters and Duplexers," *IEEE RFIC*, pp. 138-141, May 2016.
[2] Y. Xu and P. Kinget, "A Switched-Capacitor RF Front End with Embedded Programmable High-Order Filtering," *IEEE JSSC*, vol. 51, no. 5, pp. 1154–1167, May 2016.
[3] Y. Lien et al., "A High-Linearity CMOS Receiver Achieving +44dBm IIP3 and +13dBm B1dB for SAW-less LTE Radio," *ISSCC*, pp. 412-414, Feb. 2017.
[4] G. Qi et al., "A 0.7 to 1 GHz Switched-LC N-Path LNA Resilient to FDD-LTE Self-Interference at ≥40 MHz Offset," *IEEE RFIC*, pp. 276-279, May 2017.
[5] S. Hameed and S. Pamarti, "A Time-Interleaved Filtering-by-Aliasing Receiver Front-End with >70dB Suppression at <4×Bandwidth Frequency Offset," *ISSCC*, pp. 418-419, Feb. 2017.

 978-1-5090-4940-0/18/$31.00

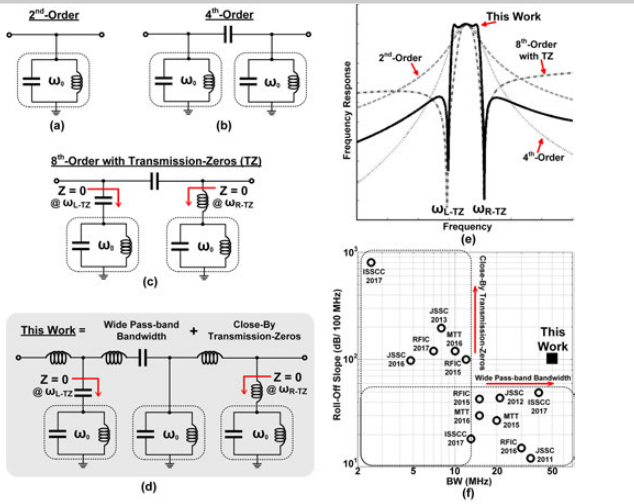

Figure 26.9.1: (a)-(e) Evolution of the proposed filter topology along with representative corresponding transfer functions, (f) Performance summary of past monolithic CMOS RF band-pass filters.

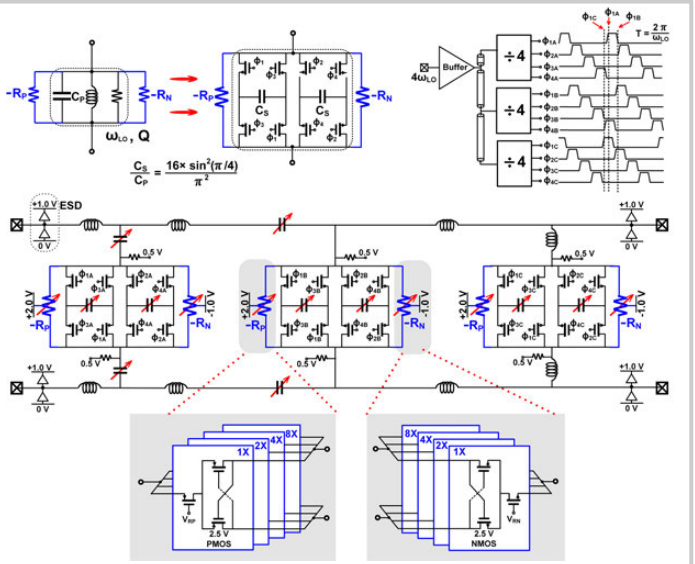

Figure 26.9.2: Schematic of the proposed filter.

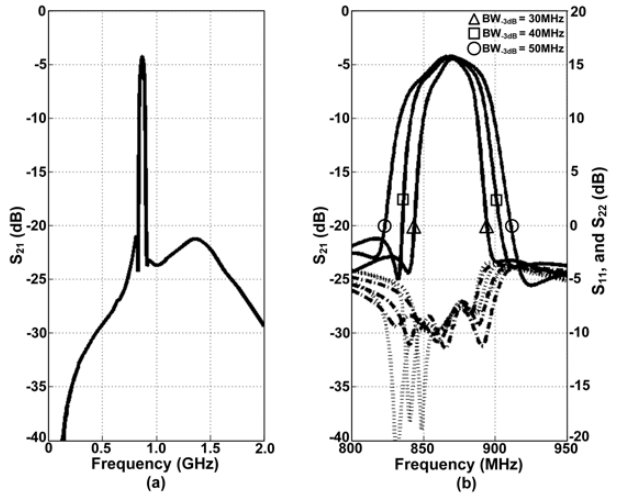

Figure 26.9.3: (a) Representative measured filter response with a 40MHz bandwidth centered on f_{LO}=875MHz, (b) Representative measured filter shapes with bandwidth of 30, 40, and 50MHz.

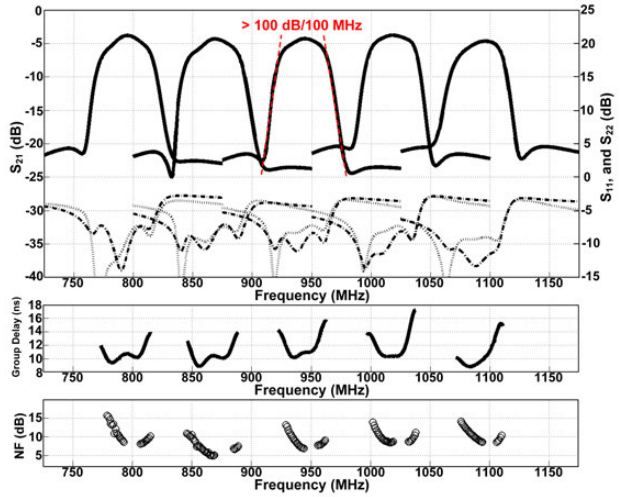

Figure 26.9.4: Representative measured small-signal S-parameters, group delay, and NF of filters with similar frequency response centered on different frequencies.

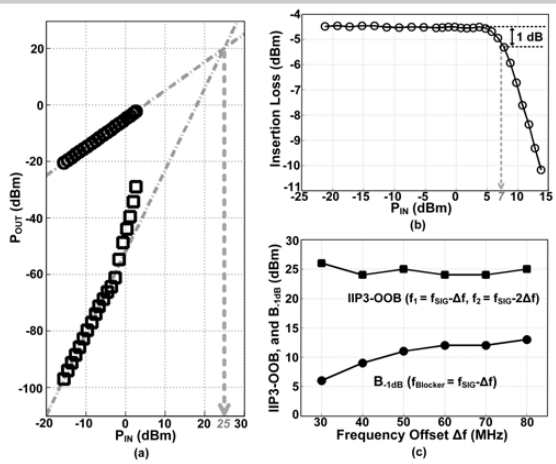

Figure 26.9.5: (a) Measured output signal and IM3 power levels versus input power, (b) Measured insertion loss versus input-signal power level, (c) Measured out-of-band (OOB) IIP3, and B_{1dB} as a function of OOB blocker frequency offset Δf. In all plots, filter response is centered on f_{LO}=875 MHz with BW_{3dB}=40 MHz and f_{SIG}=864MHz.

	RFIC 2016 [1]	JSSC 2016 [2]	ISSCC 2017 [3]	RFIC 2017 [4]	ISSCC 2017 [5]	This Work
Technology	65 nm CMOS	40 nm CMOS	28 nm CMOS	180 nm CMOS SOI	65 nm CMOS	**65 nm CMOS**
Topology	N-Path	Charge-Domain Filtering	N-Path	N-Path +LNA	Filtering by Aliasing	**N-Path**
Tuning Range (GHz)	0.5 - 1.1	0.1 - 0.7	0.1 - 2.0	0.7 - 1.0	0.1 - 1.0	**0.8 - 1.1**
Filter Order	4	1 - 4	5	8	NA	**13**
Adjustable Transmission Zero	No	No	No	No	Yes	**Yes**
Roll-Off Slope (dB/ 100 MHz)	15 *	98 *	18.3 *	120 *	49 * / 800 *	**100**
BW_{3dB} (MHz)	30	3.2 - 4.8	13	8 *	40 / 2.5	**30 - 50**
ICP_{-1dB} (dBm)	5	-27 *	-6 *	NA	-7 *	**7**
B_{-1dB} (dBm)	11	15 (Δf/BW= 6.2)	13 (Δf/BW= 6.2)	8 (Δf/BW= 5.0)	9.5 (Δf/BW= 2.0) 13 (Δf/BW= 4.0)	**9 (Δf/BW= 1.0)**
IIP3-IB (dBm)	19.2	NA	5	NA	8	**25**
IIP3-OOB (dBm)	26	24 (Δf/BW= 6.2)	44 (Δf/BW= 6.2)	32.3 (Δf/BW= 5.0)	21 (Δf/BW= 1.2)	**24 (Δf/BW= 1.0)**
NF (dB)	3.8 - 5.8	6.8 - 9.7	4.1 - 10.5	5.5 - 6.4	7	**5.0 - 8.6**
Power (mW)	15 - 25	59 - 105	38 - 96	42 - 57	64 - 84	**80 - 97**
Active Area (mm^2)	0.50 *	2.03	0.49	2.2	2.3	**1.9**

* Estimated from figures

Figure 26.9.6: Performance summary and comparison.

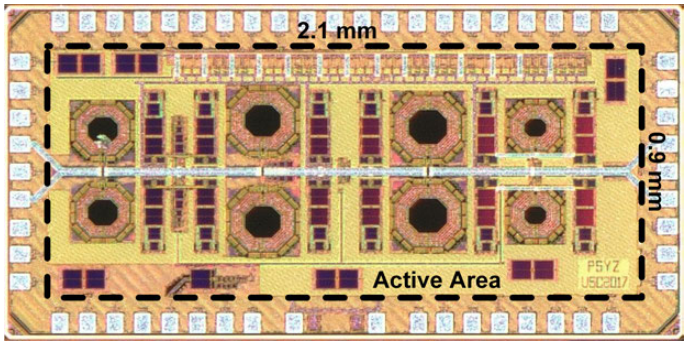

Figure 26.9.7: Die micrograph.

978-1-5090-4940-0/18/$31.00

26.10 A 128-Pixel 0.56THz Sensing Array for Real-Time Near-Field Imaging in 0.13µm SiGe BiCMOS

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Real-time terahertz video cameras are regarded as key enabler systems for numerous applications. Unfortunately, their spatial resolution is fundamentally restricted by the diffraction limit. Near-field-scanning optical microscopy (NSOM) is used in the THz domain to break through this limit [1]. Recently reported THz near-field sensors based on silicon technology promise significant improvements compared to NSOM with respect to sensor sensitivity, system cost, and scanning time [2,3]. However, only single-pixel implementations have been presented with unmodulated CW sources so far, which limits the sensors dynamic range (DR) due to detector 1/f noise. This paper scales-up the research of near-field sensing into larger surfaces made of a plurality of super-resolution pixels with video-rate imaging capabilities. The 128-pixel 0.56THz imaging array includes all functions such as illumination, sensing, detection, and digital readout on a single silicon chip.

Figure 26.10.1 shows the scalable circuit architecture implemented in a 0.13µm SiGe-BiCMOS technology (IHP) with f_t/f_{max}=300/450GHz. The core of each pixel is a cross-bridged double-split-ring resonator (SRR) with a lateral resolution on the µm scale [2] (Fig. 26.10.2). The sensor exposes a sharply confined electric field to the top surface of the chip around two short strips. With an object placed in the sensing volume, the capacitive part of the resonator increases and the SRR resonance frequency shifts towards lower frequencies. For a fixed excitation frequency, this leads to a change in transmitted power and to a dielectric-permittivity-based imaging contrast with the maximum response caused by metallic objects [2,3].

The array consists of two 64-pixel-long rows of SRRs and power detectors in a vertically mirrored arrangement. Each row is divided into 16 subarrays of 4 pixels, each driven from a single chopped free-running triple-push oscillator (TPO) (Fig. 26.10.3) to provide the highest possible array density. All 4 sensors in a subarray are interconnected with a corresponding TPO by means of a 4-way equal-power splitter consisting of two cascaded, 3.9dB-insertion-loss (540GHz) modified Wilkinson power splitters [4] in a stripline configuration (Fig. 26.10.2). The subarray schematic is provided in Fig. 26.10.3. The oscillator is based on a 534-to-562GHz Colpitts TPO with 28µW output power presented in [2]. A current-mirror biasing scheme is used for external-reference current control (I_{ref}) and source chopping with a 1.2V CMOS controlled base pull-down logic. The TPO oscillation is periodically turned on/off by pulling down the common DC base bias with an externally supplied chopping signal (chop). The chopped THz wave is then coupled capacitively (25fF) to a SiGe-HBT power detector with an estimated current responsivity of 0.48A/W [2]. The pixels comprise a beta-helper current-mirror biasing scheme that can be controlled with a 3.3V CMOS selection logic. The array is operated with only one TPO and one detector turned on at a time enabling a fully scalable circuit architecture with a total power consumption of 79mW. All detectors share an active PMOS load to convert the detector output current to voltage.

The detector output signal is further processed by a 0-to-42dB gain active bandpass filter (BP) and a lock-in amplifier (LIA) as shown in Fig. 26.10.1. The LIA comprises a passive CMOS mixer, a third-order switched-capacitor lowpass filter, and an instrumentation amplifier. The lowpass corner can be externally adjusted with the LPclk frequency to optimize the frame rate vs. the SNR. The LIA output is subsequently sampled with a 6b flash ADC with programmable reference voltages. The flash architecture was chosen to support fast oversampling with successive approximation algorithms and dynamic range adjustments to accommodate oscillator/detector PVT variations and varying signal strengths due to different materials. The ASIC part provides registers for reference voltage and gain settings, address decoders, multiplexers, clock dividers, and an SPI interface.

Full-wave EM simulations were conducted to investigate the impact of the power-splitting network and the coupling capacitor on the single sensor performance and the cross-coupling between pixels. Simulation results of the transmitted power through the 4-way power splitter and the SRRs are presented in Fig. 26.10.2 for one detector (IN-to-Det_1) as a function of frequency and object material properties. Note, that the slope above the resonance frequency is well preserved compared to a single sensor [2] because of the good isolation (>30dB, Fig. 26.10.2) and return loss provided by the divider network. Because of the specific row arrangement, two different coupling phenomena need to be considered. First, the coupling through the radiative and reactive near-field zones between the pixels, not connected through the divider network, was analyzed and found to be negligible (<-46dB). Second, the parasitic coupling between sensors connected to the same divider network was found to be more relevant, due to a finite variation of the power division ratios at the internal divider nodes as a function of the object loading conditions. Figure 26.10.2 presents the simulated power transmission (IN-to-Det_1) in a 4-way sensor arrangement across frequency for different object loading conditions while influenced by the closest-proximity pixel (Det_2) with varying material properties. The worst-case scenario occurs for a perfect electric conductor on Det_2 and no object on Det_1. This shifts the resonance frequency down and causes a -27dB change in relative power at the detector input, referred to the oscillator power available at the resonator input. This corresponds to a dielectric permittivity uncertainty of around 0.1 for an object with a relative permittivity of 2 (Fig. 26.10.2).

The array can be operated in an analog or a digital readout mode. In analog mode, the single pixel sensor performance was measured using setup a) as shown in Fig. 26.10.4 with the BP output signal muxed to a pad (TP1, Fig. 26.10.1). The dynamic range (DR), defined as the ratio between the maximum sensor response for a metal tip and the spot noise at a chopping frequency (f_{chop}), is typically around 93dB at f_{chop}=200kHz. The DR variations are within 18dB due to a global biasing scheme unable to accommodate pixel-to-pixel process variations. The measured parasitic coupling between 4 subarray pixels is smaller than -23dB. In digital mode, the sensor performance was measured with setup b) shown in Fig. 26.10.4 by analyzing the ADC output for a single pixel in the time domain. The DR of the digital readout is 37dB with 64 averaged samples per pixel (1MHz sampling clock) resulting in a frame-rate of 28fps for the whole array (f_{chop}=200kHz, 2.45kHz low pass corner). Imaging results are shown in Fig. 26.10.5 for a Ni-mesh close-to direct contact with the chip surface. The mesh exhibits a 50µm bar width and a 250µm bar pitch. The 2D image was acquired during a single 1D lateral scan at a 1µm step size. The sensors resolve the bar edges with 15µm resolution according to a 10-to-90% rising-to-falling edge criterion, being slightly higher than the previously reported 10 to 12µm [2] due to the soft bar edges of the mesh.

Figure 26.10.6 shows a comparison of this work with prior near-field imaging systems and Fig. 26.10.7 shows the die micrograph. This work advances the prior art in Fig. 26.10.6 by showing a monolithically integrated THz super-resolution imaging SoC with real-time capability. The array provides a scanning time reduction of more than two orders of magnitude and increases the dynamic range by up to 51dB compared to previously reported single pixel sensors in [2,3].

Acknowledgements:
This work was partially funded by the DFG priority program SPP 1857 ESSENCE and a Reinhart Koselleck project.

References:
[1] A. Adam, "Review of Near-Field Terahertz Measurement Methods and Their Applications," *J. Infrared, Millimeter and Terahertz Waves*, vol. 32, no. 8, pp. 976-1019, Sept. 2011.
[2] J. Grzyb et al., "Solid-State Terahertz Superresolution Imaging Device in 130-nm SiGe BiCMOS Technology," *IEEE TMTT*, DOI: 10.1109/TMTT.2017.2684120, in press.
[3] J. Grzyb et al., "A 0.55 THz Near-Field Sensor With a µm-Range Lateral Resolution Fully Integrated in 130 nm SiGe BiCMOS," *IEEE JSSC*, vol. 51, no. 12, pp. 3063-3077, Dec. 2016.
[4] S. Horst et al., "Modified Wilkinson Power Dividers for Millimeter-Wave Integrated Circuits," *IEEE TMTT*, vol. 55, no. 11, pp. 2439-2446, Nov. 2007.
[5] T. Mitsunaka et al., "CMOS Biosensor IC Focusing on Dielectric Relaxations of Biological Water With 120 and 60 GHz Oscillator Arrays," *IEEE JSSC*, vol. 51, no. 11, pp. 2534-2544, Nov. 2016.

 978-1-5090-4940-0/18/$31.00

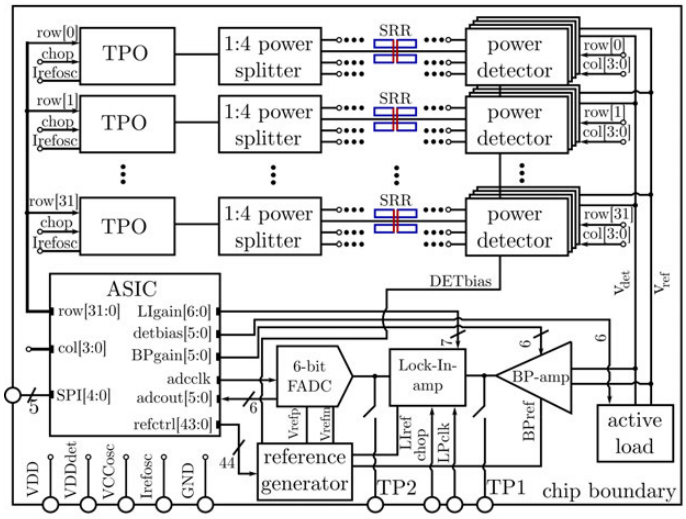

Figure 26.10.1: Block diagram of the 128-pixel near-field array.

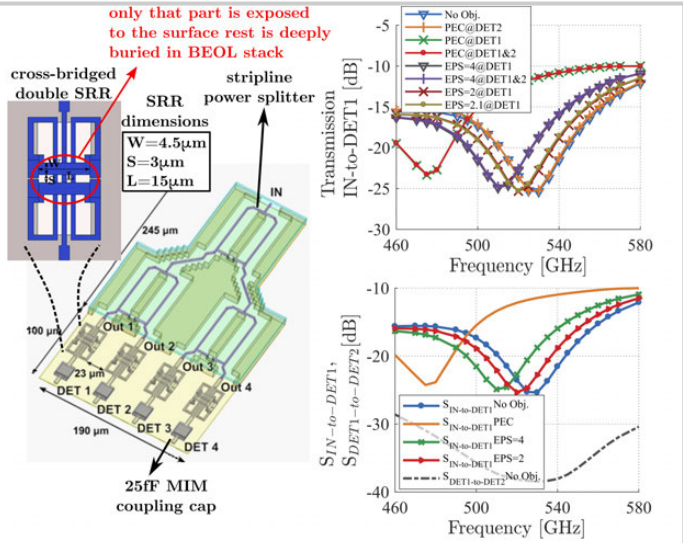

Figure 26.10.2: Illustration of the subarray arrangement and sensor simulation results.

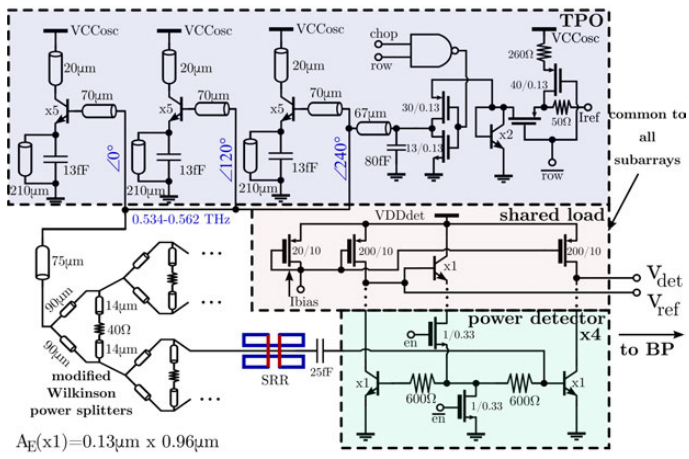

Figure 26.10.3: Schematic of a single 4×1-pixel subarray and the shared active load.

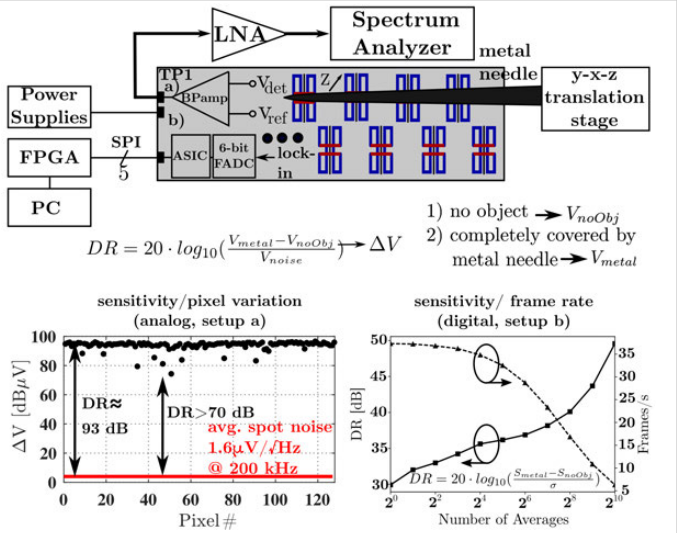

Figure 26.10.4: Analog/digital sensor characterization: Measurement setup a) and b) results.

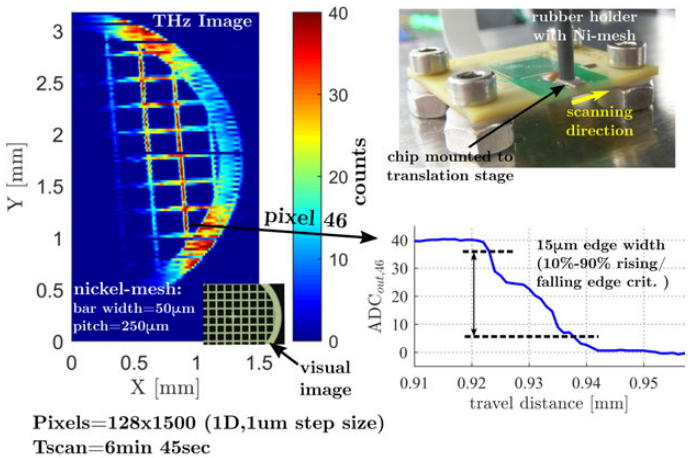

Figure 26.10.5: 2D imaging results for a 1D scan of a Ni-mesh (1µm step size).

Technology	Resolution [µm]	Frequency [THz]	Dynamic range [dB]	Integration level	Number of pixels	Ref.
NSOM	typ. 3.3-40	0.2-2.5	-	external detector/ source	1	[1]
0.13-µm SiGe	est. 10-12	0.534-0.562	42[1]	detector/ source	1	[2]
0.13-µm SiGe	est. 8-10	0.533-0.555	20[2]	detector/ source	1	[3]
65-nm CMOS	-	0.06,0.12	-	fully integrated	128,192	[5]
0.13-µm SiGe	**est. 10-12**	**0.534-0.562**	**93[3] 37@28fps[4]**	**fully integrated**	**128**	**This Work**

[1] estimated to be equal to the SNR of the image in Fig. 19 [2]
[2] estimated to be equal to the SNR of the image in Fig. 25.1.5 [3]
[3] measured at the bandpass output (TP1), referenced to a bandwidth of 1Hz
[4] DR off the full readout chain with 64 averaged ADC samples for every pixel

Figure 26.10.6: Comparison table for near-field imagers.

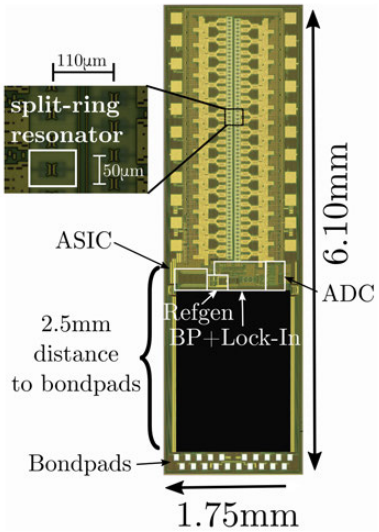

Figure 26.10.7: Die micrograph (stitched). The blacked-out region contains circuits that are not related to the array.

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