ISSCC 2018

SESSION 26

RF Techniques for Communication and Sensing

A 0.55-to-0.9GHz 2.7dB NF Full-Duplex Hybrid-Coupler Circulator with 56MHz 40dB TX SI Suppression

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[1]Oregon State University, [2]Intel Corporation Hillsboro

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Outline

- Motivation
- Hybrid-Coupler based Circulator-RX
- Circulator-RX Implementation in 65-nm CMOS
  - Design
  - Measurements
- Conclusion and Future Work

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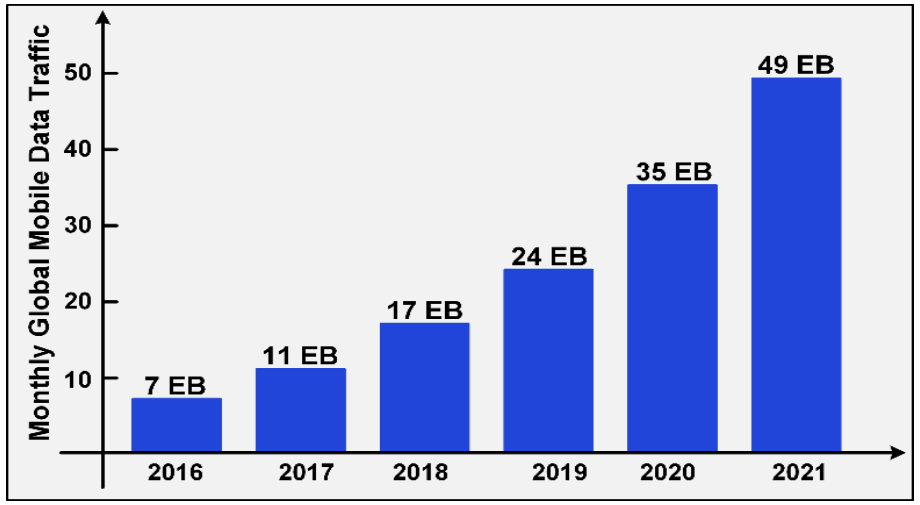
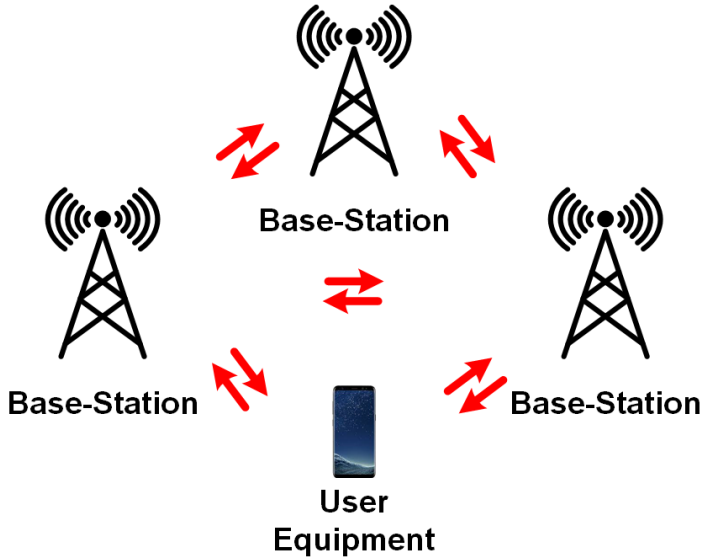
Full Duplex Links: Increased Spectrum Efficiency/Throughput



Source: Cisco VNI Mobile, 2017



- Demand for wireless data transfer increasing rapidly; however limited spectrum available.
- Full-duplex links can increase throughput (up to 2x for a single link).
- Further increase in throughput possible with listen-and-talk network protocols that reduce latency. [1, 2]

[1] J. Choi *et al.*, MobiCom' 10, [2] Y. Choi *et al.*, WirelessComm' 13

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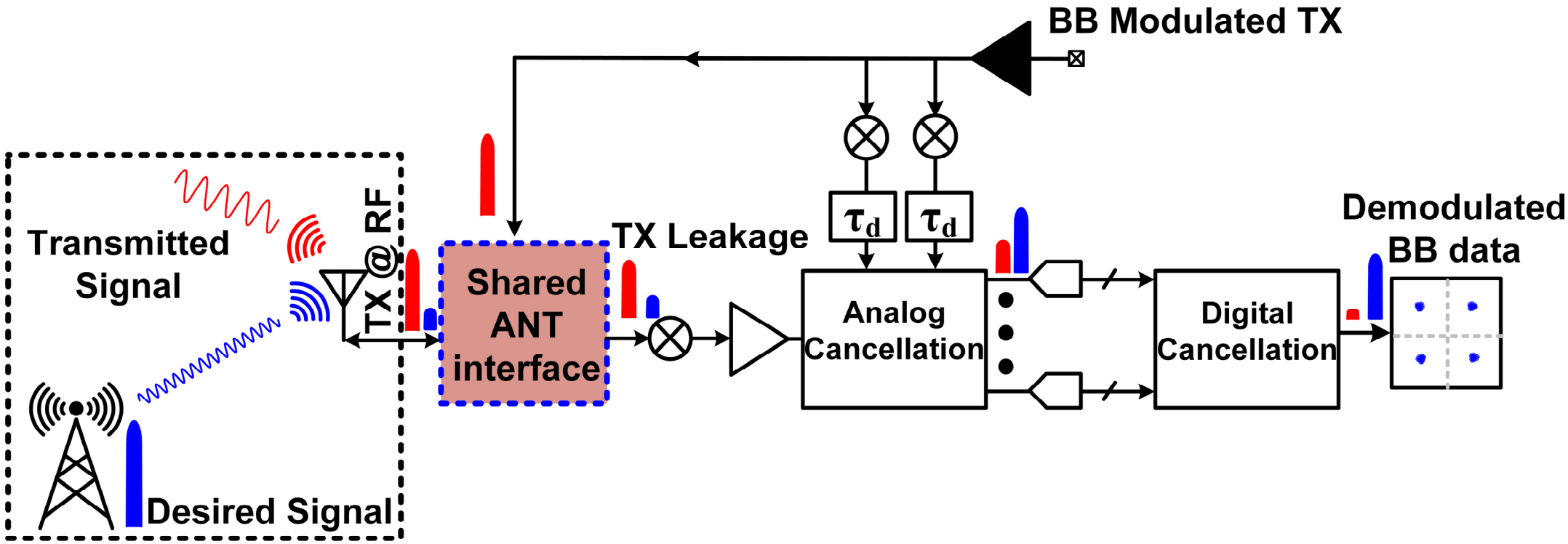
TX to RX Isolation in FD Links



- Up to 110dB [*] of overall SI cancellation required to maintain RX sensitivity.
- Assuming digital cancellation of 50dB → 60dB [*] of analog/RF SIC required.
- Shared antenna interface desirable for small area and channel symmetry.

[*] D. Bharadia *et al.*, SIGCOMM' 13

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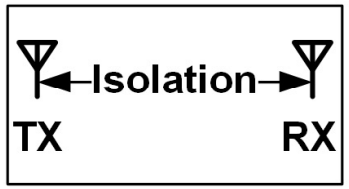
Antenna Interface Metrics

RX/TX Isolation for FD

Separate RX/TX ANT

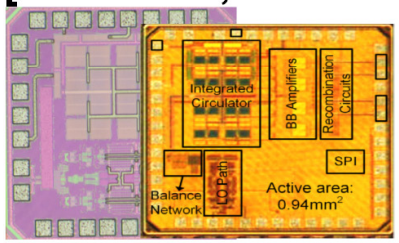


[J. Choi *et al.*, MobiComm '10]
[M. Duarte *et al.*, Asilomar '10]

Circulator

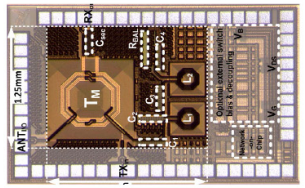
[Bharadia *et al.*, SIGCOMM '13]

[Zhou *et al.*, ISSCC '16]



[Reiskarimian *et al.*, ISSCC '17]

Electrical Balanced Duplexer



[Liempd *et al.*, ISSCC '15]

- Key metrics for the shared antenna interface:
  - TX to ANT Insertion Loss: Impacts link range and system efficiency.
  - ANT to RX Insertion Loss: Degrades RX NF.
  - TX to RX Isolation: Critical to reduce non-linearities due to TX SI in the RX.
  - Isolation BW: Limits modulation bandwidth of TX and desired signal.
  - Power handling: Limits TX output power.
  - Robustness against ANT VSWR

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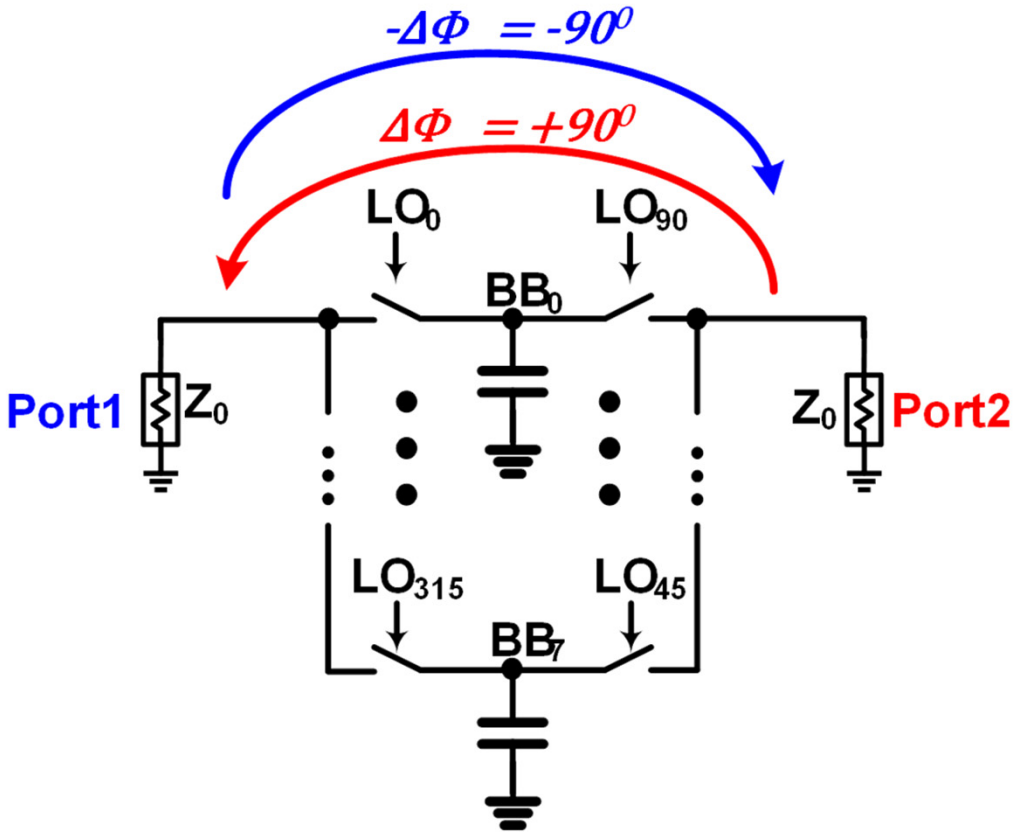
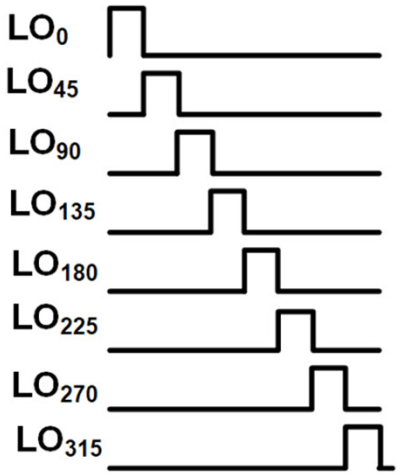
Non-Reciprocal Two-port N-path Mixers





For large number of phases

$$s = \begin{bmatrix} 0 & e^{-j\pi/2} \\ e^{j\pi/2} & 0 \end{bmatrix}$$

[Zhou *et al.*, ISSCC' 16]

Phase Non-Reciprocal 2-Port N-path Mixer

- Quadrature steady-state phase-shift from RF to BB for quadrature LO.
- N-path structure provides high-Q frequency selectivity.
- Non-reciprocal phase progression provides phase selectivity.

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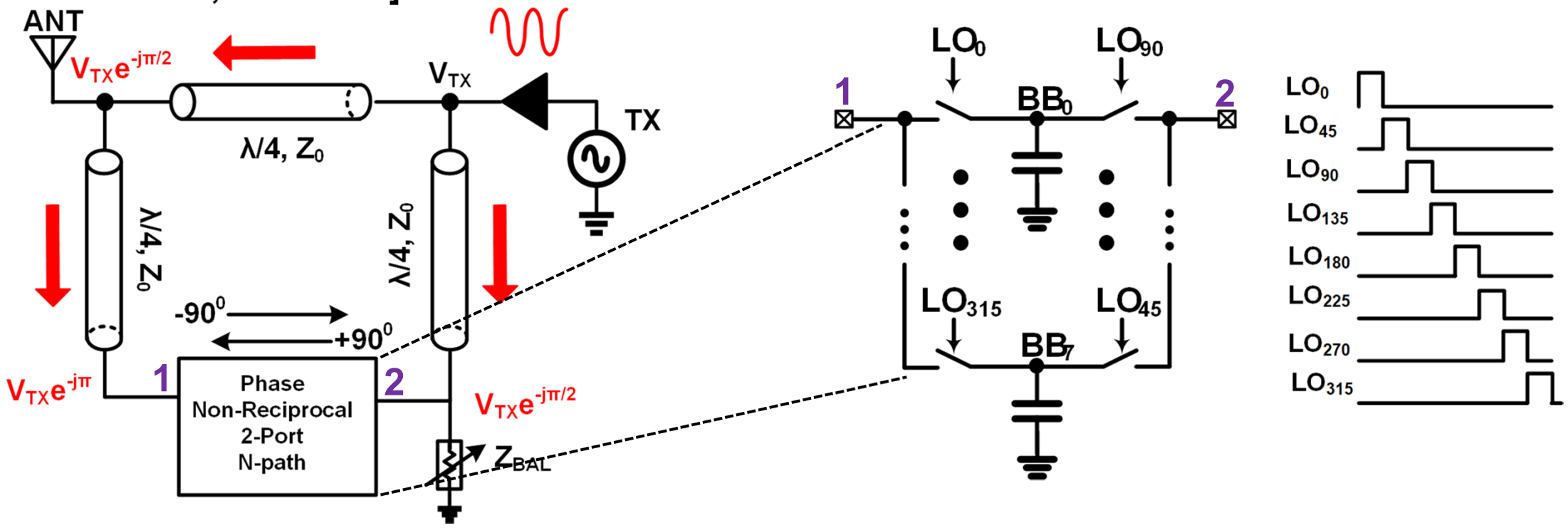
Two-port N-path Mixer-based Circulator: TX

[Reiskarimian *et al.*, ISSCC' 17]



- T-line structure creates quadrature TX phases at 2-port N-path mixer.
- TX signal combines destructively at the baseband(BB) capacitor providing TX SI cancellation(SIC).

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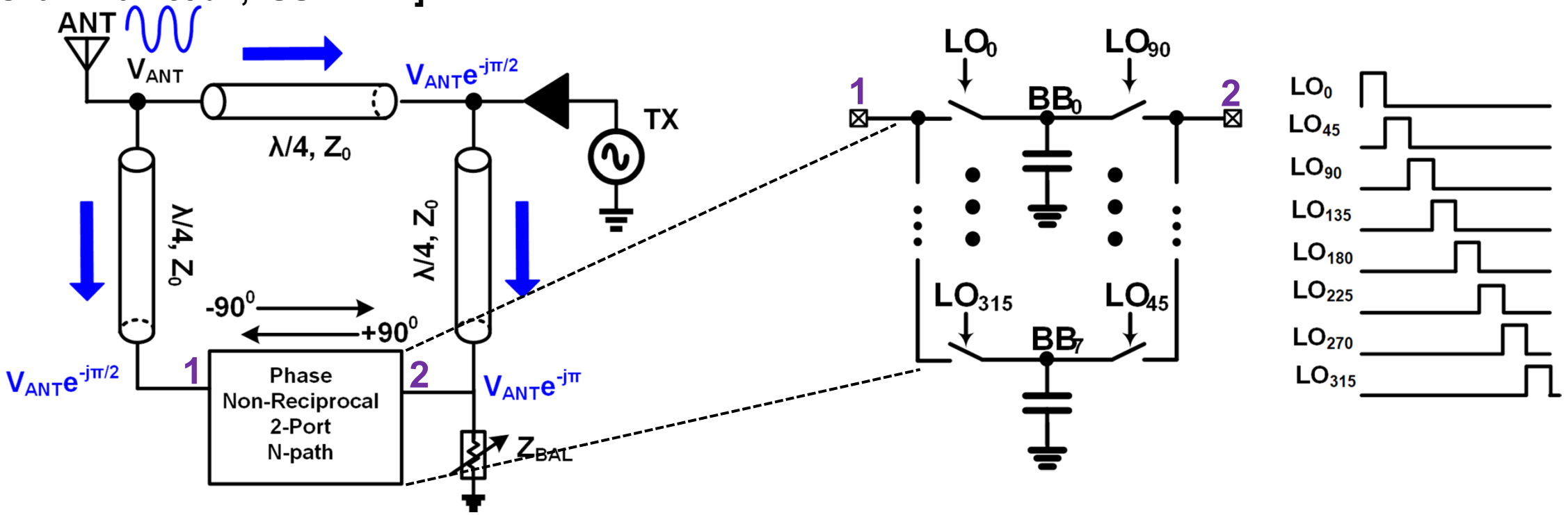
Two-port N-path Mixer-based Circulator: RX

[Reiskarimian *et al.*, ISSCC' 17]



- RX signal adds constructively at BB capacitors → desired signal reception with nulling of TX signal.
- No matching requirements → Potentially low-NF.
- Z_{BAL} can improve TX nulling but degrades measured NF.

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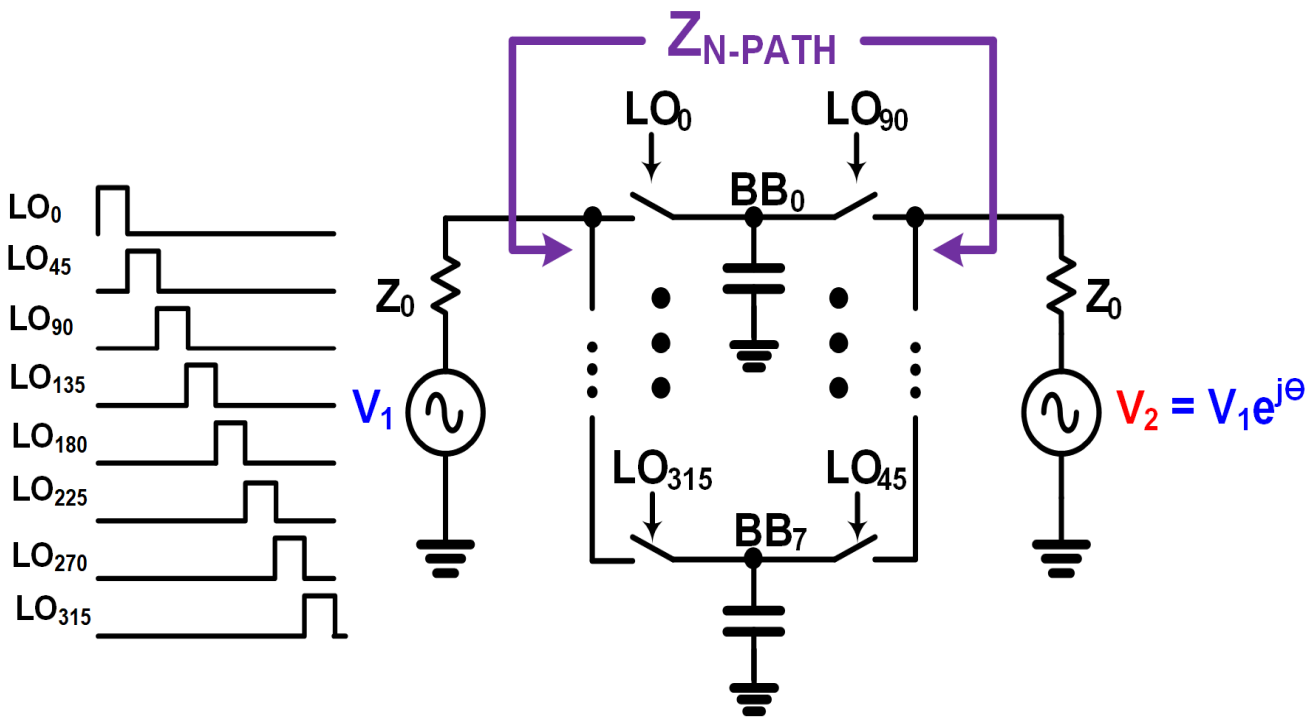
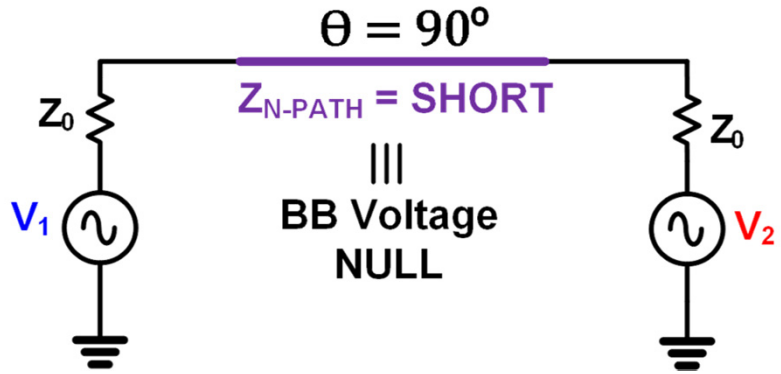
Two-Port N-path Filter Impedance





- Two-port N-path filter impedance dependent on relative phase difference between input signals and mixer LO signals.
- For balanced amplitude ($|V_1| = |V_2|$), LO phase progression shown, steady state “short” can be achieved for phase difference of 90º.

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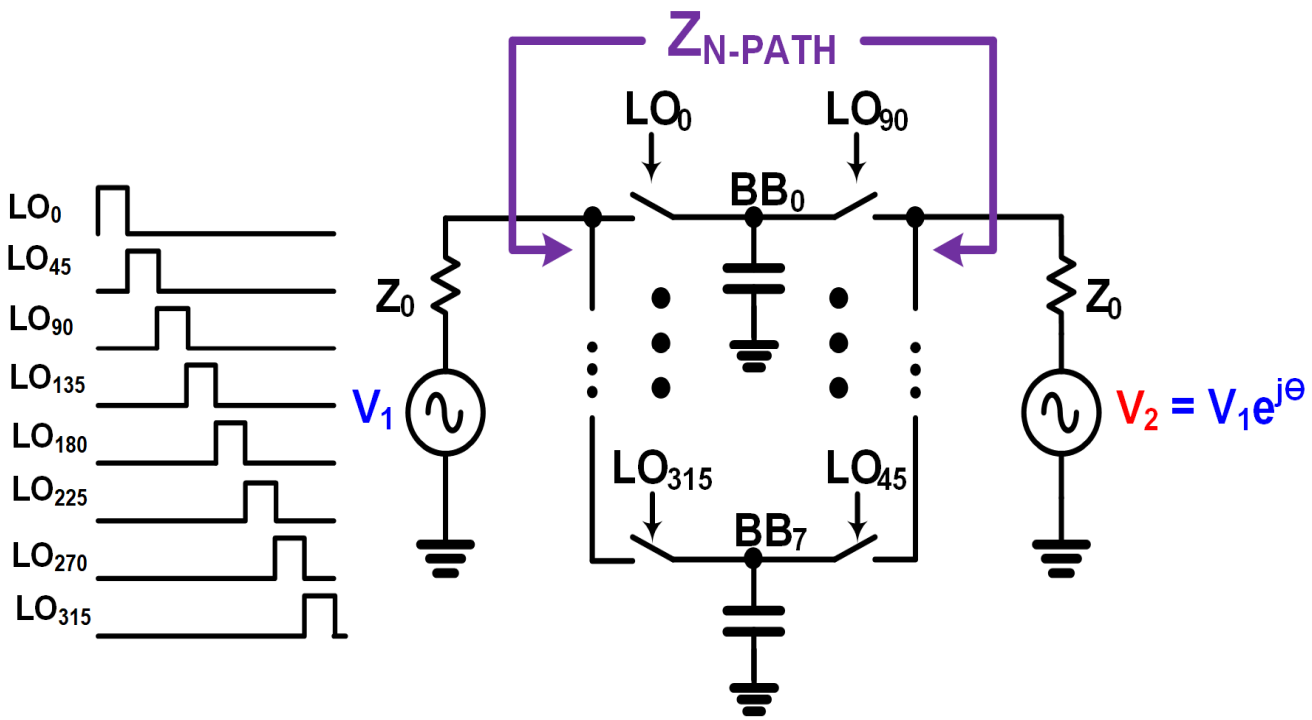
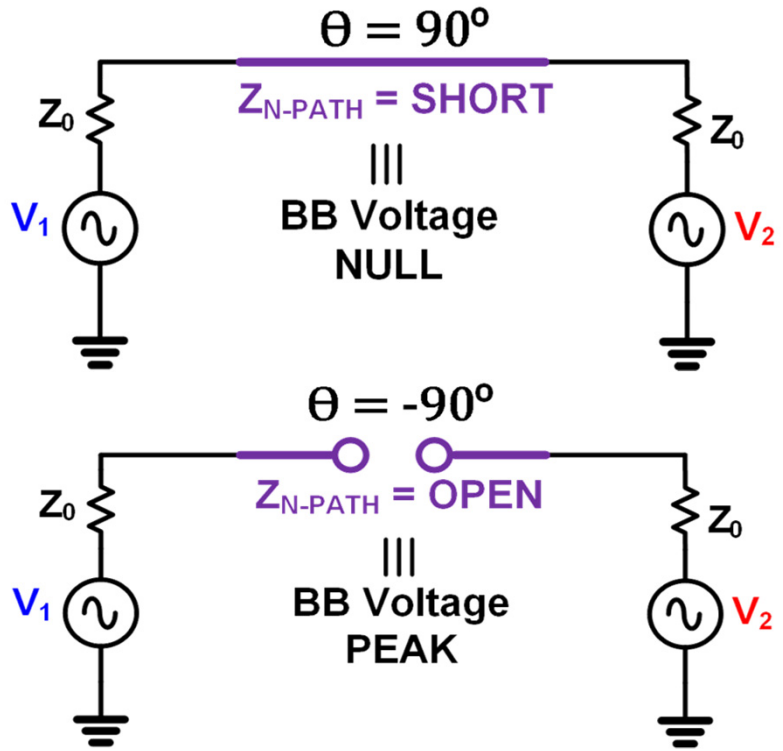
Two-Port N-path Filter Impedance





- Two-port N-path filter impedance dependent on relative phase difference between input signals and mixer LO signals.
- For balanced amplitude ($|V_1| = |V_2|$), LO phase progression shown, steady state “open” can be achieved for phase difference of -90º.

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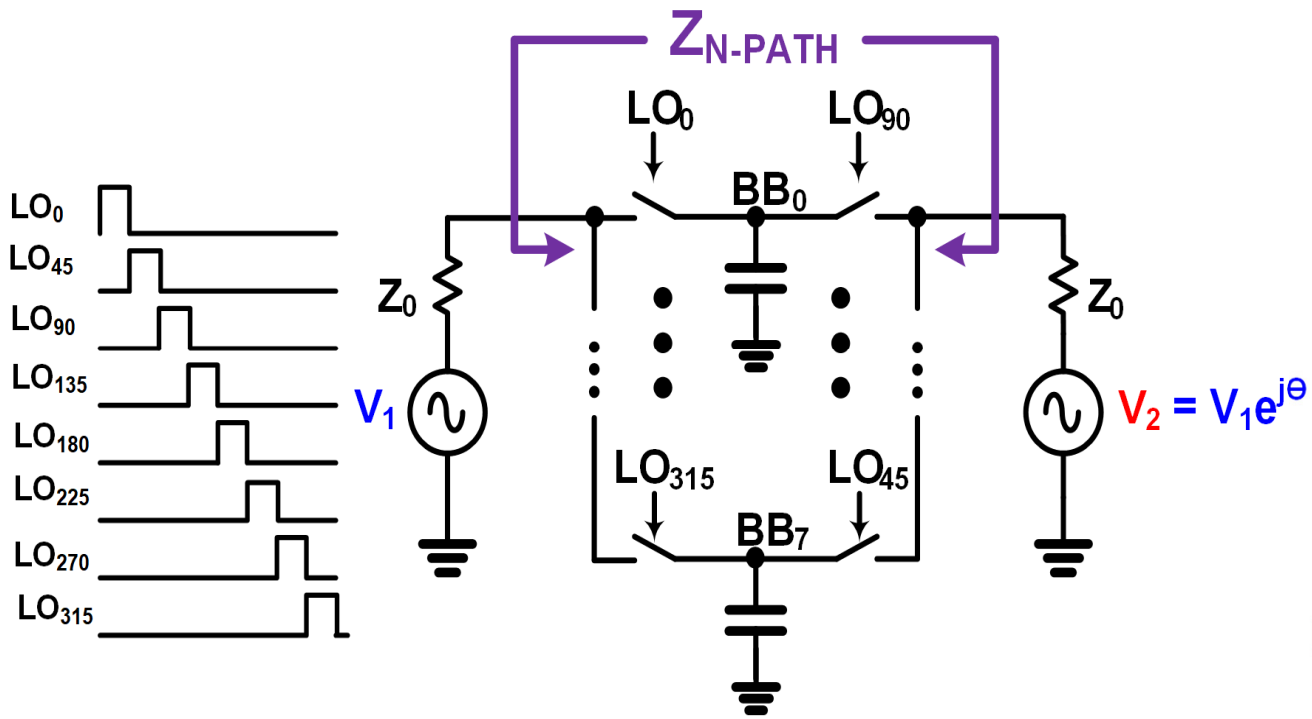
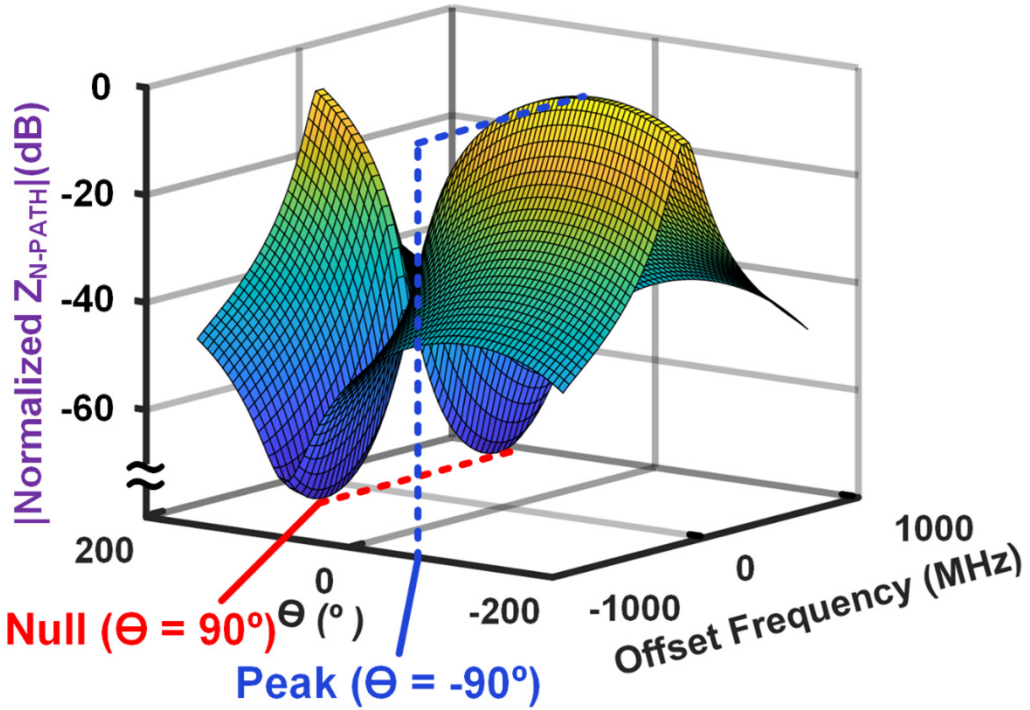
Two-Port N-path Filter Impedance





Phase Non-Reciprocal 2-Port N-path Mixer

- Two-port N-path mixer impedance depends on frequency and relative phase.
- Low impedance at frequencies offset from LO; null for θ = 90º.

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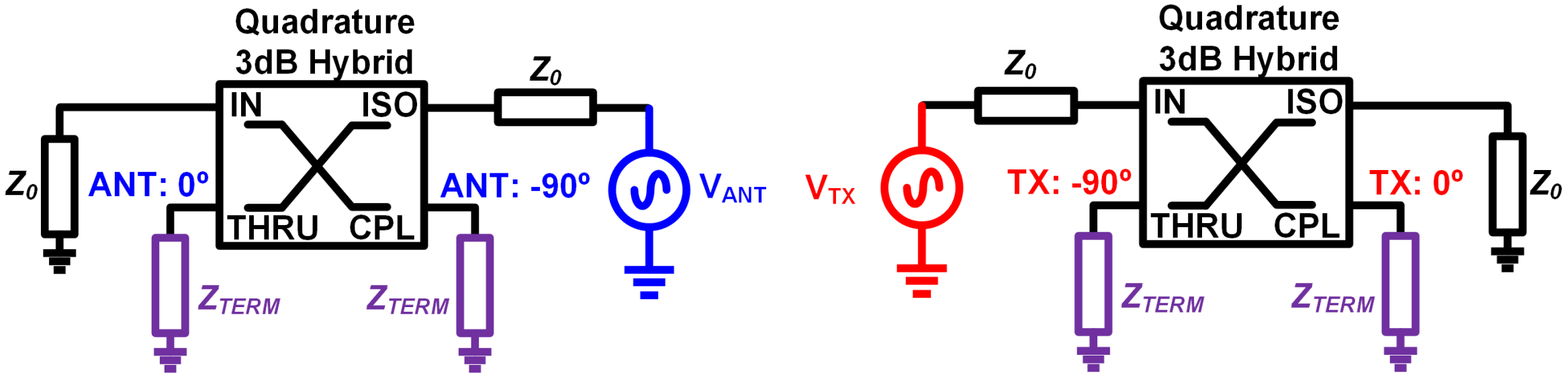
Hybrid Coupler: Quadrature Outputs



- ANT Input: Thru leads Couple port by 90°.
- TX Input: Couple leads Thru port by 90°.

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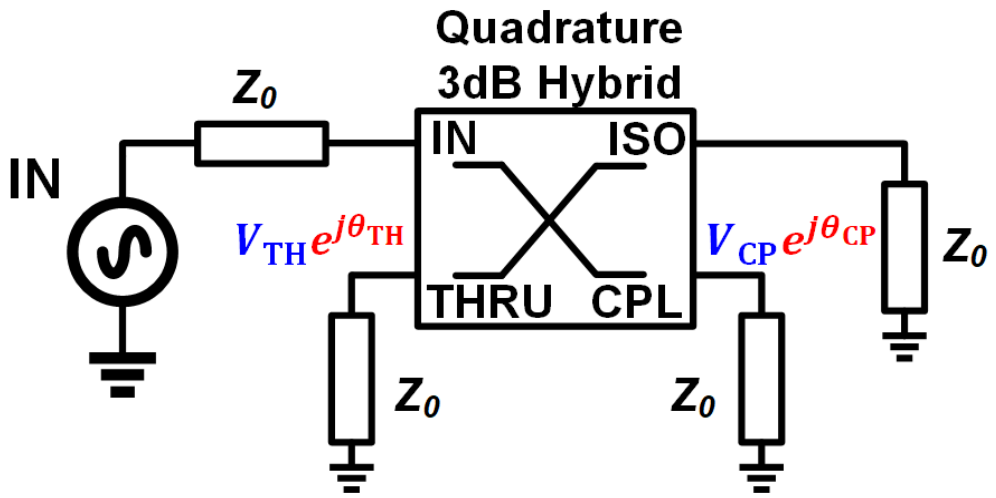
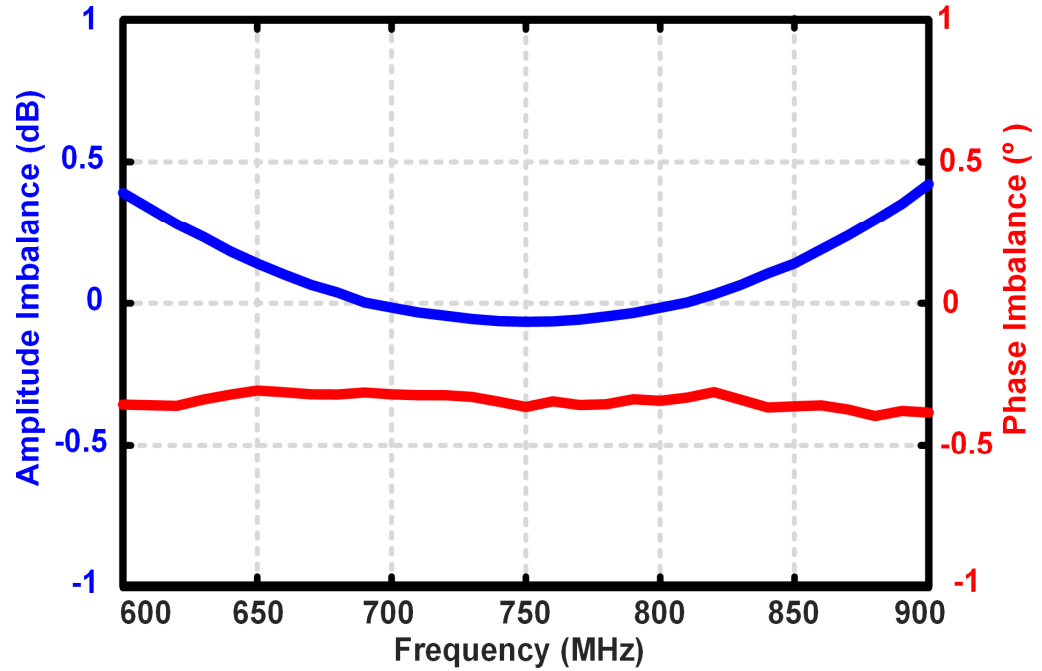
Hybrid Coupler: Quadrature Balance



$$\text{Amplitude imbalance} = 20 * \log10|V_{TH} - V_{CP}|$$

$$\text{Phase imbalance} = |\theta_{TH} - \theta_{CP}| - 90^0$$



Simulated Coupler phase and amplitude imbalance

- Couplers can provide wideband quadrature phase and amplitude balance.
- Symmetry leads to wideband TX SI cancellation.

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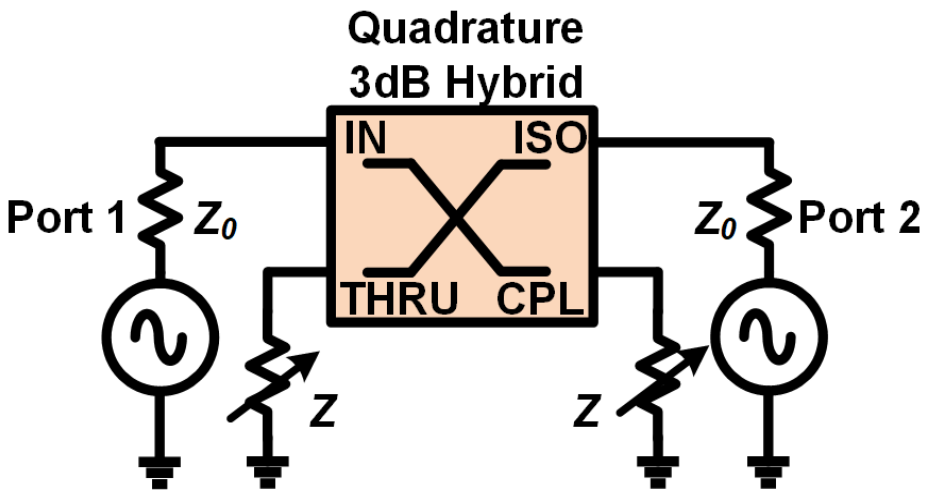
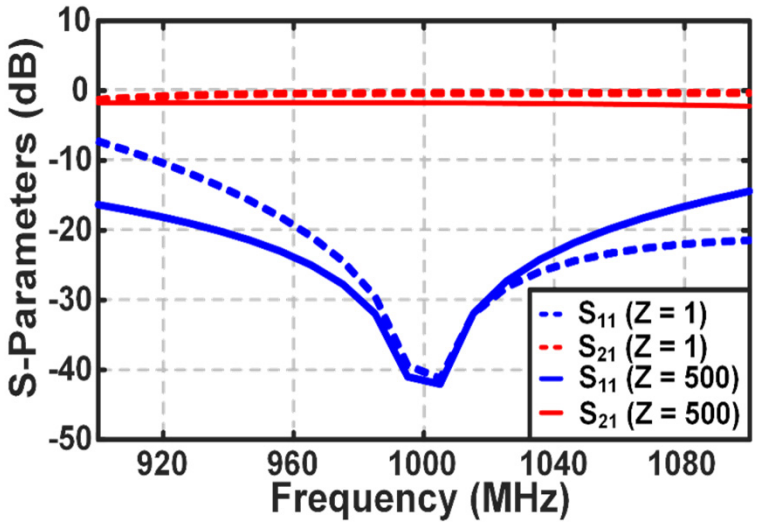
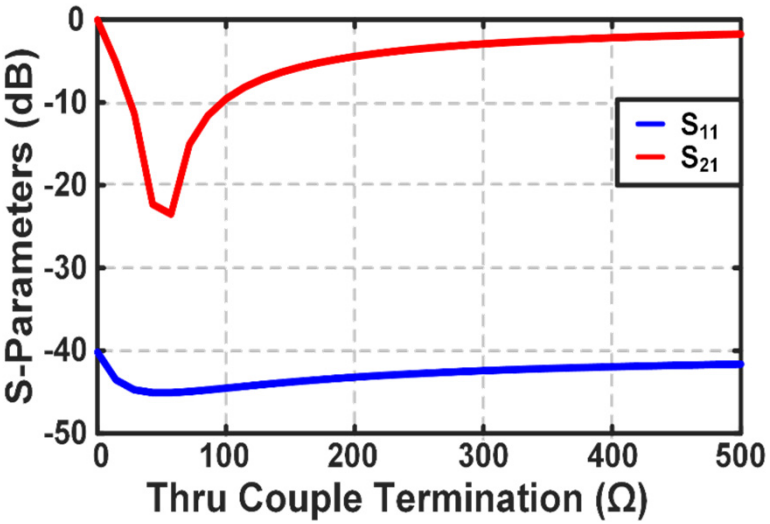
Hybrid Coupler: Thru and Cpl Terminations







- Thru and coupled ports terminated in a short/open:
  - Wideband matching at IN and ISO ports.
  - Insertion loss(IL) from IN→ISO and ISO→IN are function of hybrid coupler loss and termination resistance.
  - Lossless coupler terminated in ideal short/open → Zero IL.

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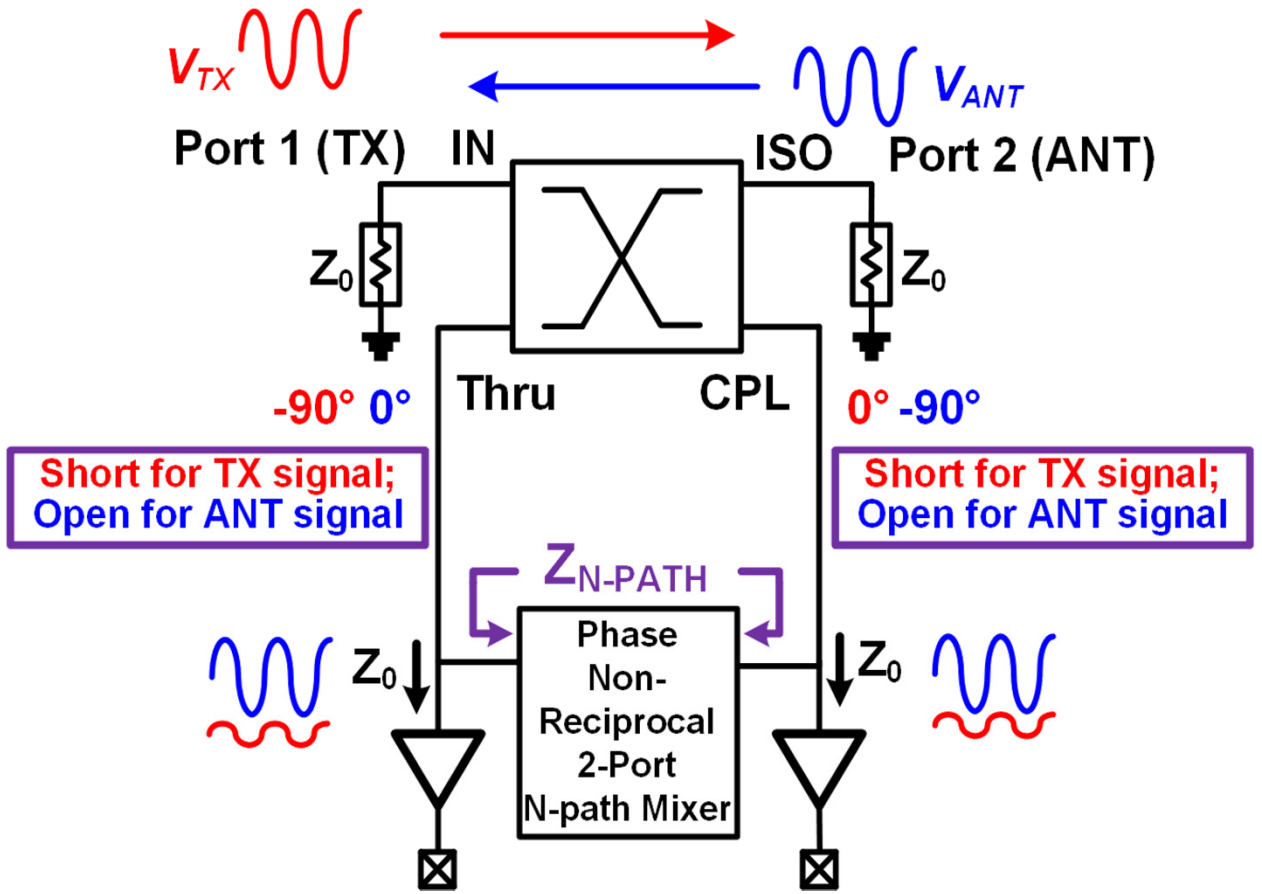
Hybrid Coupler based 4-Port Circulator



- Hybrid coupler with two-port N-path mixer → **Circulator functionality**.
- Two-port N-path mixer creates short for TX; open for signals incident at ANT.
- Quadrature RX signals available at the Thru and Cpl ports.

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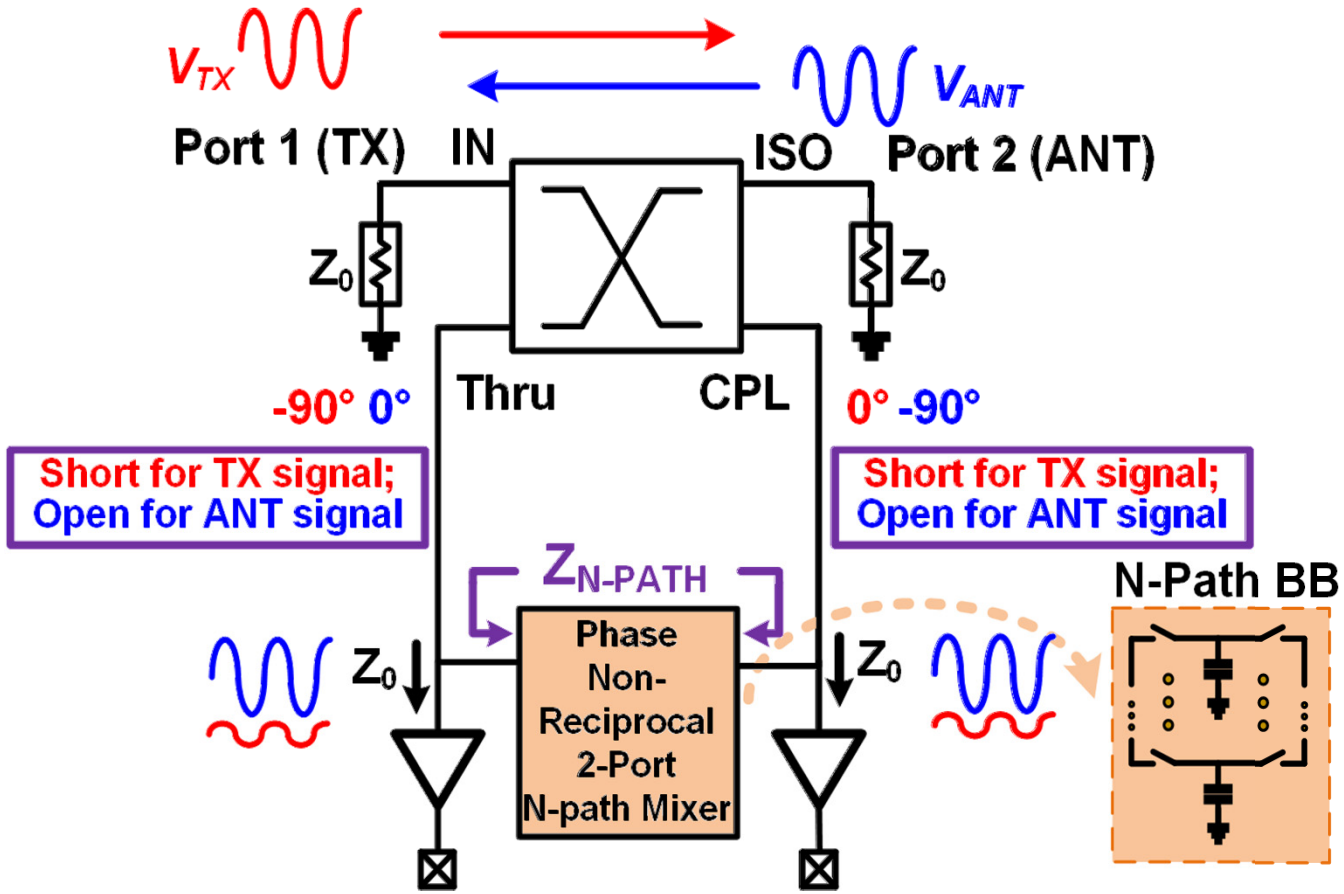
Hybrid Coupler based 4-Port Circulator



- Wideband coupler → Wideband TX SIC and wide tuning range.
- NF is limited by RX matching requirements.

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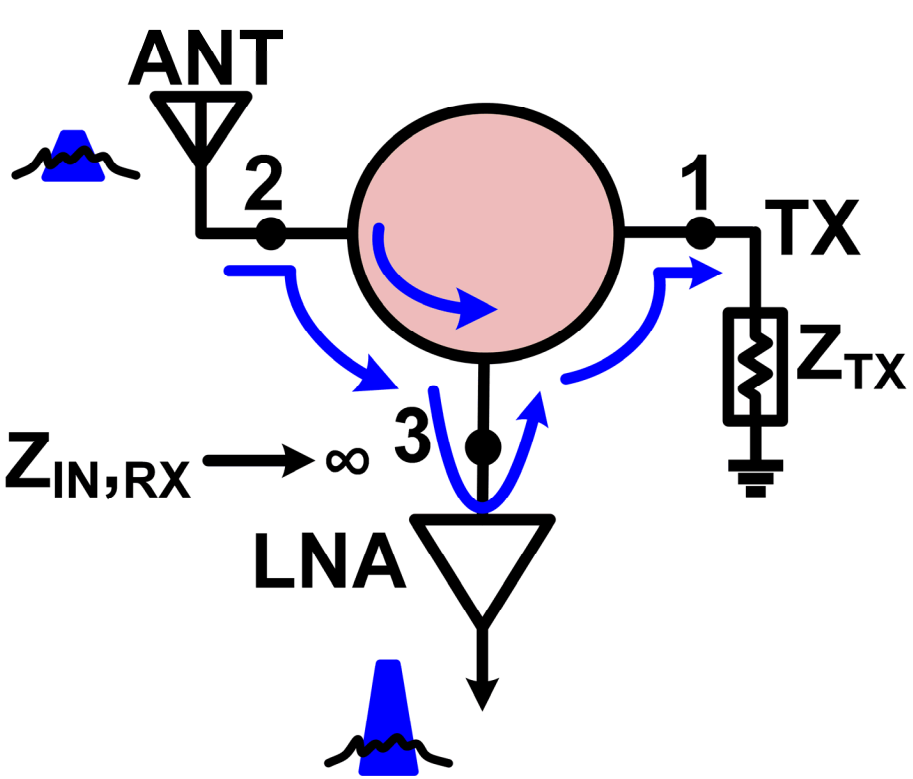
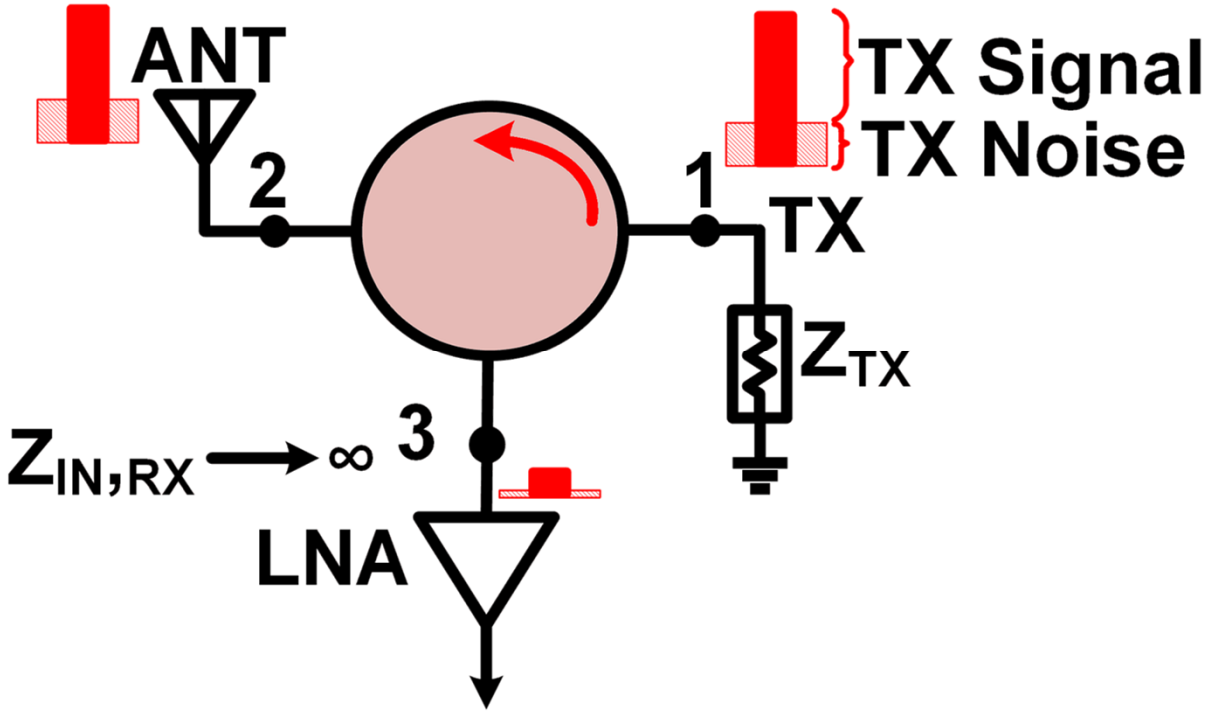
Circulator-RX with Mismatched RX Port





- Three-port circulator with high impedance termination on one port.
- ANT port matching due to TX impedance.
- High-impedance LNA designed for low noise.

[Reiskarimian *et al.*, ISSCC' 17]

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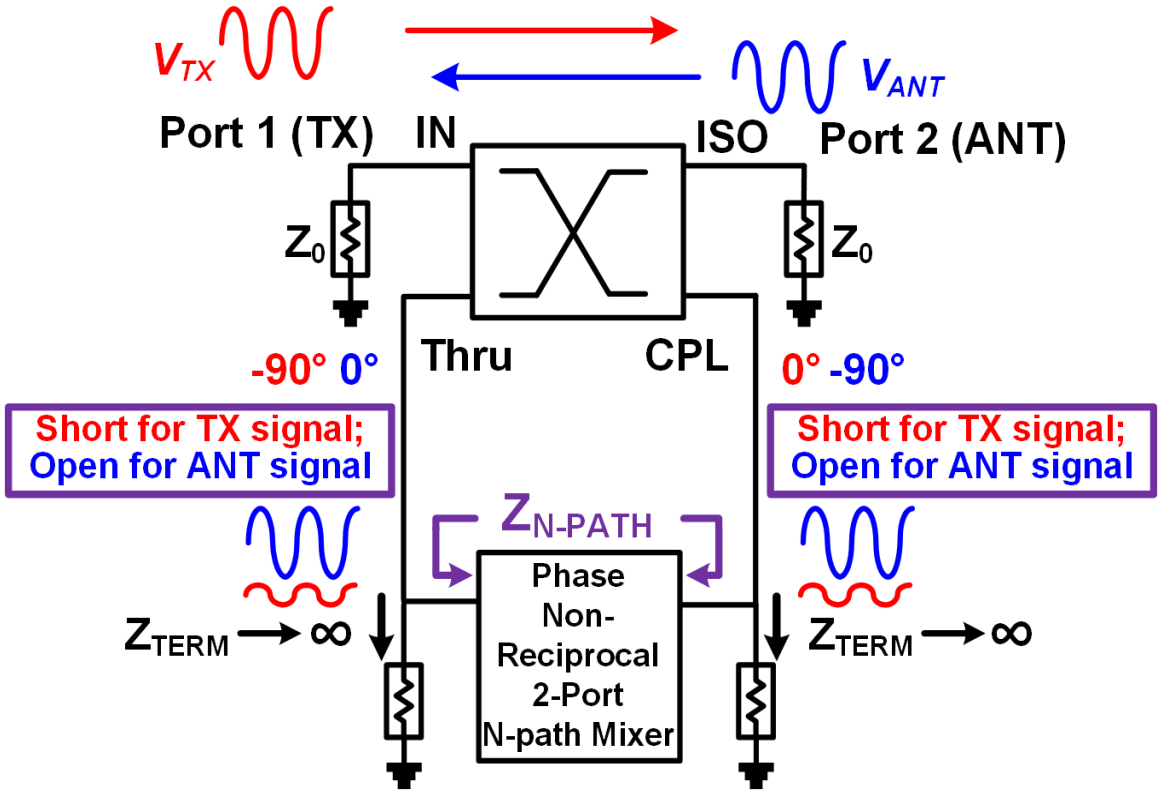
Hybrid Coupler based 3-Port Circulator



- Four-port circulator can also be adapted to a high-impedance termination on one of the ports.
- High-impedance termination provides the same benefits as 3 port case.

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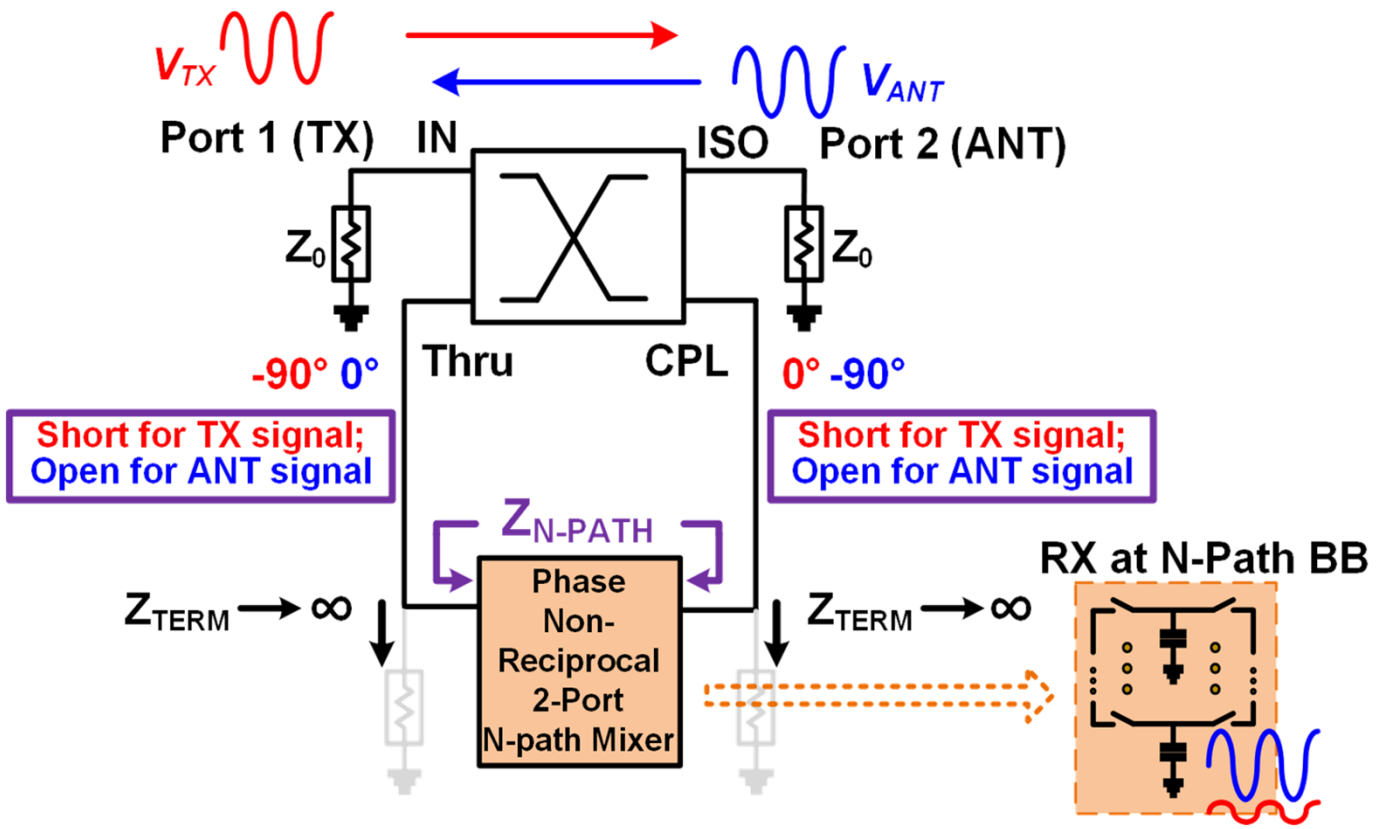
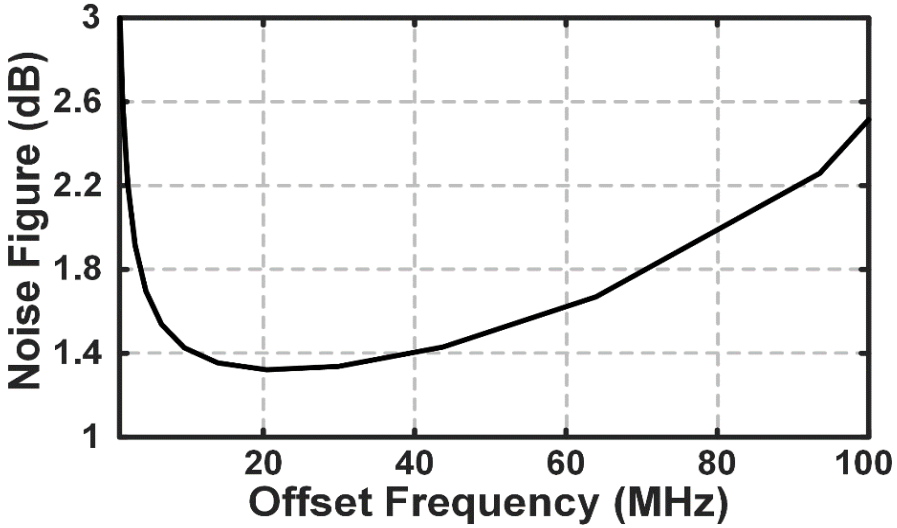
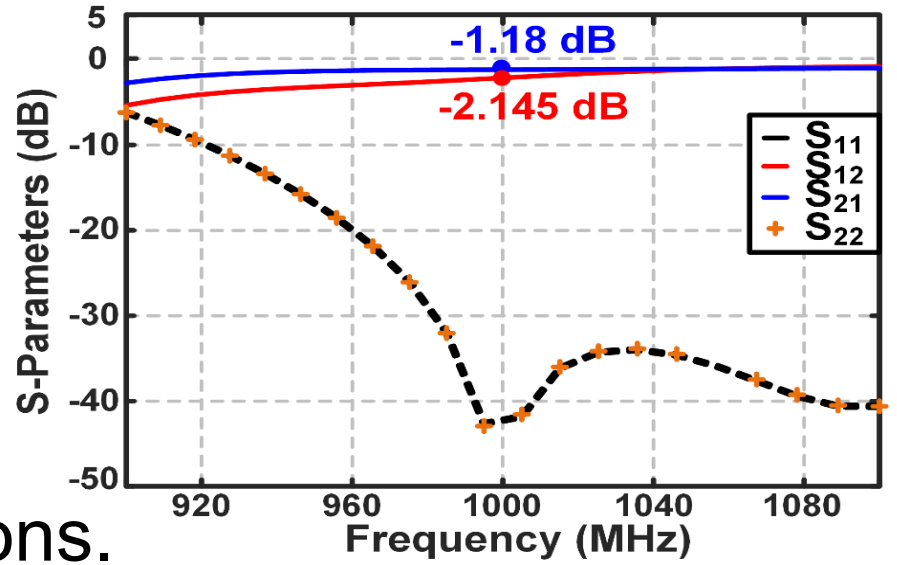
Hybrid Coupler based 3-Port Circulator







- Matching for ANT port provided by TX port.
- Noise from TX port does not appear at RX BB.
- RX BB designed with no matching considerations.

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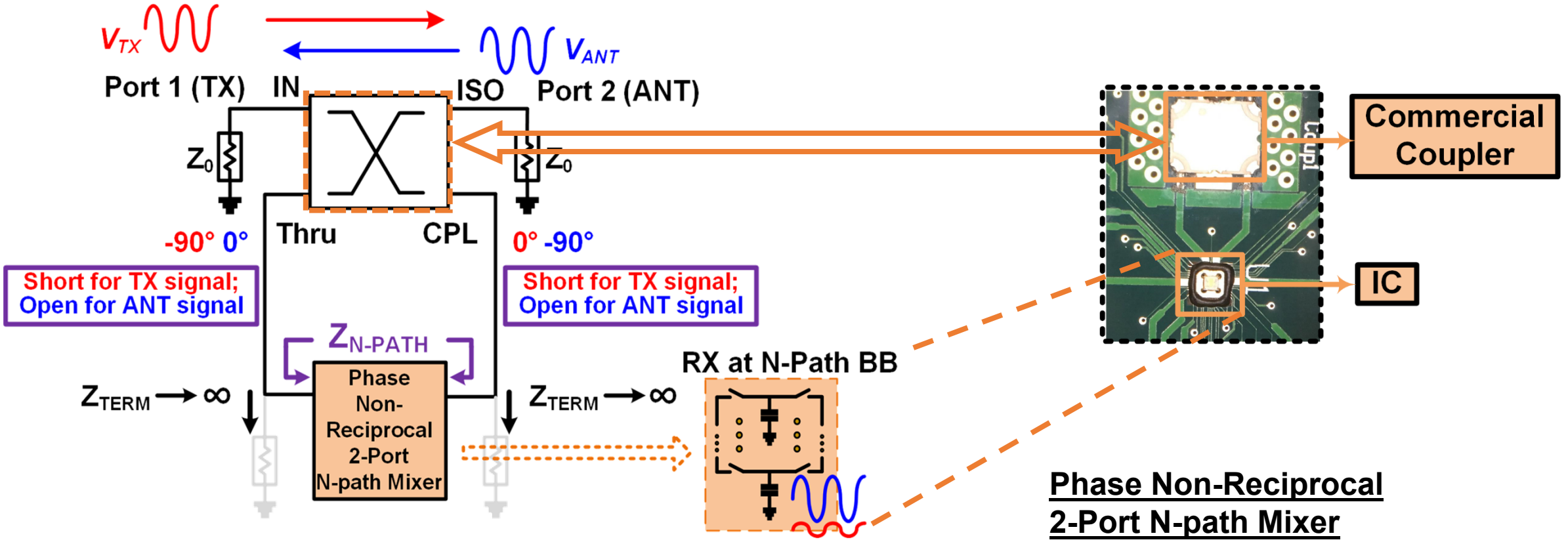

- Commercial wideband coupler achieves:
- 0.2dB insertion loss across 300 MHz BW (600MHz-900MHz).
- $<\pm 4^0$ phase imbalance and < ±0.25dB amplitude imbalance.

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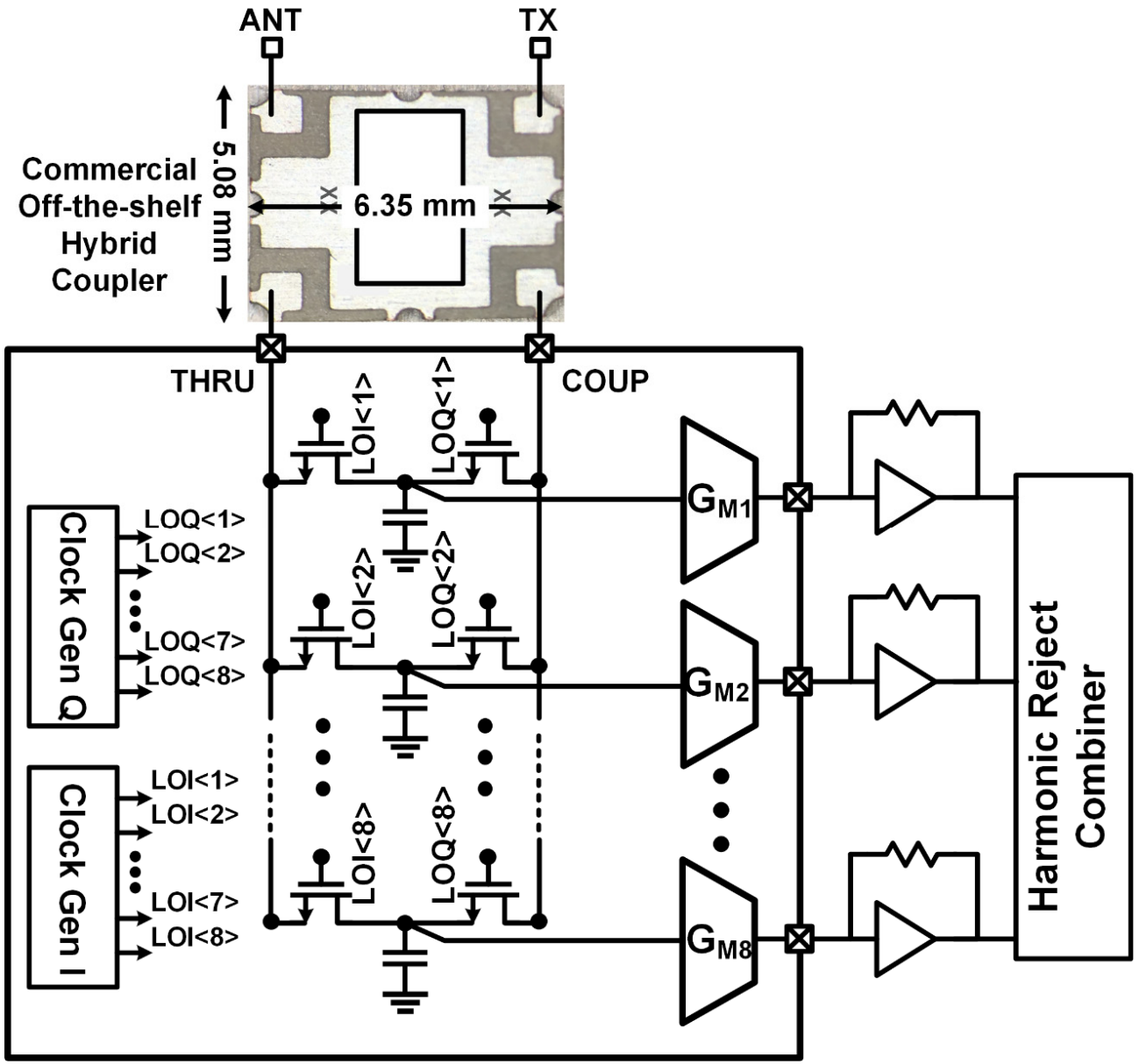
Circulator-RX Implementation in 65-nm CMOS



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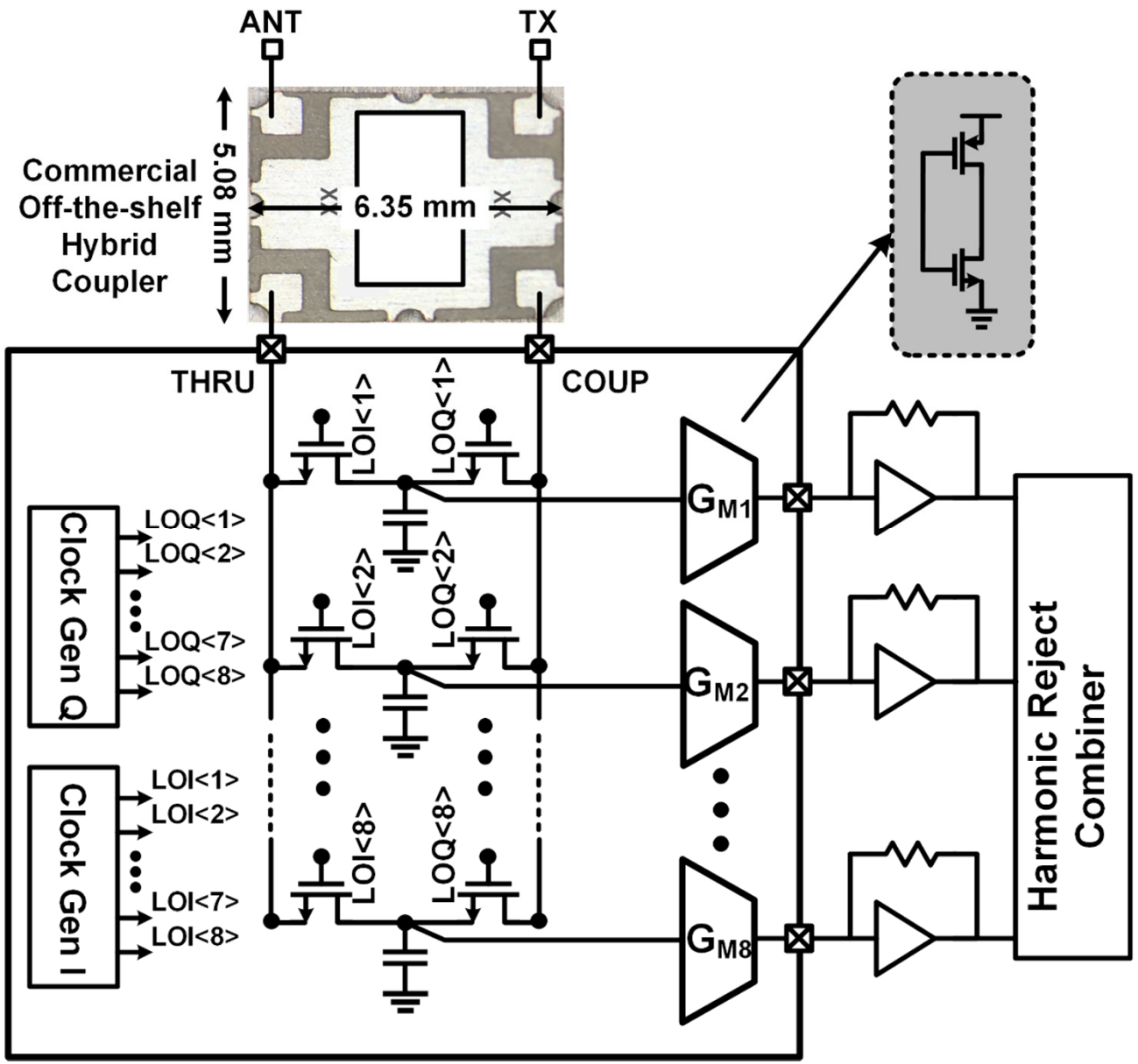

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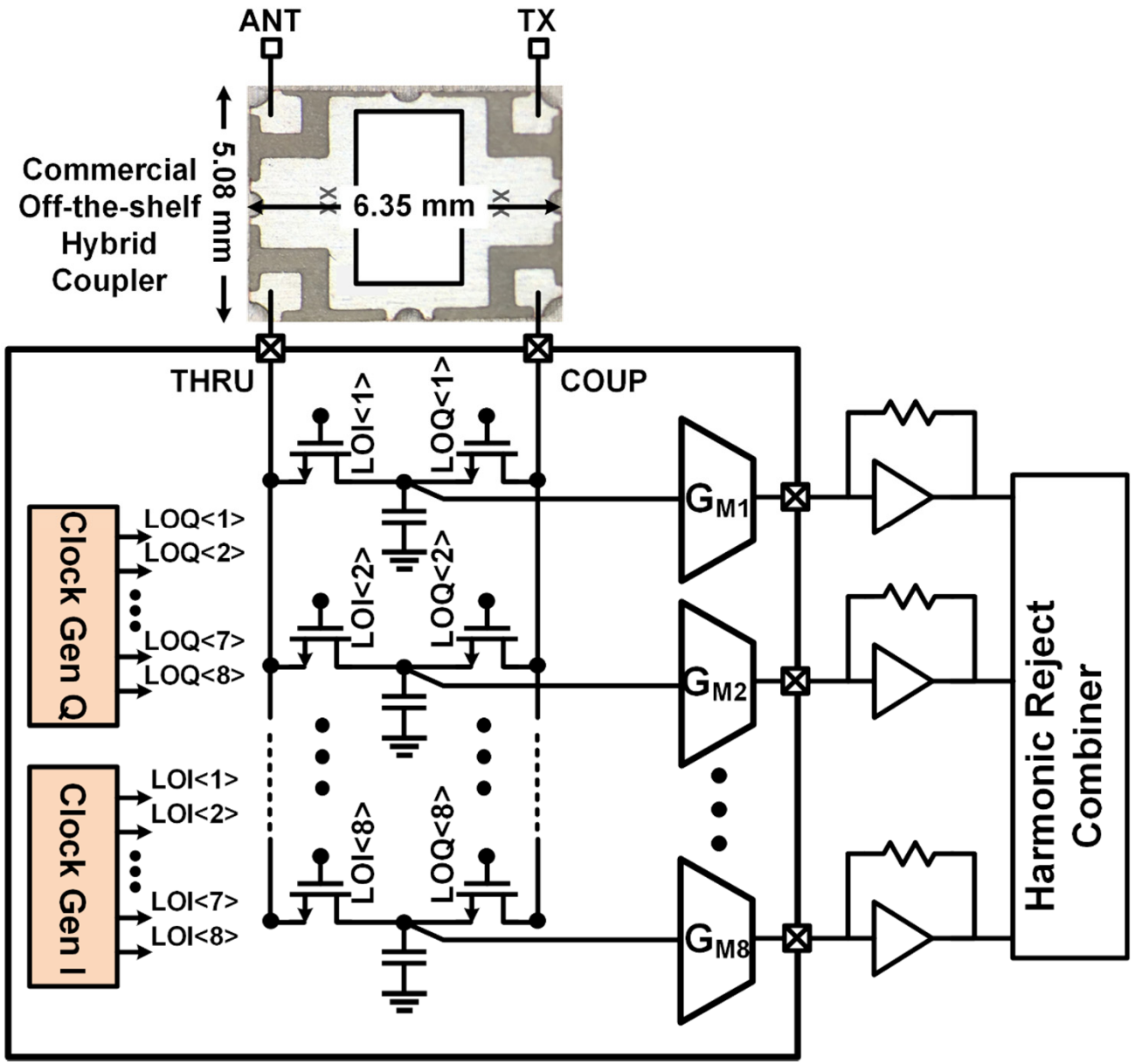
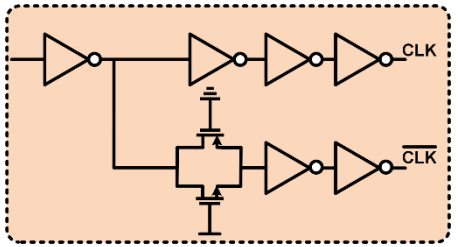
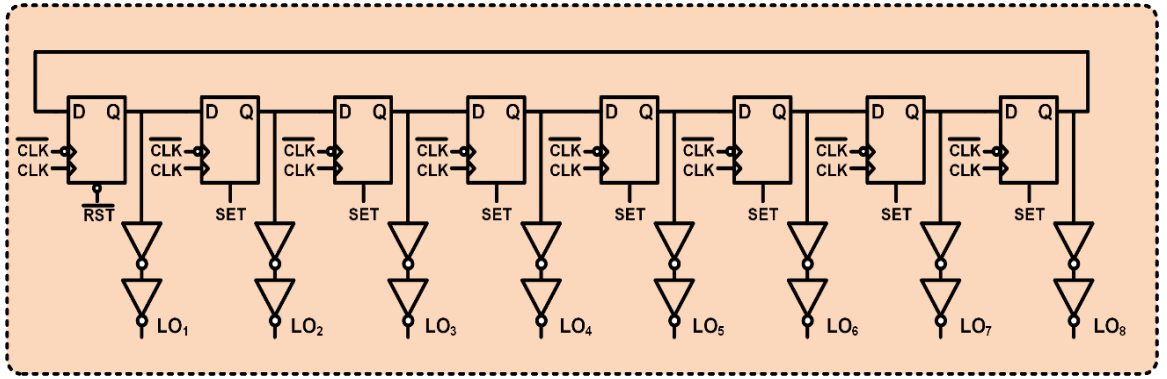
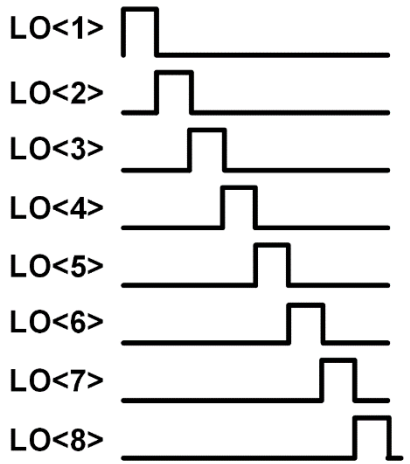
Circulator-RX Implementation in 65-nm CMOS









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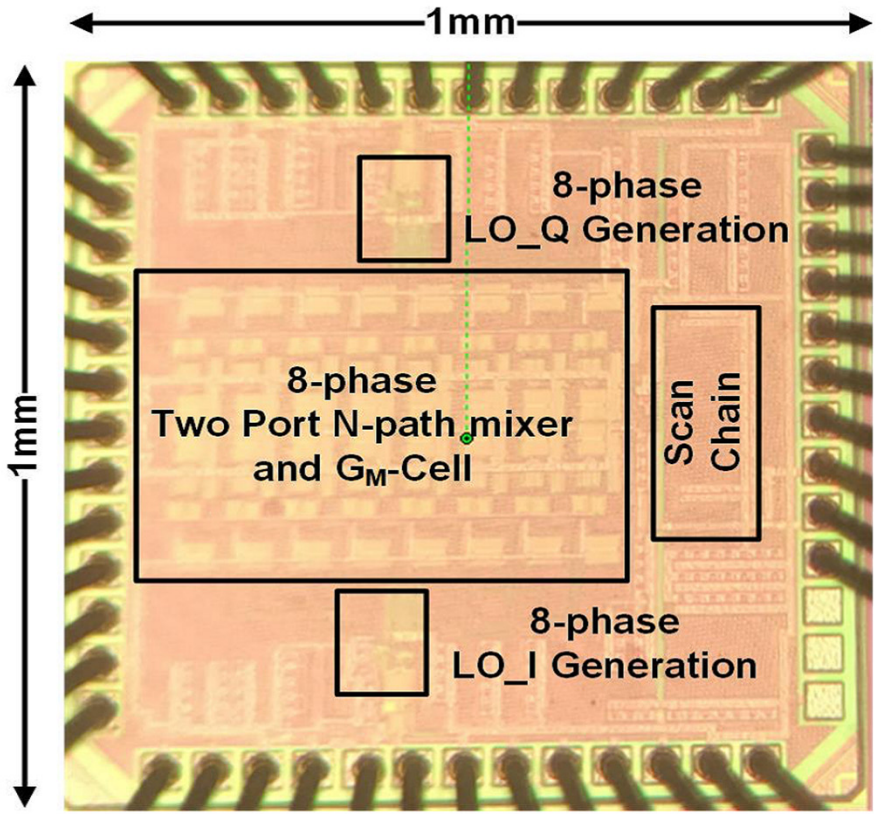
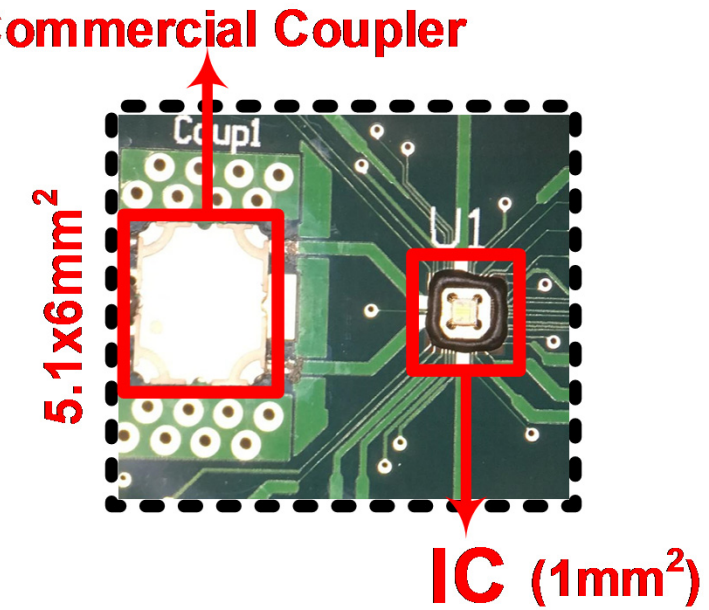
Measurements: Die Photo





- IC implemented in 65-nm CMOS and occupies ~1 mm^2.
- SMD Coupler packaged with IC using chip-on-board approach.

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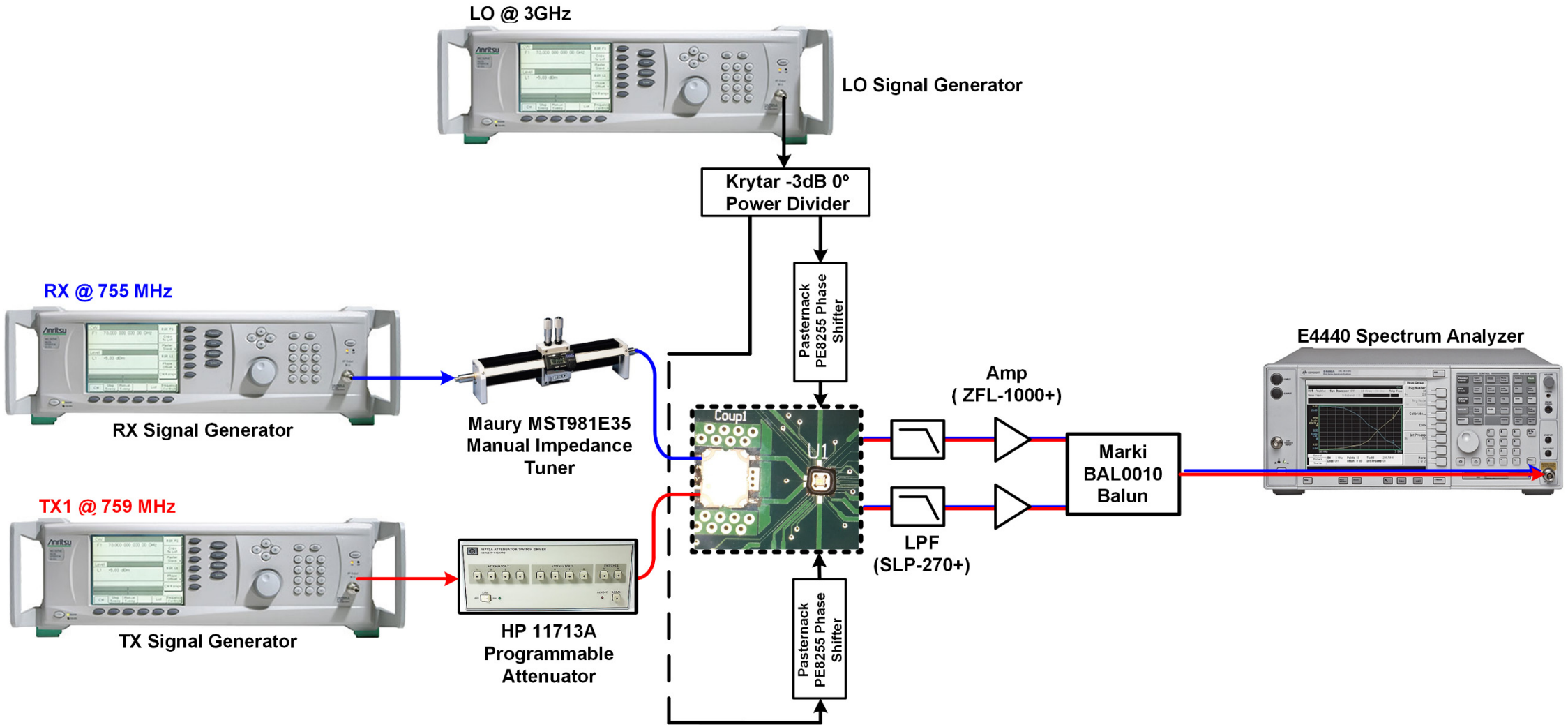
Measurement Setup



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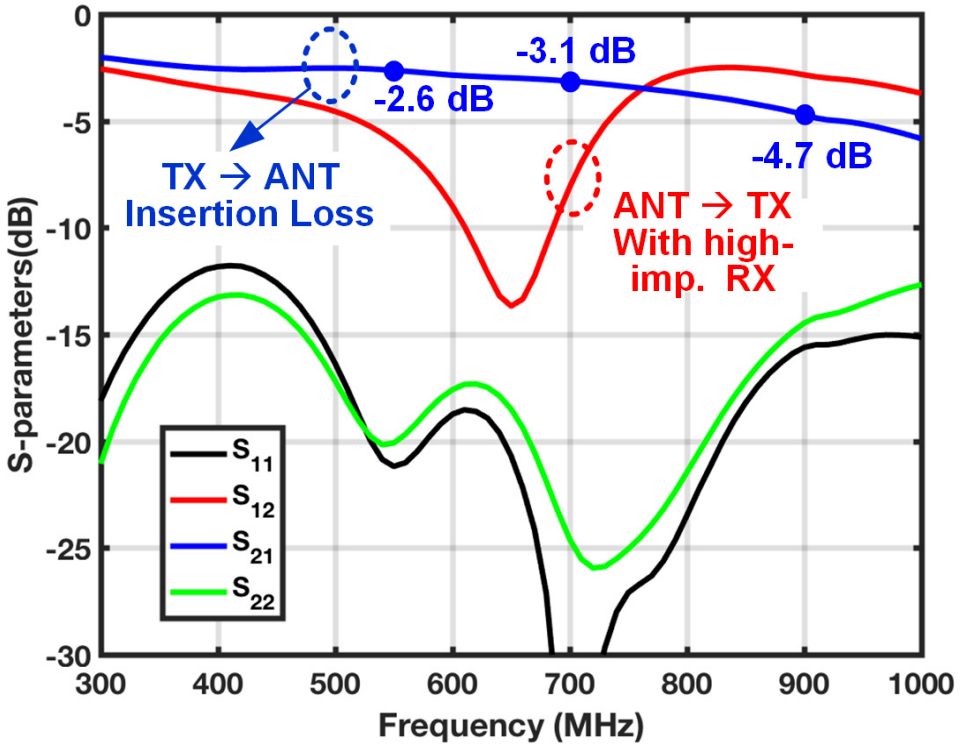
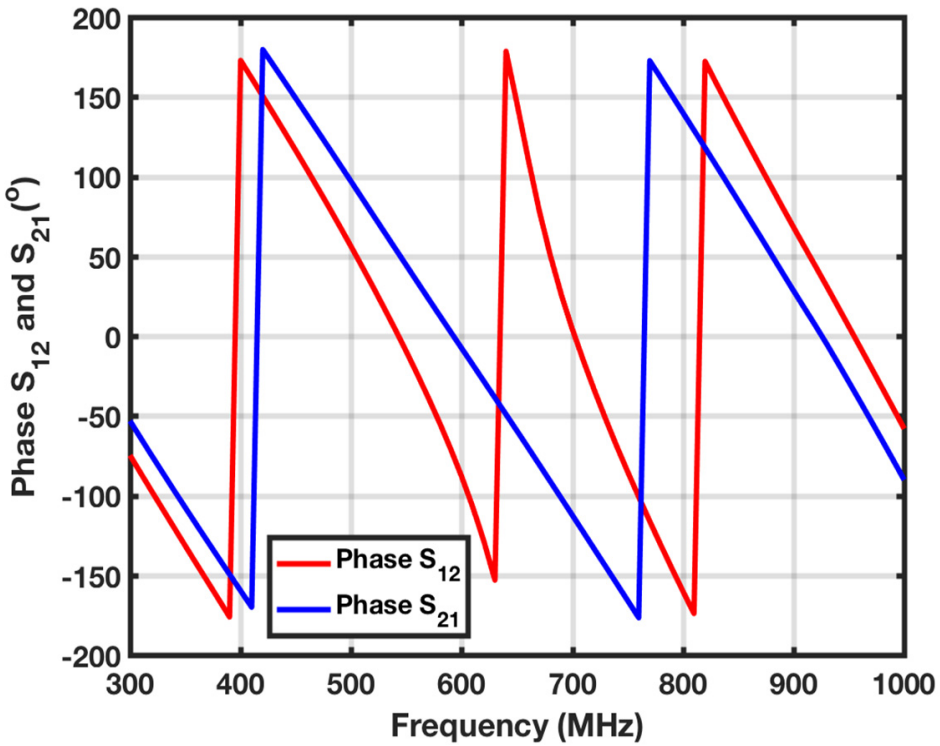
Measurements: Circulator RX S-parameters





- Wideband input match at TX and ANT ports.
- TX to ANT port insertion loss → -2.6dB at 0.5GHz to -4.7dB at 0.9GHz.
- Non-reciprocal behavior → different phases of S12 and S21.

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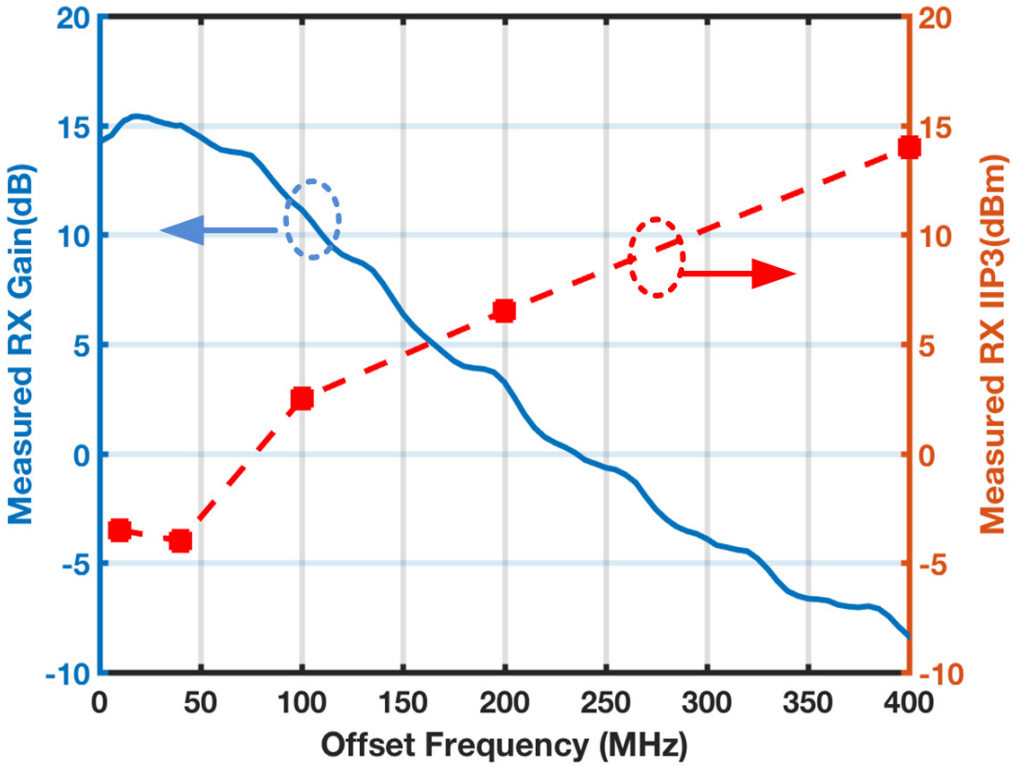
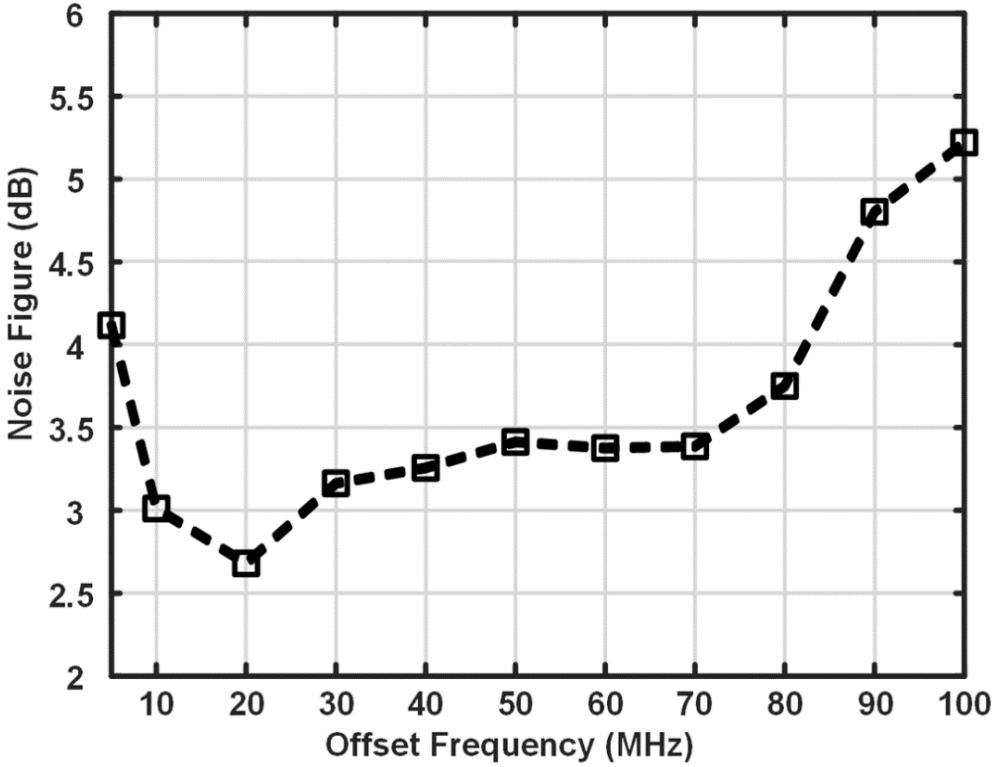
Measurements: RX Gain, IIP3 and NF





- Measured 15dB peak RX gain.
- In-band and out of-band IIP3 demonstrates linearity of passive-mixer first approach.
- Measured *state-of-the-art NF of* **2.7 dB**.

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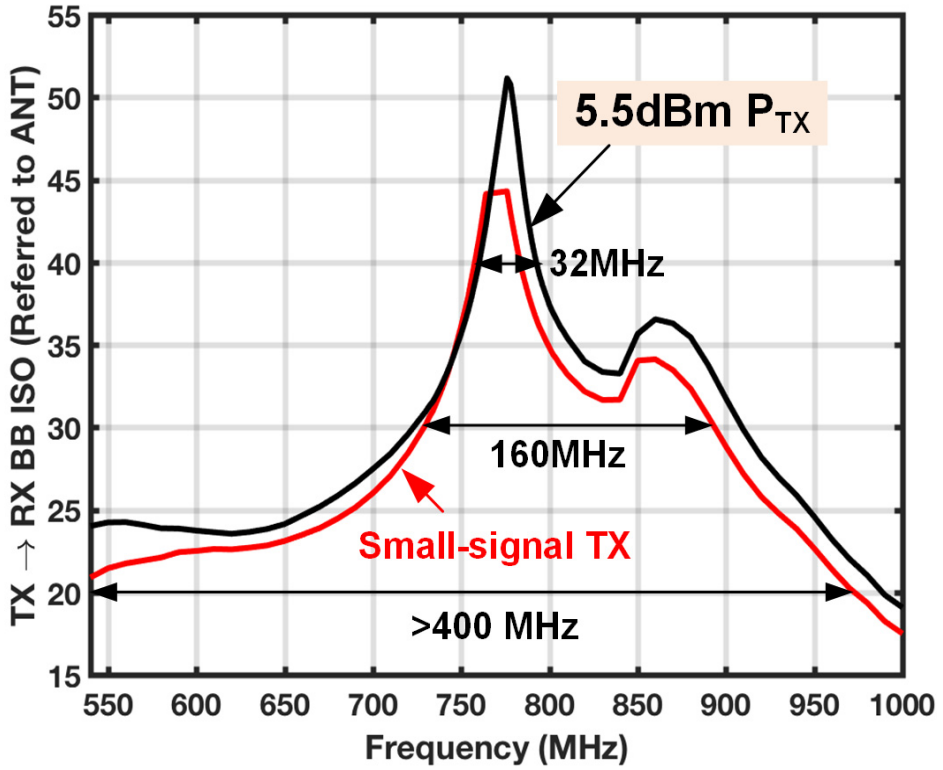
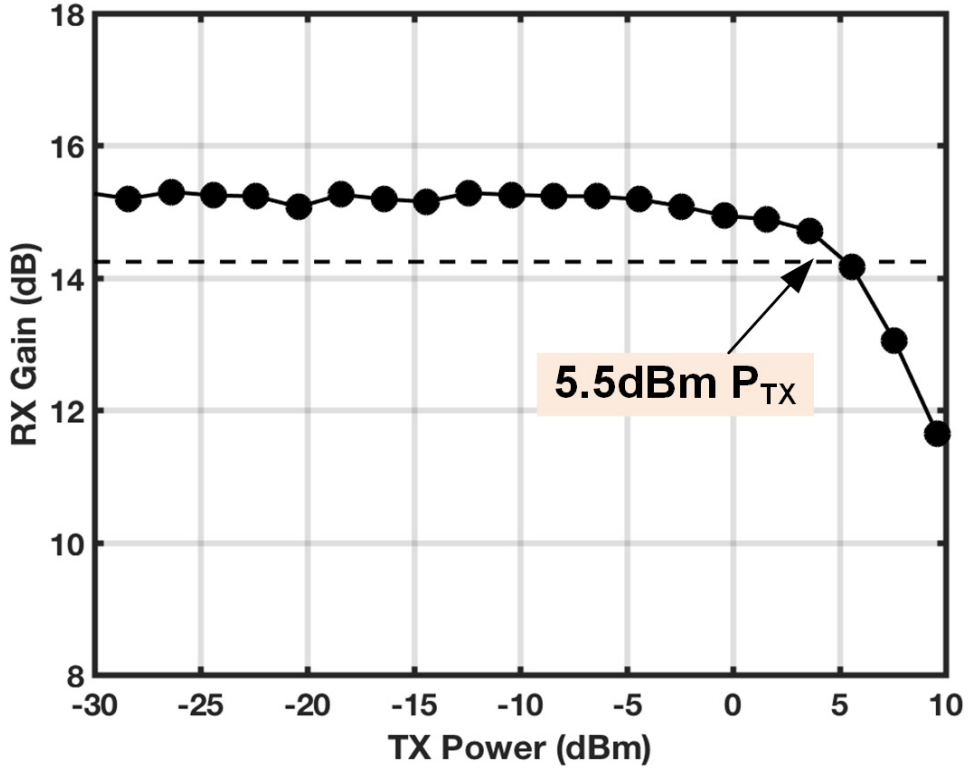
Measurements: SI Cancellation and B1dB





- >50dB peak large-signal TX to BB isolation.
- >400MHz BW for >20dB TX to BB isolation.
- Blocker-1dB tests show +5.5dBm TX power handling.

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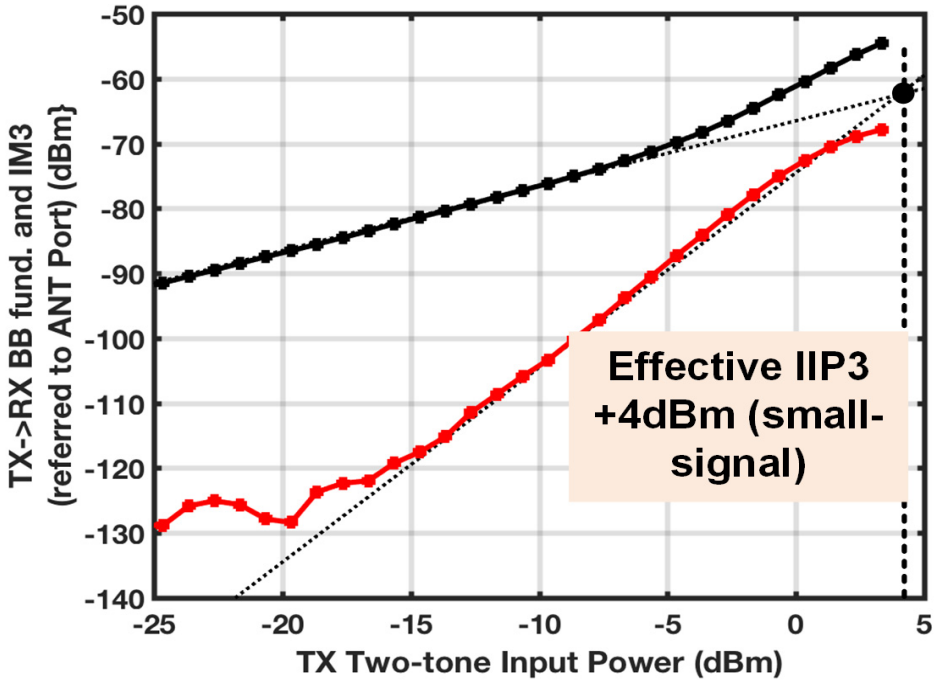
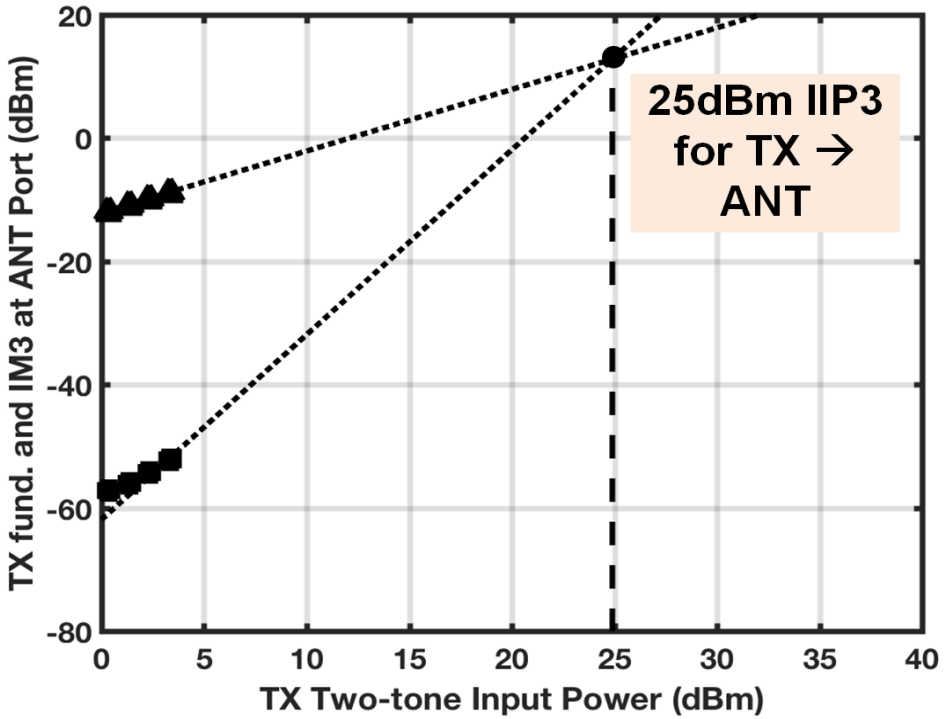
Measurements: Two-tone Linearity w.r.t. TX





- +4dBm IIP3 for two-tone TX input measured at RX BB.
- Two-tone TX → ANT test shows +25dBm IIP3.

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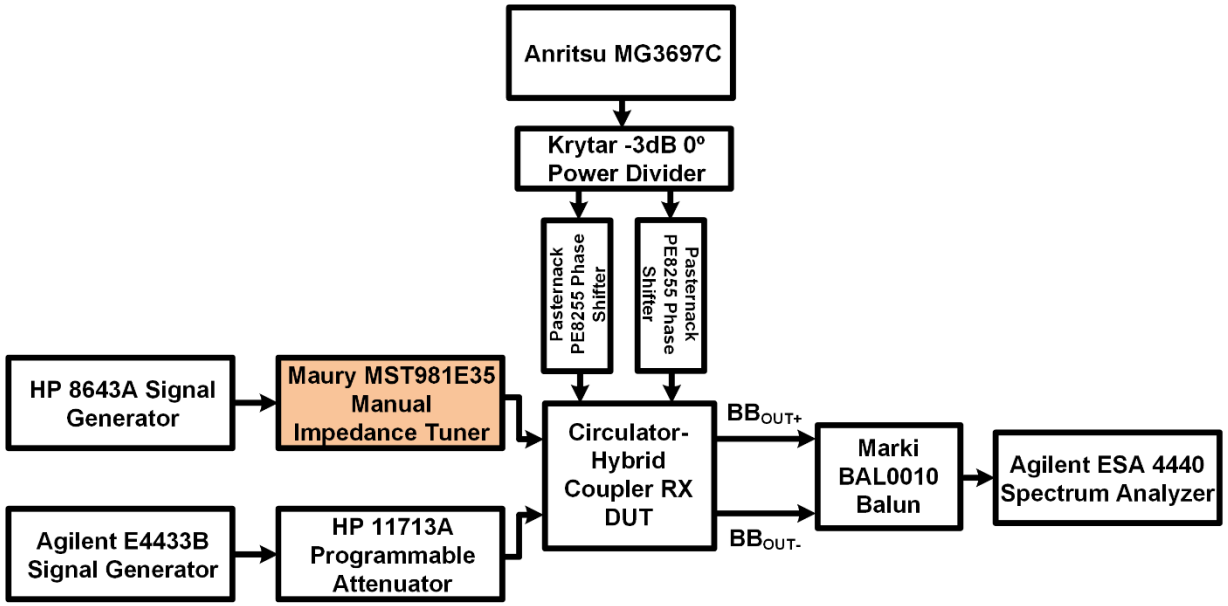
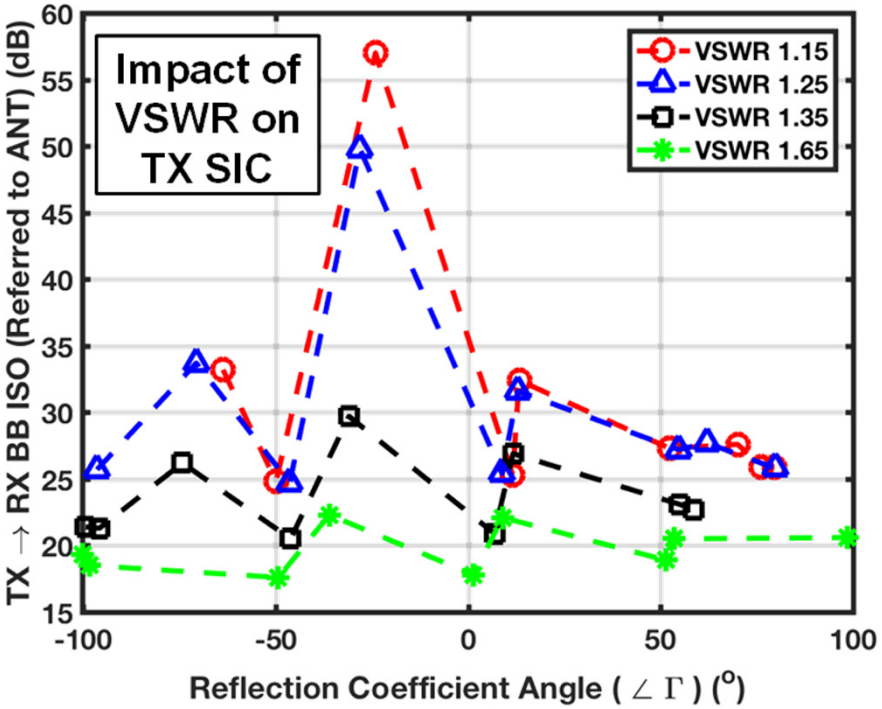
Measurements: TX SIC Vs ANT VSWR





- Impact of ANT port VSWR on TX SIC measured using impedance tuner.
- TX to RX BB peak isolation degraded by >25dB across antenna VSWR.

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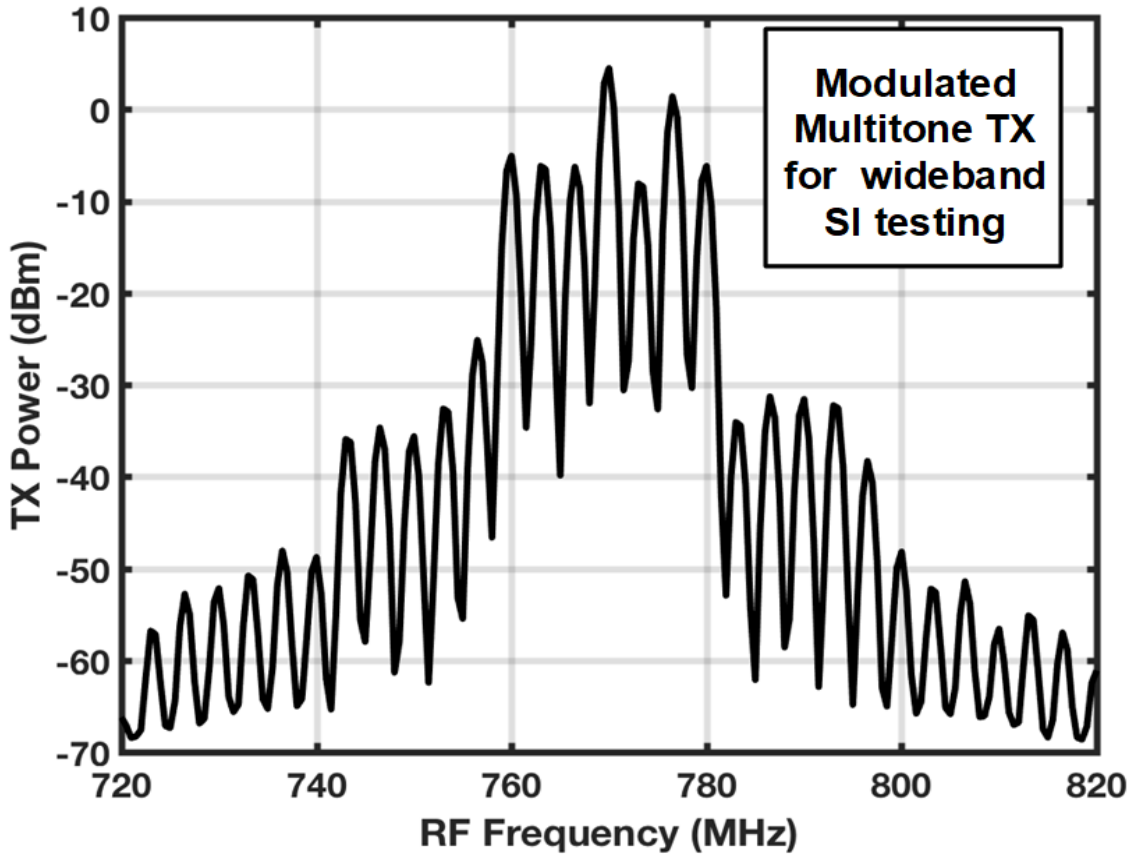
Measurements: Modulated TX SIC



- 20MHz Modulated TX with power of -11.5 to +3.5dBm was fed to DUT.

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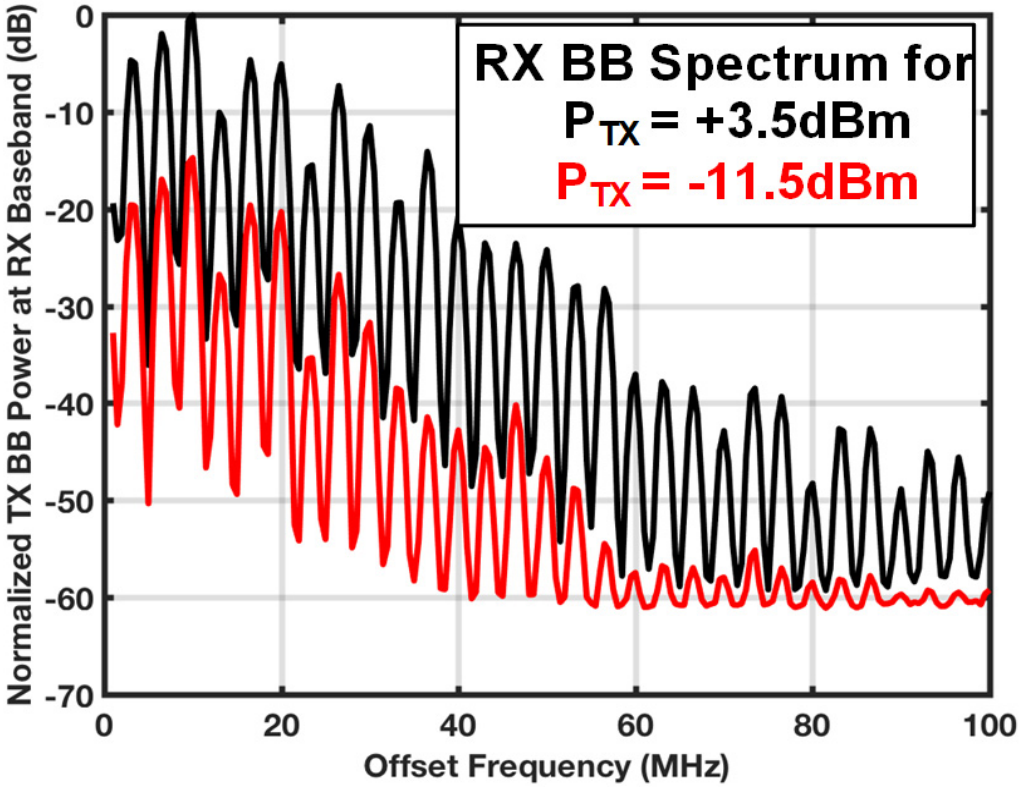
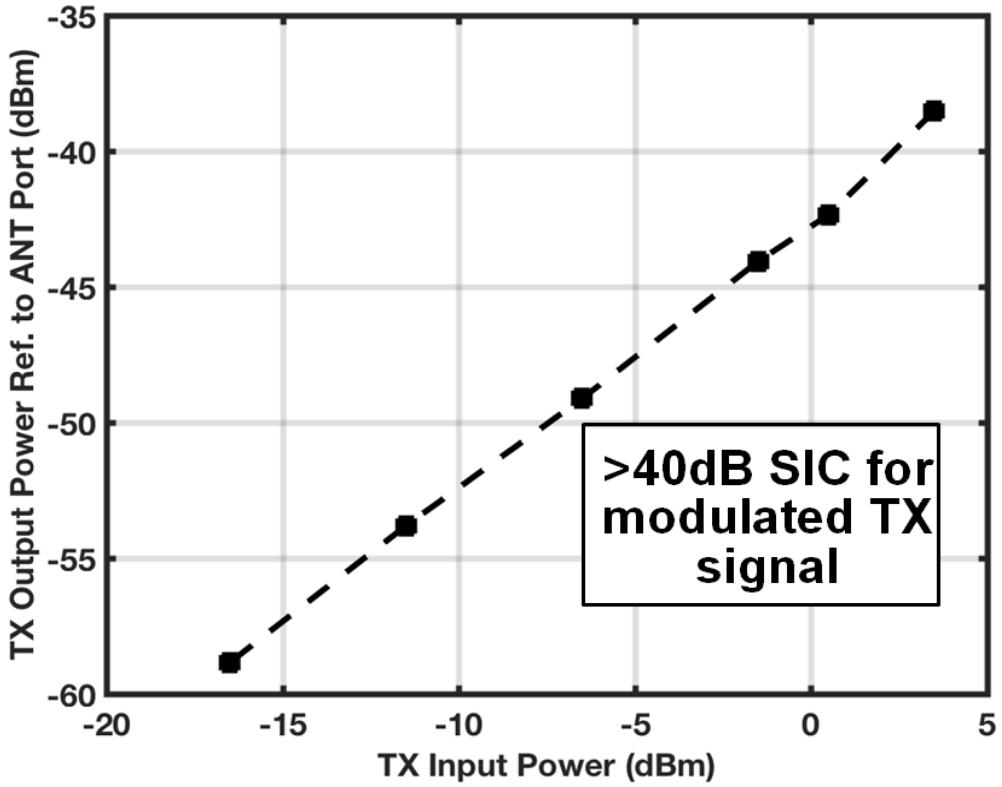
Measurements: Modulated TX SIC





- Wideband TX SIC testing using a modulated multi-tone input.
- ~ Linear increase in SI power for modulated input measured at BB output.
- >40dB TX to BB isolation (ref. to ANT) across modulated TX input powers.

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Measurements: Comparison Table

Specification	This Work	IMS 2017	ISSCC 2017	ISSCC 2017	ISSCC 2016	JSSC 2015
Architecture	Hybrid-Coupler based N-path Circulator RX	Single ended EBD with integrated LNA	T-line based N-path Mixer Circulator RX	Dual Path Adaptive Filter	T-line based N-path Mixer Circulator RX	Mixer-First TRX with Baseband Duplexing
Frequency	0.55-0.9GHz	0.7-1GHz	0.61-0.975GHz	1.7-2.2GHz	0.6-0.8GHz	0.1-1.5GHz
Antenna Interface	Yes	Yes	Yes	No	Yes	Yes
RX Gain (dB)	15dB	7.5-8.8dB	28-43dB	20-35dB	42dB	53dB
RX NF	2.7dB	7.6-8.9dB	6.3dB[h]	4dB	5dB	5-8dB[h]
OOB IIP3	+14dBm	+42dBm	+15.4dBm	NR	+19dBm	+22.5dBm
Analog SIC Domain	RF	RF	RF	RF + BB	RF + BB	BB
RF/Analog SI suppression	40dB ave. SIC across 56MHz BW; >40dB 32MHz BW >30dB 190MHz BW	>50dB across >2MHz[f]	40dB SIC across 20MHz BW[a]	>30dB RF; 40MHz BW >50dB RF, BB; 42MHz BW	42dB SIC across 12MHz BW[a]	33dB across 300KHz TX BW
TX Port Power Handling	+5.5dBm	+24dBm	+7	NR	-7dBm	-17.3
TX → ANT IL	2.6dB @ 550MHz 3.1dB @ 700MHz 4.7dB @ 900MHz	2.6dB to 3.4dB	1.8dB to 3.2dB	NA	1.7dB-3.2dB	NA
Effective IIP3 with respect to TX power	+4dBm small-signal	>+58dBm	-10dBm small-signal	NR; canceller IIP3 26.5dBm[b]	+1dBm at 42dB gain	0dBm at 43/53dB gain
RX + SIC Power	25mW[g]	12mW	72mW[d]	33.5mW	100mW[e]	43-56mW incl. TX
Antenna Interface Power	24mW	N/A	36mW[c] at 0.7GHz	N/A	59mW[c] at 0.7GHz	RX power incl. interface
Technology	65-nm CMOS	0.18-µm SOI	65-nm CMOS	40-nm CMOS	65-nm CMOS	65-nm CMOS

[a]additional digital SI cancellation also demonstrated; [b]linearity of canceller reported; IIP3 with respect to TX at BB not reported; [c]includes on-chip phase control, [d] includes two-stage baseband amplification; [e] includes BB canceller ; [f] with respect to the EBD; [g] uses external I/Q splitters; [h]full-duplex NF

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Conclusions and Future Work

- A wideband hybrid-coupler circulator-RX approach is presented that can achieve TX → ANT insertion loss and wideband cancellation.
- The approach preserves passive-mixer first in-band and out-of-band linearity while achieving low noise.
- A 65-nm CMOS prototype is presented that achieves <3dB NF with 40 dB average TX to RX BB isolation over 56MHz bandwidth.

- Future work includes incorporation of balance network in hybrid coupler to mitigate impact of TX and antenna port mismatch

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Acknowledgements

- This work is supported by the DARPA Arrays at Commercial Timescales (ACT) Program and the NSF CAREER Award (NSF Award No. 1554720).

- Dr. Roy (Troy) Ollson and Dr. Ben Epstein, DARPA for valuable technical discussions.

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A 62-to-68GHz Linear 6Gb/s 64QAM CMOS Doherty Radiator with 27.5%/20.1% PAE at Peak/6dB-Back-off Output Power Leveraging High-Efficiency Multi-Feed Antenna-Based Active Load Modulation

Huy Thong Nguyen, Taiyun Chi, Sensen Li, Hua Wang

Georgia Institute of Technology

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Outline

- Introduction
- Multi-Feed Antenna-Based Doherty Output Network
- Design of a 62-to-68GHz Linear CMOS Doherty Radiator
- Measurement Results
- Conclusion

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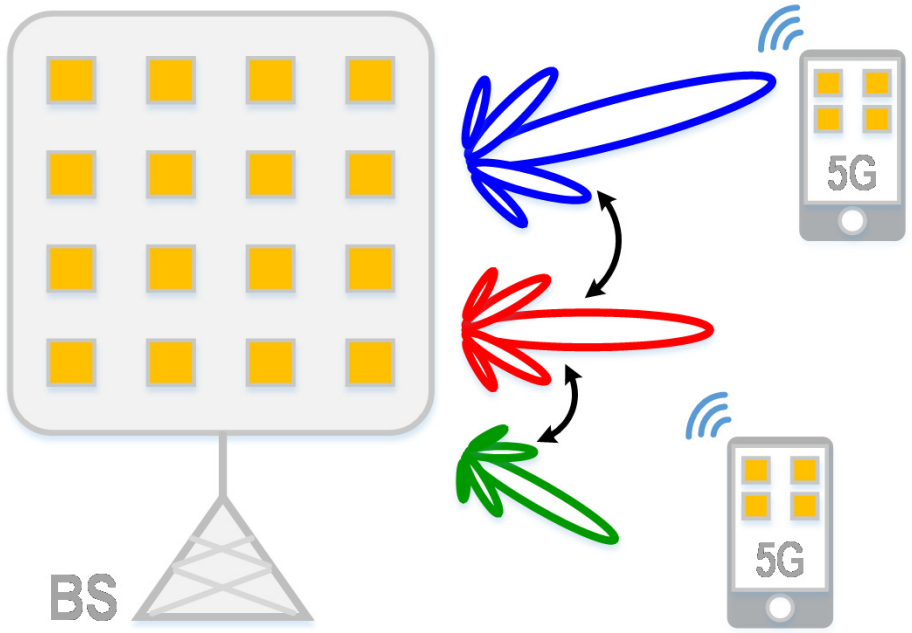
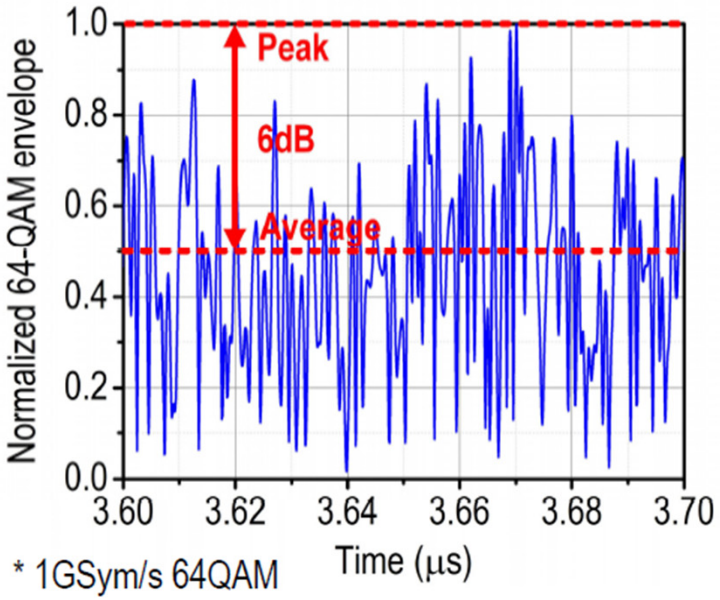
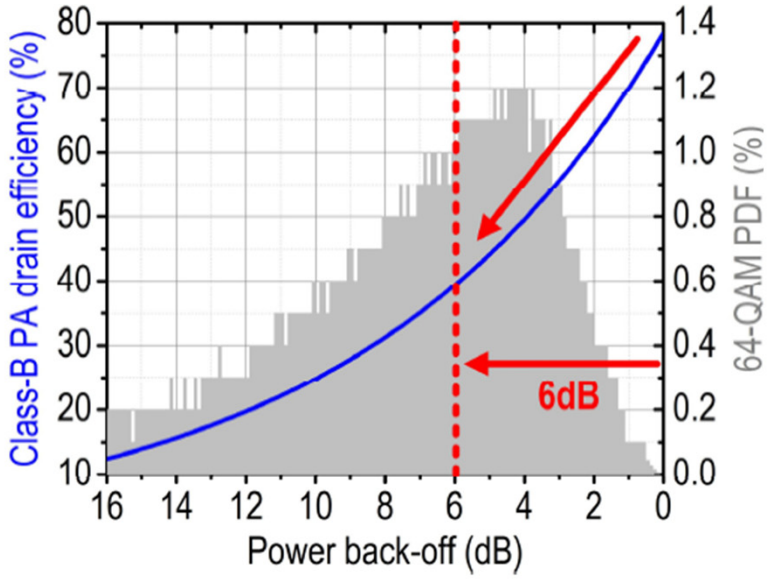
Introduction

- **Radiators in 5G massive MIMO systems transmit spectrum-efficient modulated signals with large PAPR**

→ Overall system's efficiency largely depends on the efficiency of Power Amplifier at Power Back-Off (PBO)







[S.Hu ISSCC' 17]

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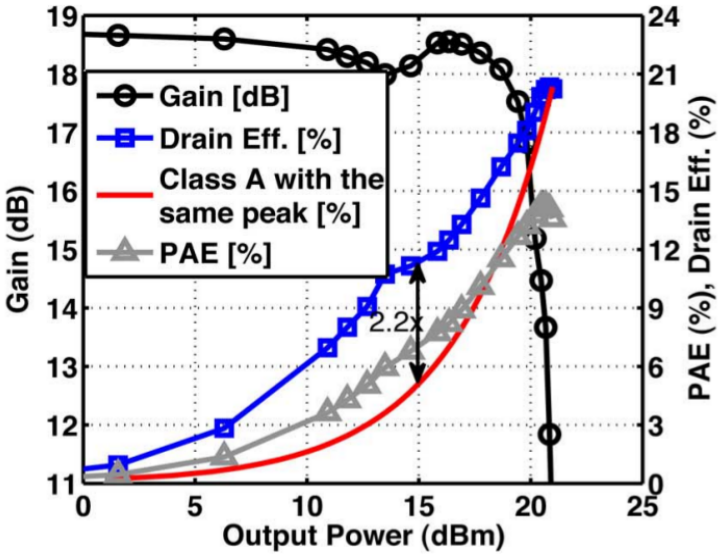
State-of-the-Art of Doherty PA at 60-80GHz

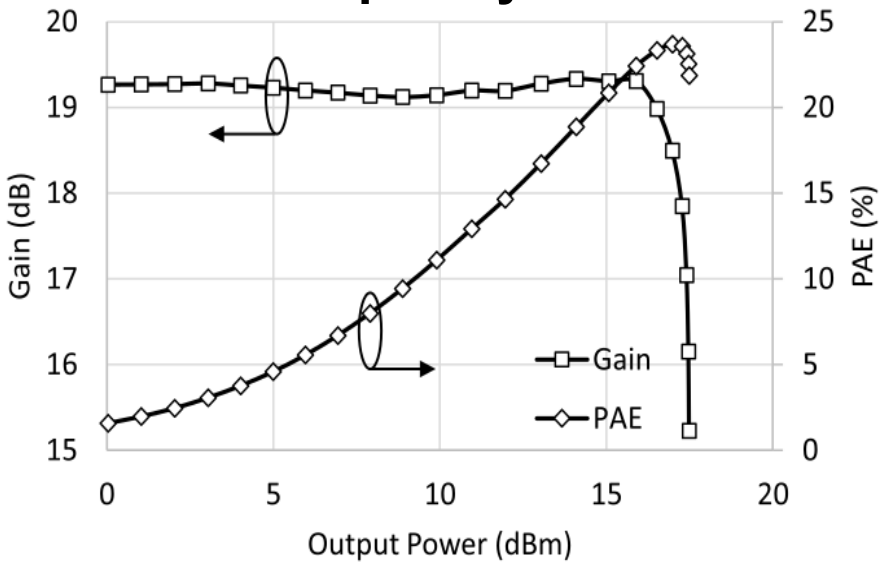
- Doherty is one of the commonly-used techniques for PBO efficiency enhancement

Carrier Frequency = 72GHz



[Kaymaksut TMTT'15]

Carrier Frequency = 62GHz



[Greene JSSC'17]

- Reported Doherty PAs at 60-80GHz exhibit marginal PAE enhancements at 6dB PBO compared to an idealistic class-B PA
  (due to inefficient Doherty output network and imperfect Main/Aux. cooperation)

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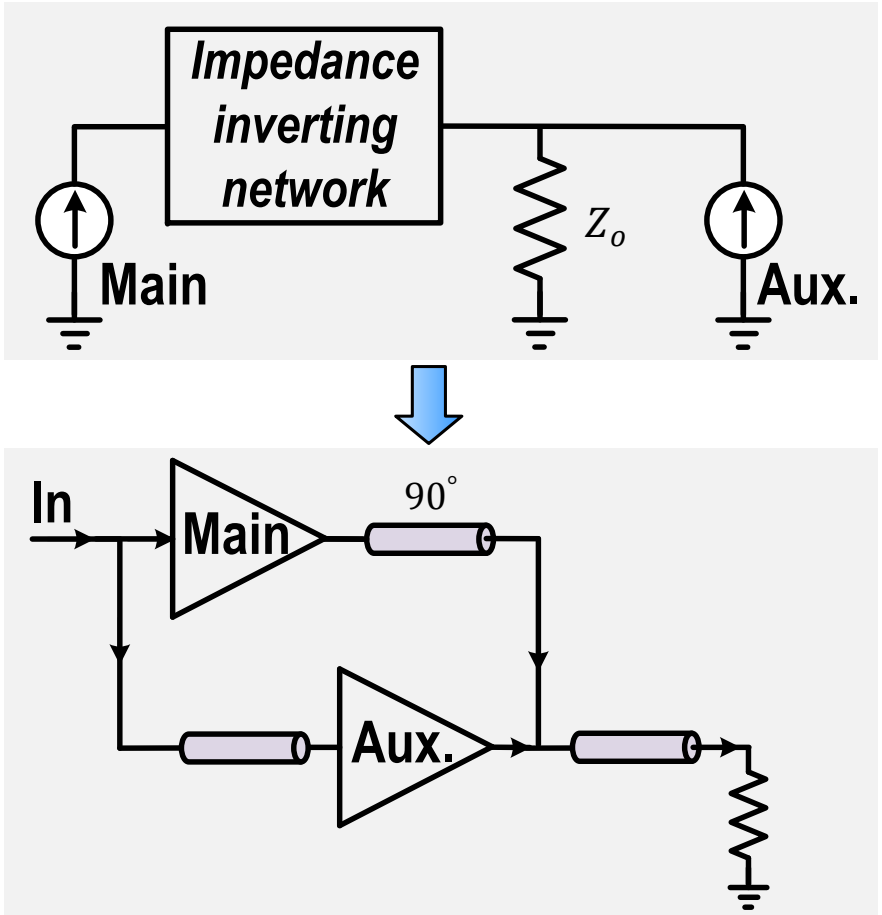
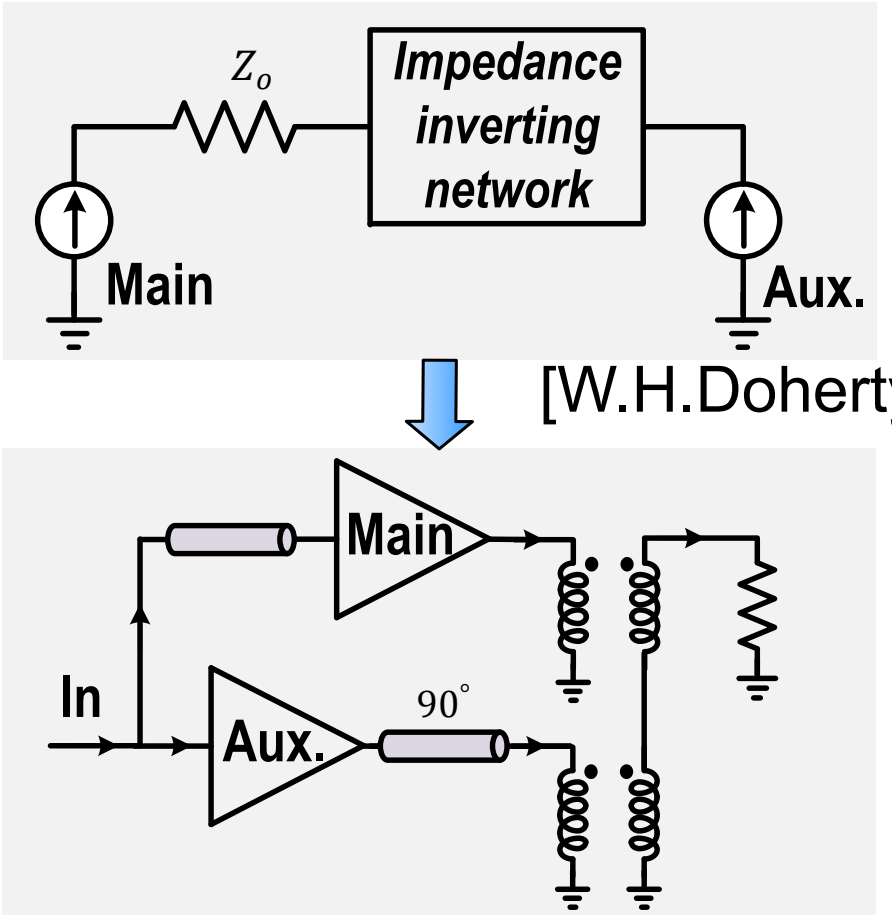
Doherty Architectures

Doherty network for parallel combiner



Doherty network for series combiner



[W.H.Doherty IRE' 1936]

- Two Doherty structures for parallel and series power combiner

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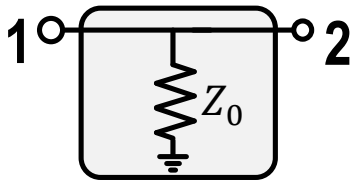
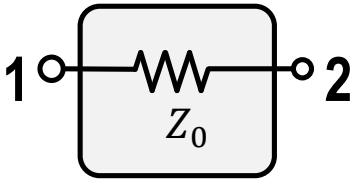
Parallel vs Series Combiner

- Parallel power combiner intrinsically scales up the impedance

- Series power combiner naturally scales down the load

→ appealing for high-power PAs in voltage-limited Si processes

	Circuit Realization	Matrix form	Relationship	Load Modulation	
				6dB PBO	0dB PBO
Parallel Combiner		$[Z] = \begin{bmatrix} Z_0 & Z_0 \\ Z_0 & Z_0 \end{bmatrix}$	$V_1 = V_2$	$Z_1 = Z_0$ Z_2 = open	$Z_1 = 2Z_0$ $Z_2 = 2Z_0$
Series Combiner		$[Y] = \begin{bmatrix} Y_0 & Y_0 \\ Y_0 & Y_0 \end{bmatrix}$	$I_1 = I_2$	$Z_1 = Z_0$ Z_2 = short	$Z_1 = Z_0/2$ $Z_2 = Z_0/2$

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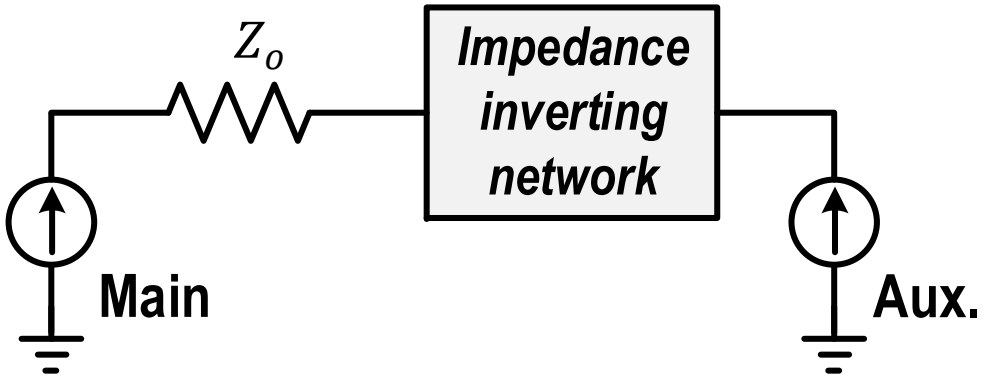
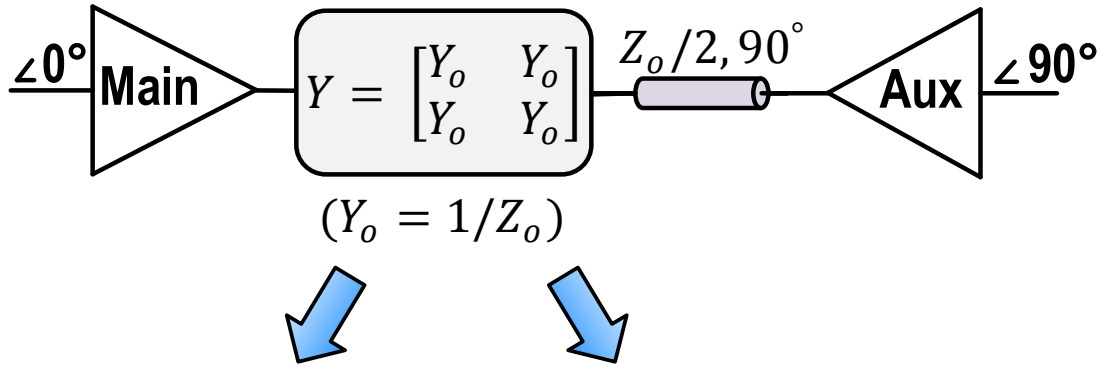
Series Combiner Doherty

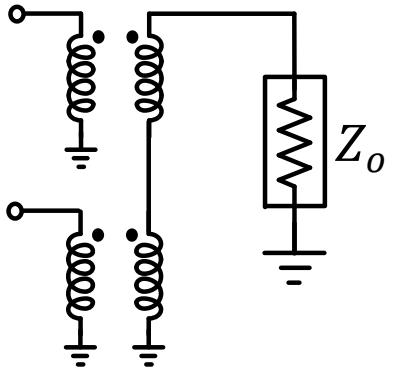




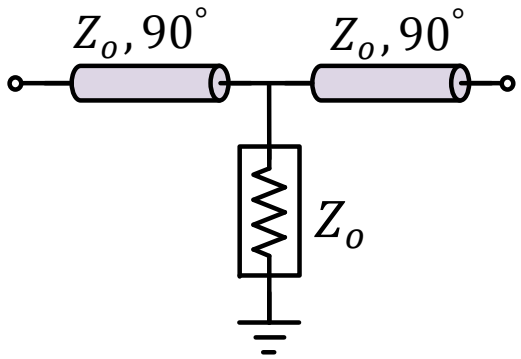
- Transformer series combiner:
  - compromised performance
  - degraded balancing

  (due to strong coil-coil capacitive coupling)

- T-line implementation:
  - area-consuming
  - cannot easily support differential PAs



Transformer-based implementation



T-line based implementation

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On-chip Antenna

- The size of antenna is comparable to the size of active circuits at mm-wave frequency (60-80GHz), and implementation of antenna on chip is practical

- We exploit on-chip antenna as a part of Doherty output network (or antenna as a signal processing unit in the front-end circuits)

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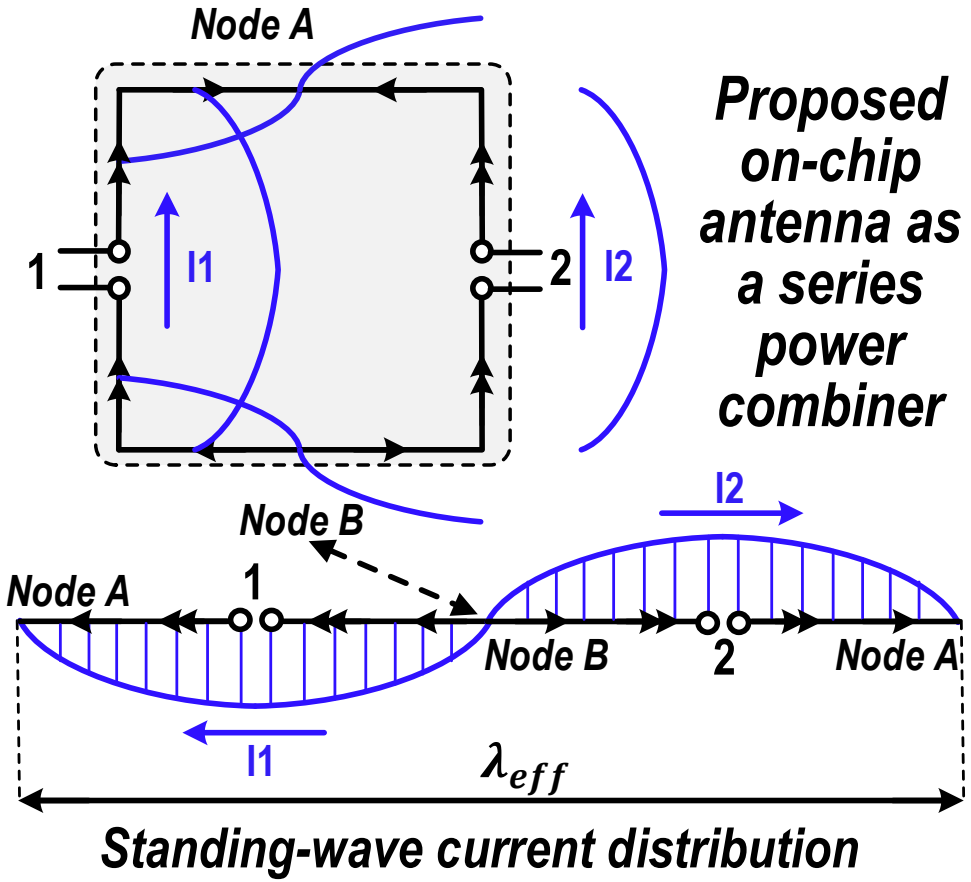
Proposed Series Combiner

- To construct the series combiner, we explore a multi-feed structure on a one-λ wire loop antenna



- Current peaks at feeds 1 and 2 *(same magnitude and phase)*
- Current nulls at nodes A & B

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Proposed Series Combiner

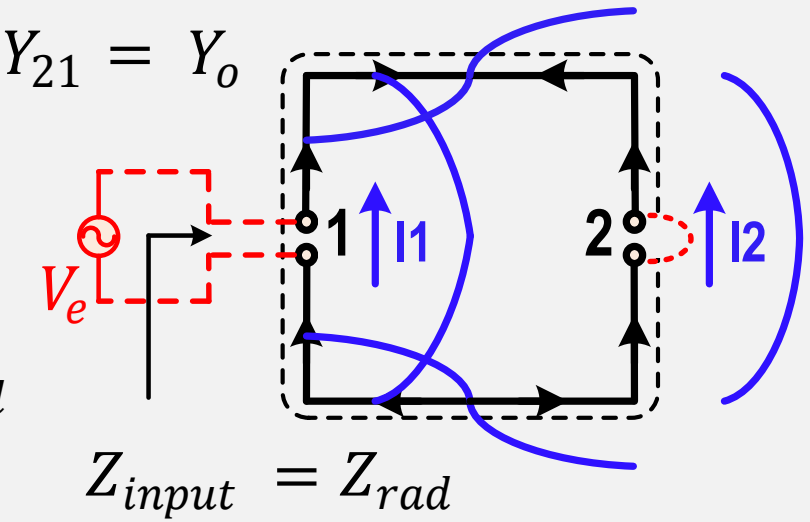
- Theoretical [Y] matrix of this structure is identical to that of a series combiner

$$I_1 = V_e/Z_{rad} = Y_o V_e \rightarrow Y_{11} = Y_o$$

$$I_2 = I_1 = Y_o V_e \rightarrow Y_{21} = Y_o$$

$$Y = \begin{bmatrix} Y_o & Y_o \\ Y_o & Y_o \end{bmatrix}$$

$$where\ Y_o = 1/Z_{rad}$$



$$Z_{input} = Z_{rad}$$

In a single antenna footprint, we construct both ***an antenna*** and ***a differential series power combiner***

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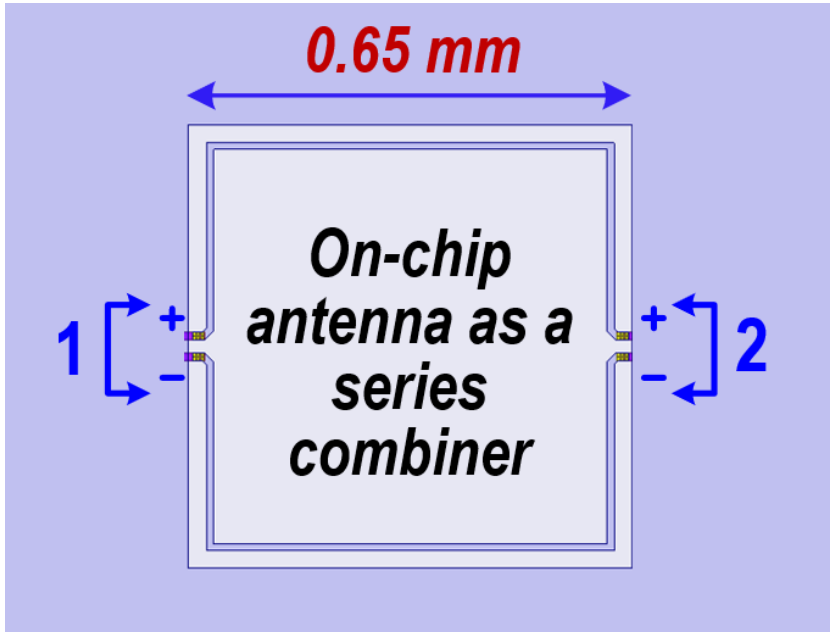
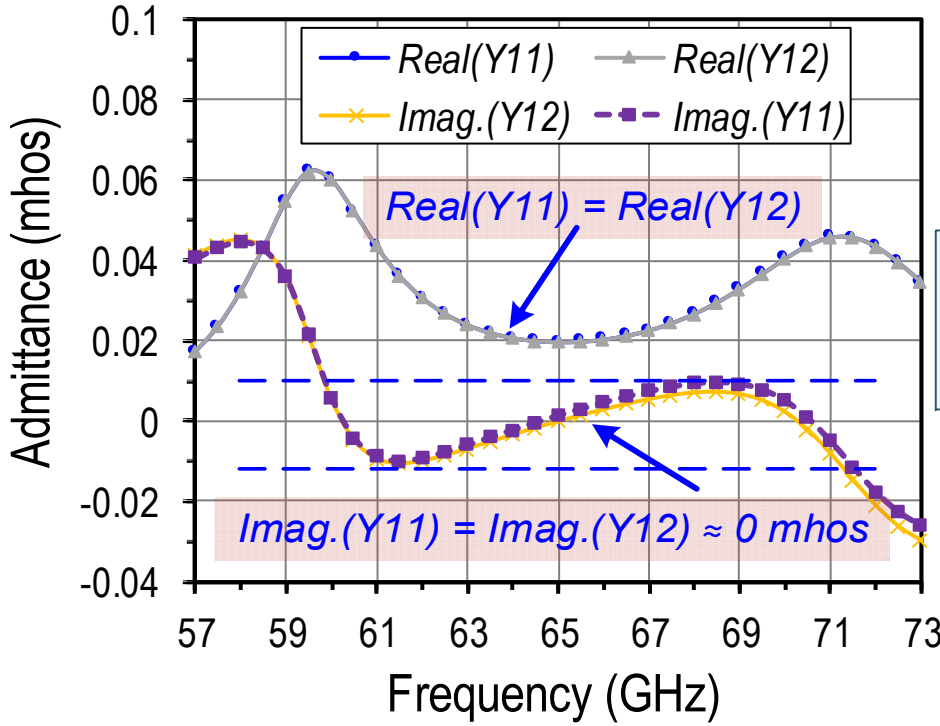
Proposed Series Combiner

- We shape the antenna ground to increase its instantaneous bandwidth, which helps exhibit double resonance [Chi ISSCC'18]





$\text{Real}(Y_{11}) = \text{Real}(Y_{21})$
$\text{Imag.}(Y_{11}) = \text{Imag.}(Y_{12})$

- Simulated [Y] matrix of proposed structure is *identical to that of an ideal series combiner* over entire antenna's bandwidth

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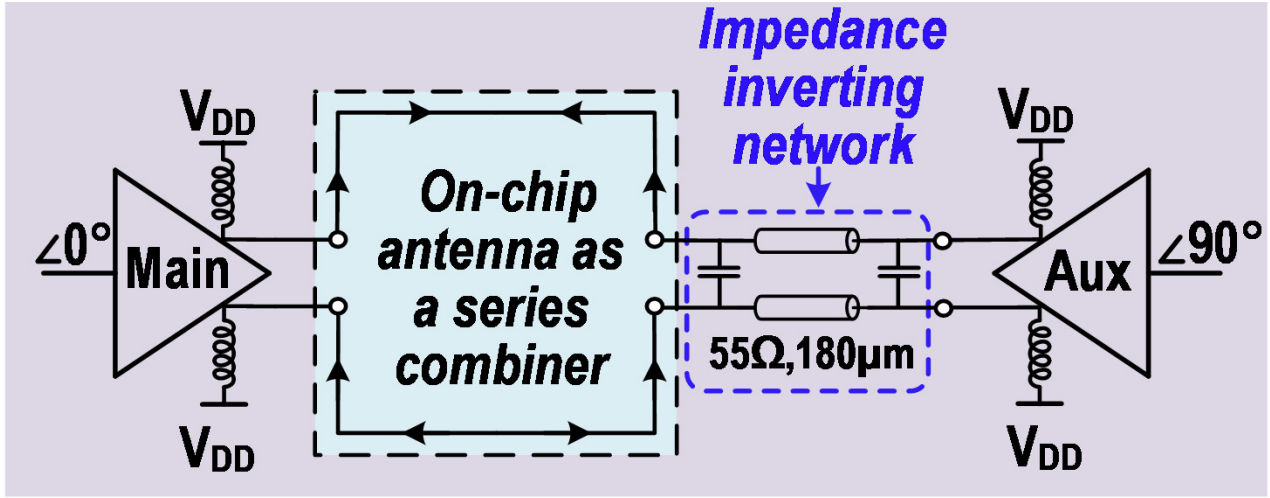
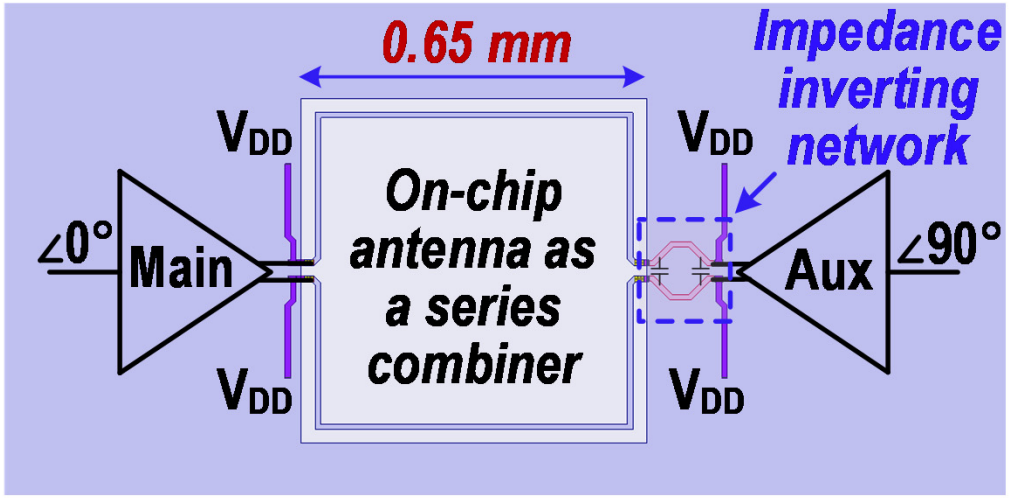
Doherty Radiator Network

Schematic of Doherty PA output stage



EM model of Doherty PA output network



- λ/4 impedance inverting network is added at Aux. path to construct the Doherty output network
  - ➢ Impedance inverting network is designed as a capacitively-loaded T-line
  - ➢ T-line length is only 35° for size reduction

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Doherty Radiator Network

➢ Low-loss power combiner

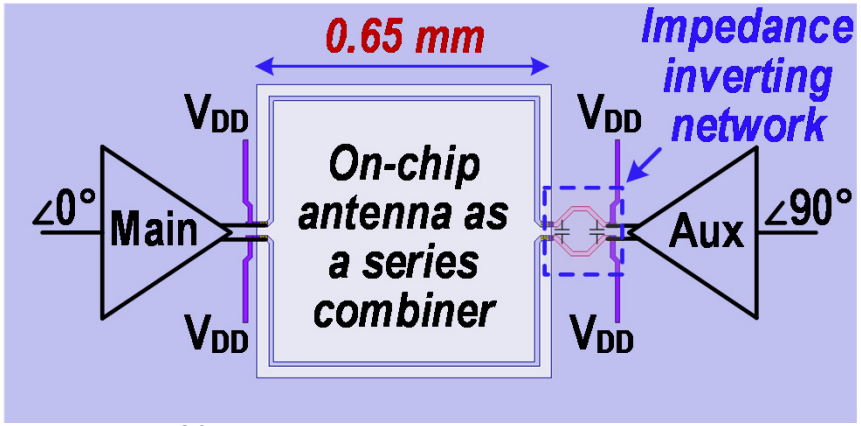
(On-antenna power combiner is typically less lossy than conventional power combiner techniques)

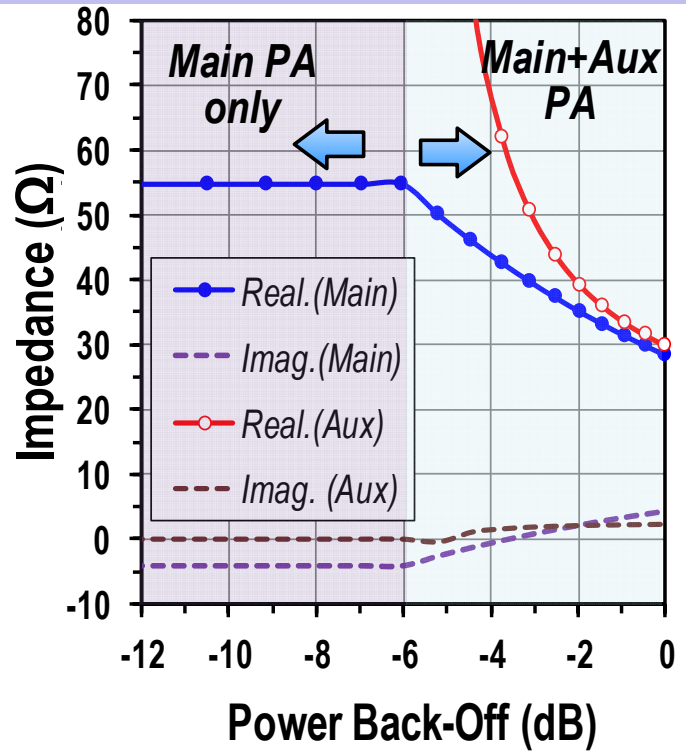
➢ Reduce on-chip passive networks

(Implementation of differential series combiner is now merged inside the antenna design)

➢ Excellent signal-processing accuracy

- ✓ Theoretically perfect combiner of differential signals (due to theoretically perfect symmetry)
- ✓ [Y] matrix implies a close-to-ideal differential series combiner
- ✓ ***Overall, we achieve a close-to-ideal Doherty active load modulation behavior***





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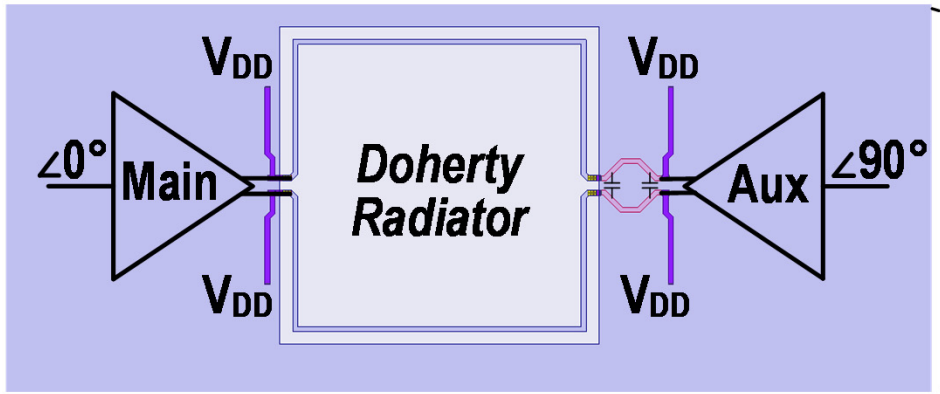
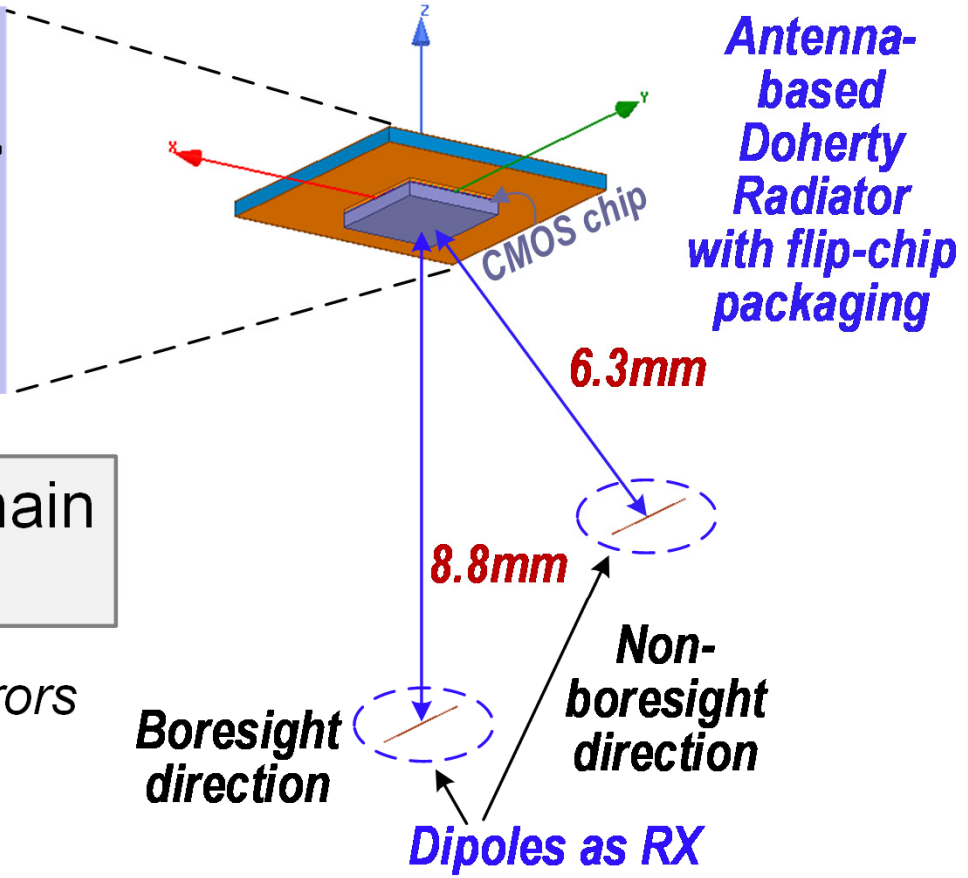
Far-Field Transmission

The loads are now receivers at far-field

Driving condition of the antenna changes:

- The Main/Aux. power ratio varies in the Doherty operation





Radiation pattern/gain of antenna must remain the same during the Doherty operation

(Otherwise, spatially dependent AM-AM/AM-PM errors will corrupt the transmitted modulations)

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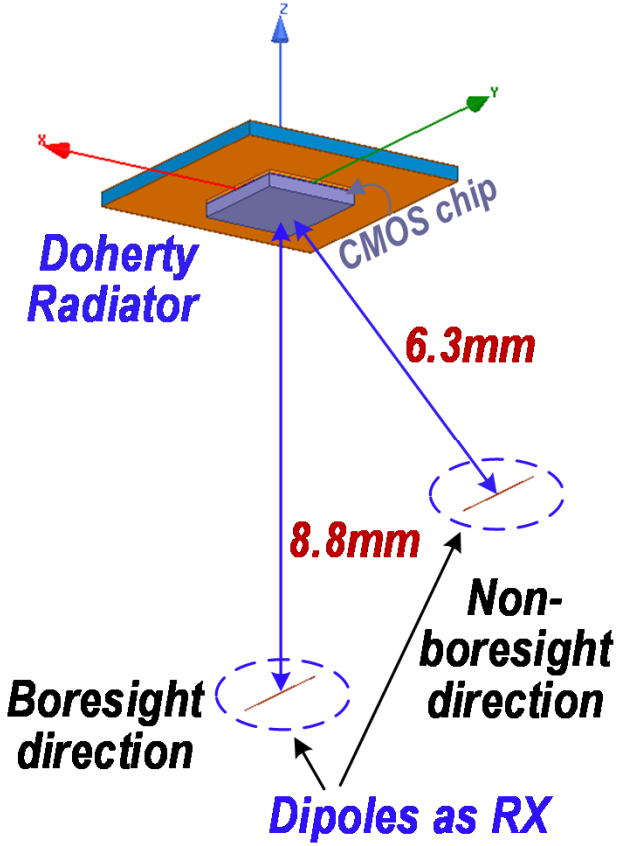
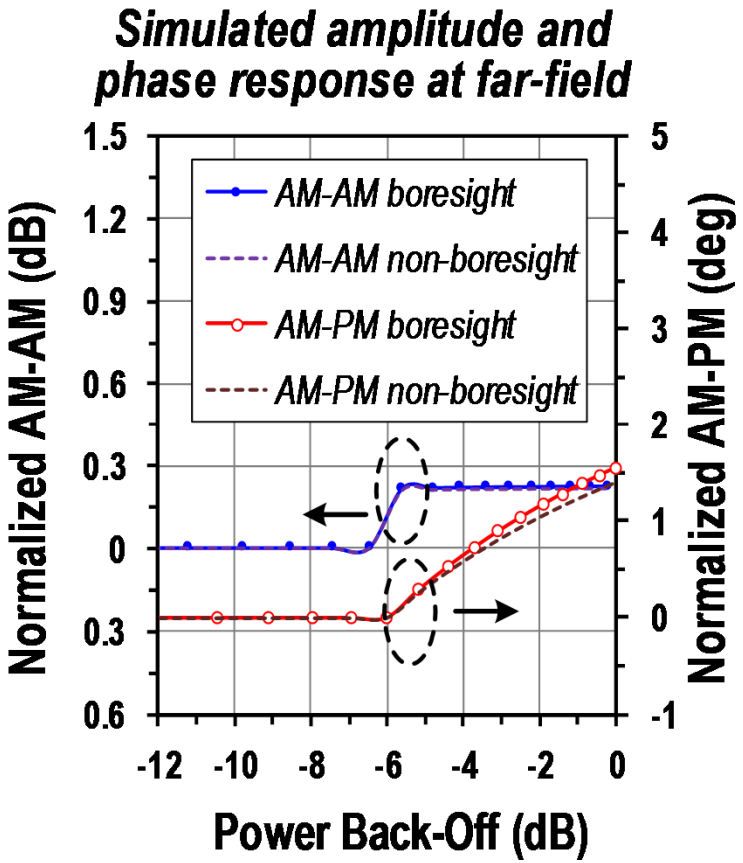
Far-Field Transmission

We set up a simulation to mimic a full communication system:

- Doherty Radiator – TX
- Dipoles in far field – RX





Assume Main and Aux. PAs follow an idealistic class-B operation (perfectly linear PAs):

✓ <0.2dB AM-AM & <1.5° AM-PM variation is observed at far-field

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Outline

- Introduction
- Multi-Feed Antenna-Based Doherty Output Network
- Design of a 62-to-68GHz Linear CMOS Doherty Radiator
- Measurement Results
- Conclusion

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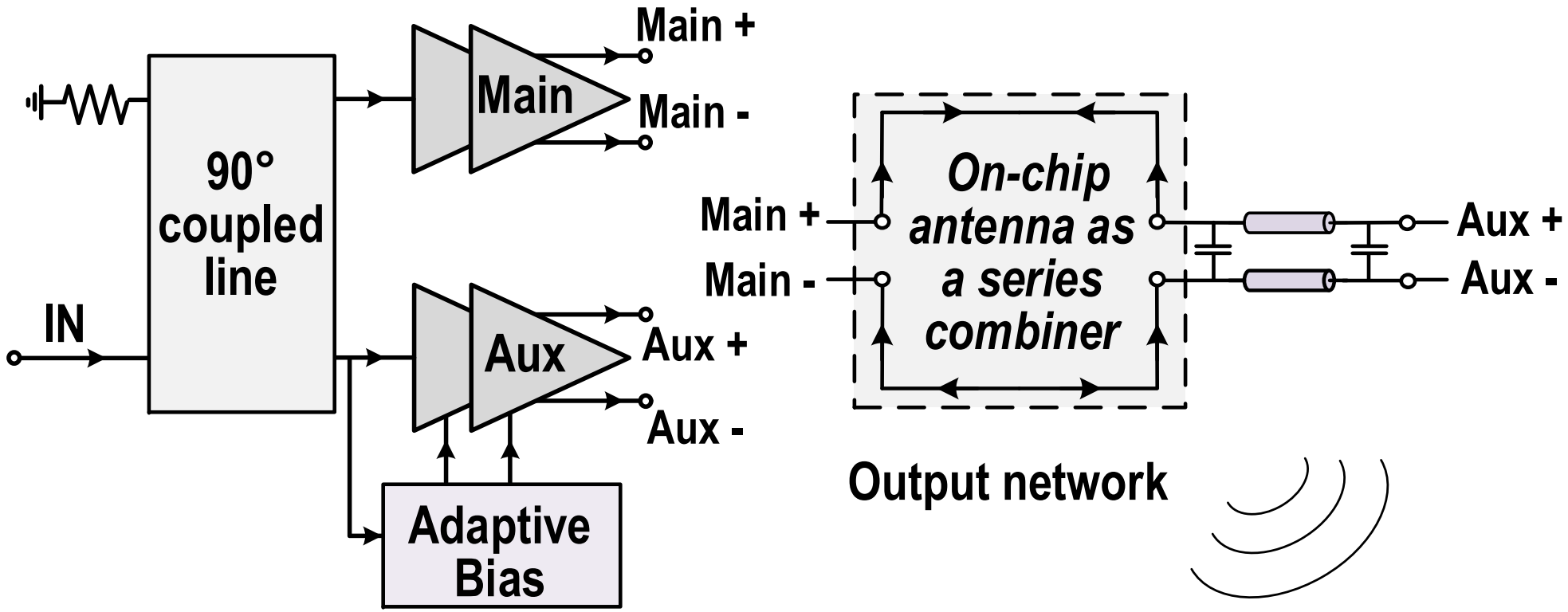
Top Level Schematic



The Doherty Radiator consists of:

- Quadrature Input Splitting
- Identical Main/Aux. PAs
- Adaptive Biasing for the Aux. PAs
- Doherty Radiator Output Network

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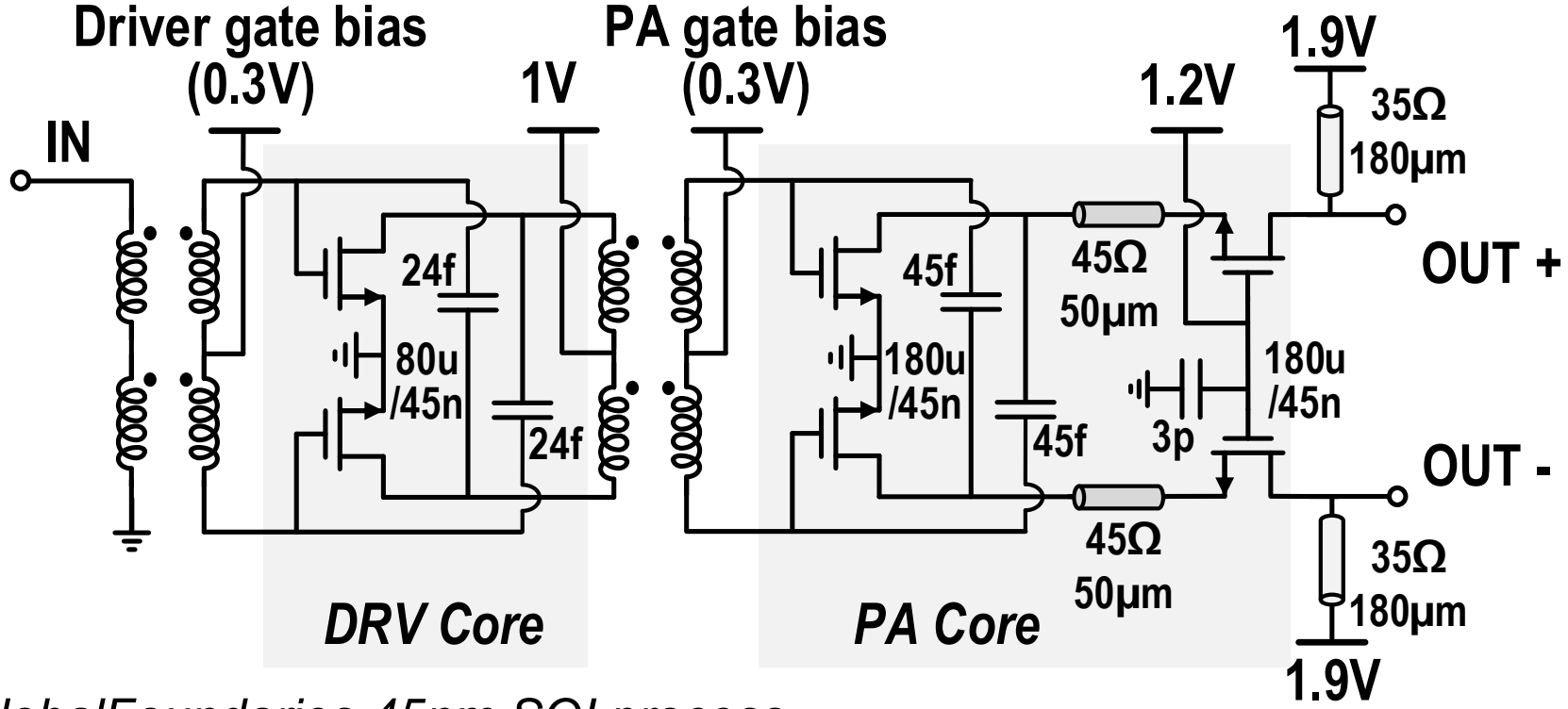
PA Schematic

- PA includes a common-source Driver and a cascode PA
- Transformer matching is employed at input and interstage
- High-Q T-lines is used at output to resonate out the device capacitance



Designed in GlobalFoundaries 45nm SOI process

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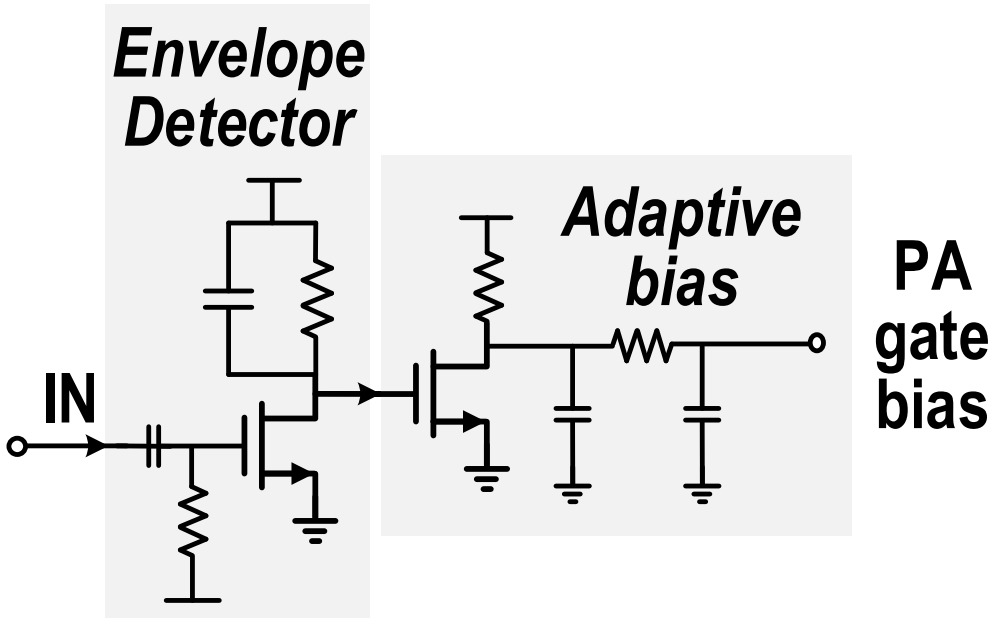
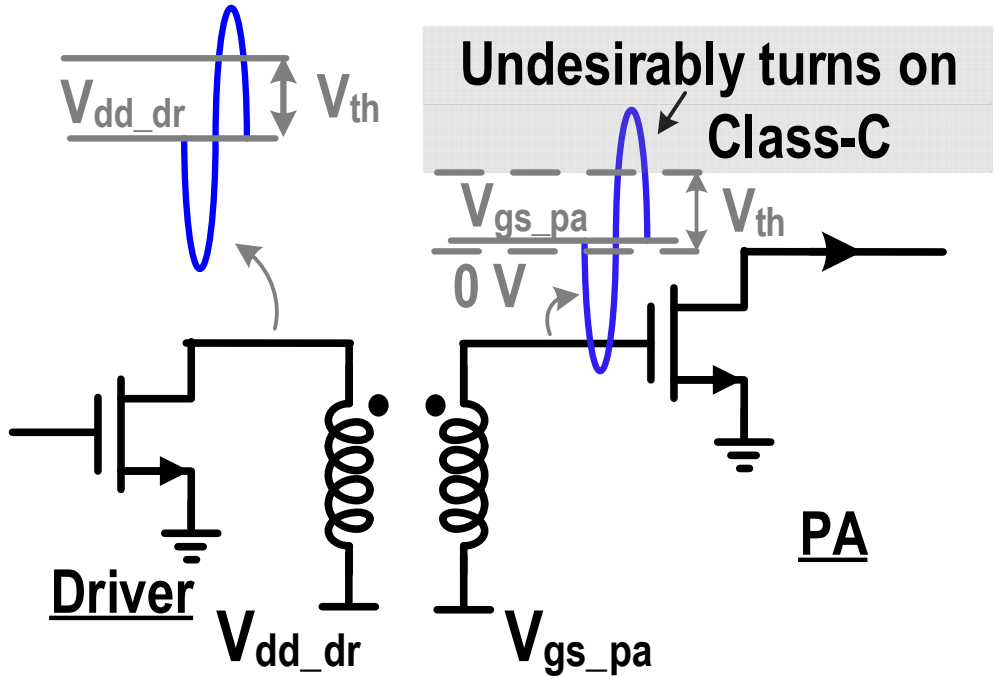
Adaptive Biasing Circuit

- High-speed adaptive biasing in the Aux. path is utilized to improve Main/Aux. PA cooperation





- Employing adaptive biasing only at the Aux. PA is often inadequate:
  - ➢ *Even at deep PBO, DRV swing can be sufficiently large to undesirably turn on the Aux. PA*

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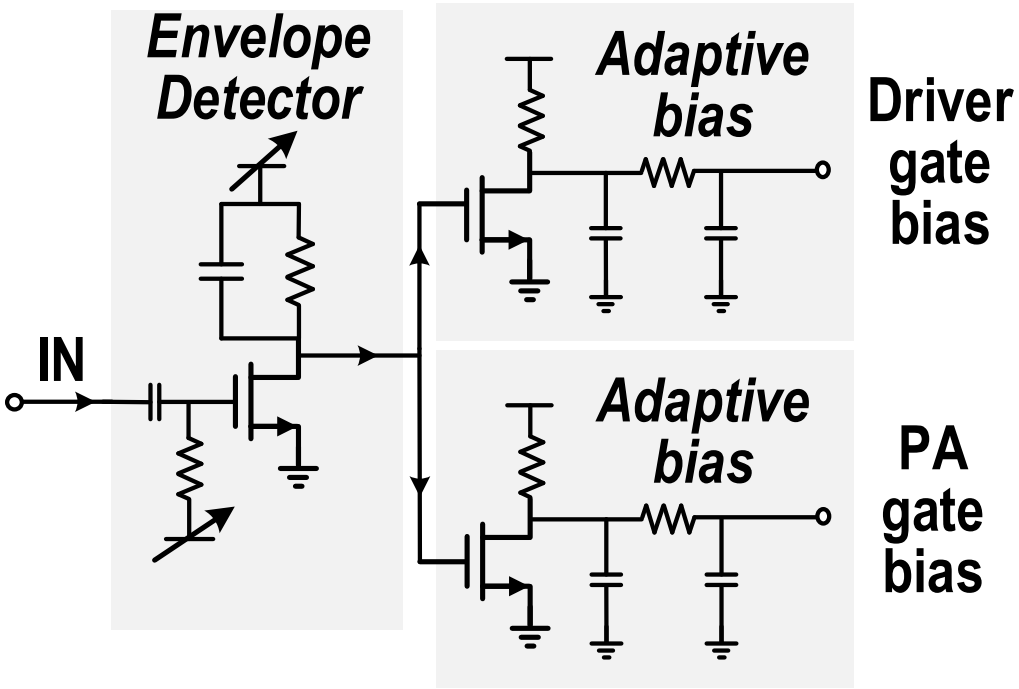
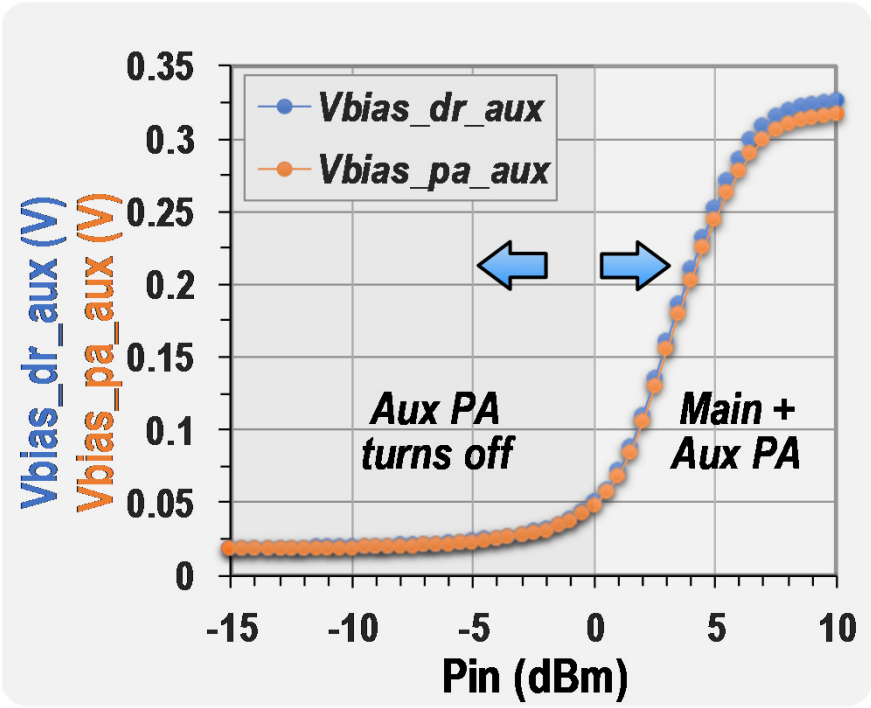
Adaptive Biasing Circuit

- We apply adaptive biasing to both DRV & PA of the Aux.
  → Completely turn off the Aux. DRV before 6dB PBO
  (save DRV Aux. power consumption)
  → Prevent the Aux. PA from undesirably turning on due to high Aux. DRV swing





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Quadrature Input Splitting

- Coupled Line for 90° signal generation
- Isolation port is terminated with 50 Ohm impedance

→*Provides isolation between I & Q signals (or Main & Aux. inputs)*

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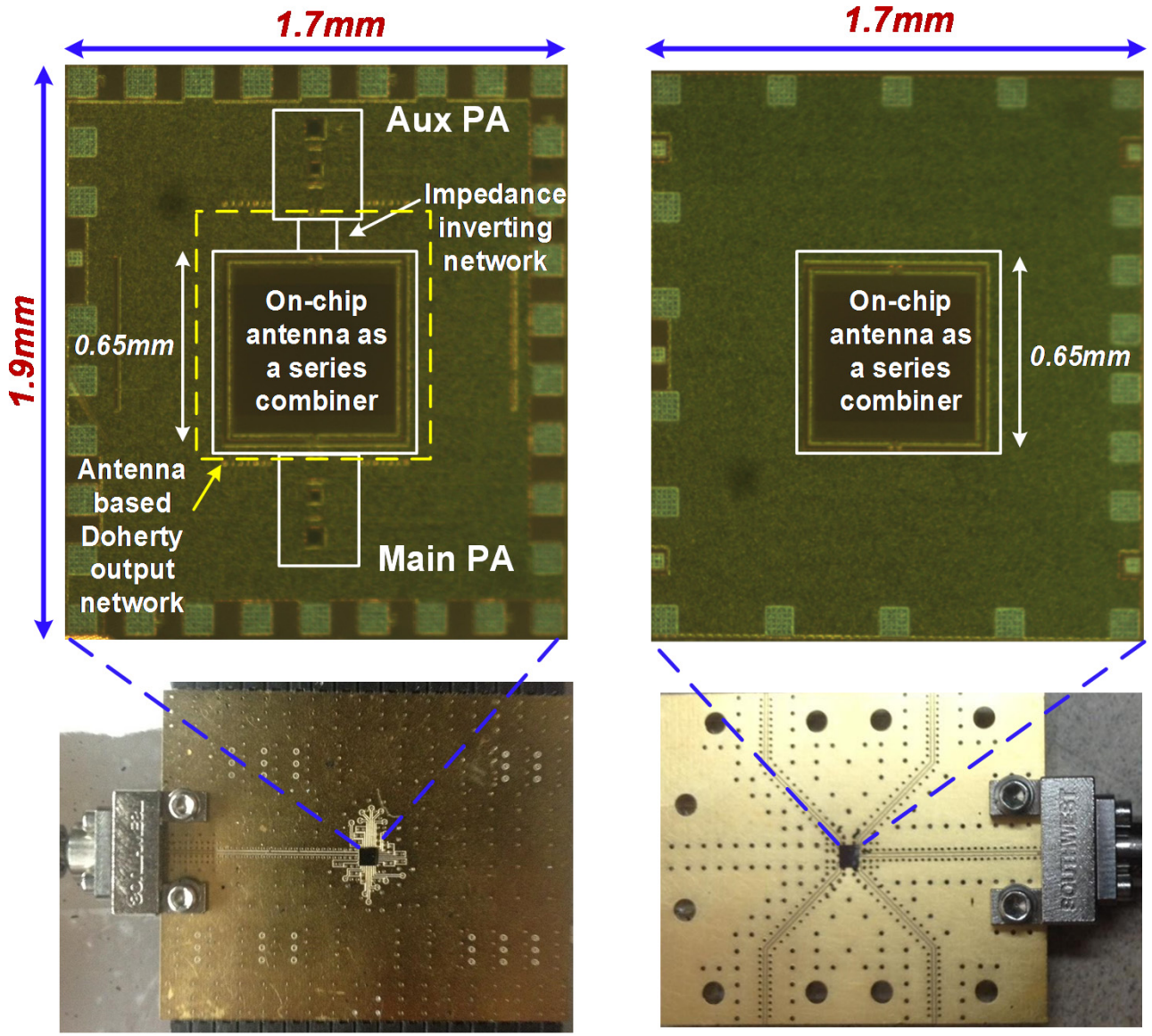
Doherty Radiator

- Chip dimension: 1.7mm x 1.9mm (including on-chip antenna)
- Flip-chip packaged to Rogers PCB
- Radiates from backside of the chip
- Separate test structure is fabricated to characterize the antenna performance



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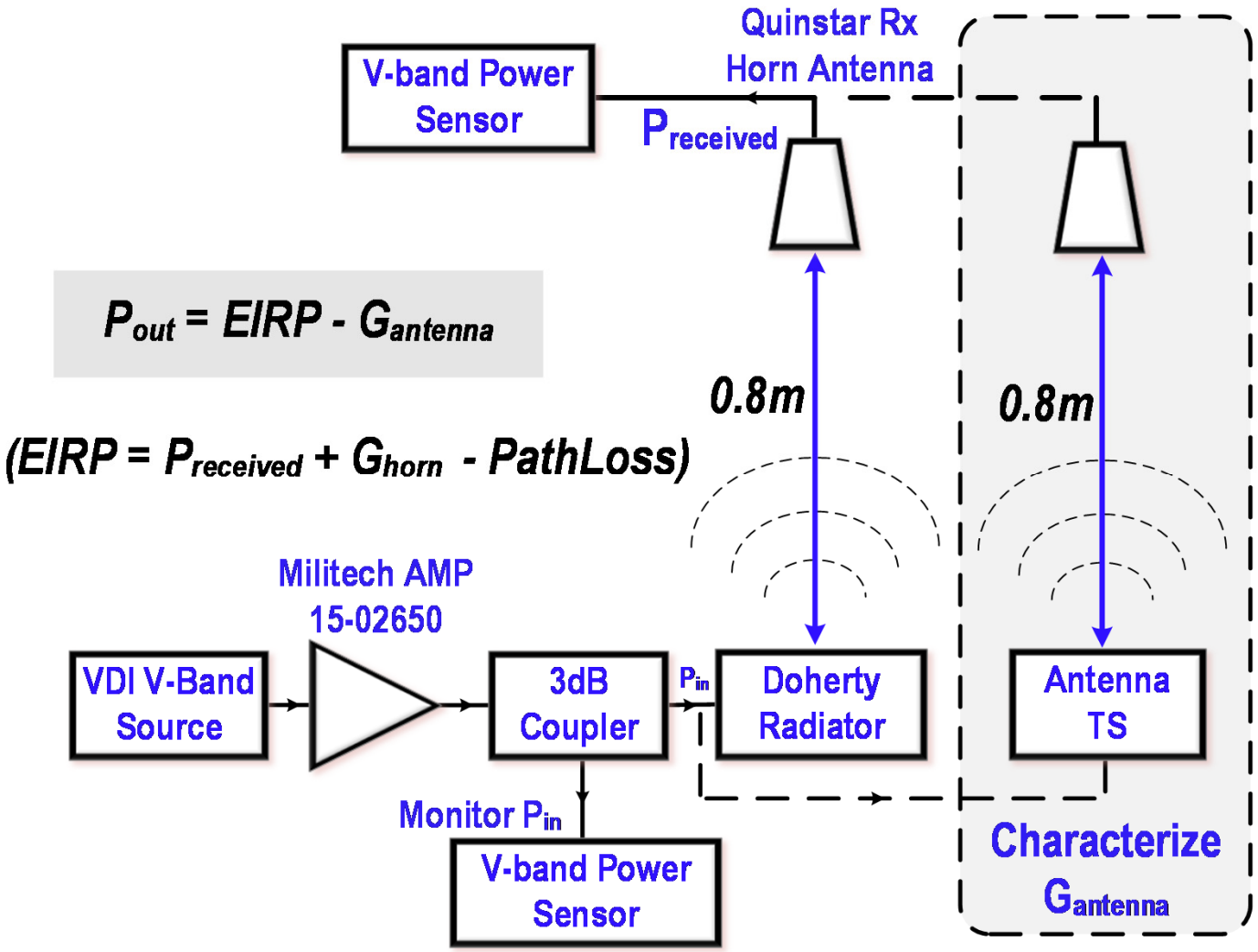
CW Measurement Setup

- Output power (P_{out}) of the Doherty Radiator is the power delivered to the antenna
- $P_{out} = EIRP - G_{antenna}$
- Antenna gain ($G_{antenna}$) is measured on a separate test structure



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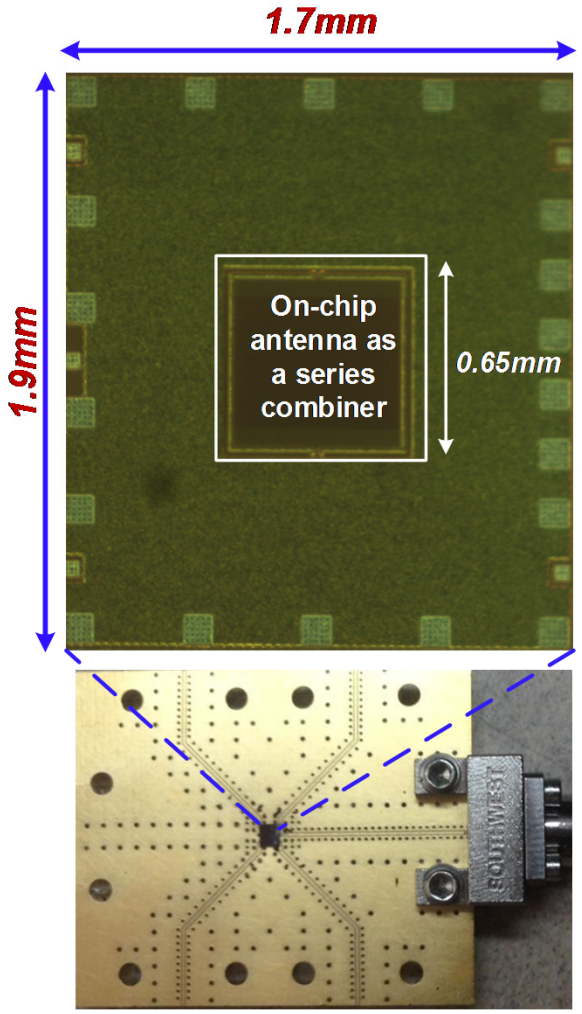
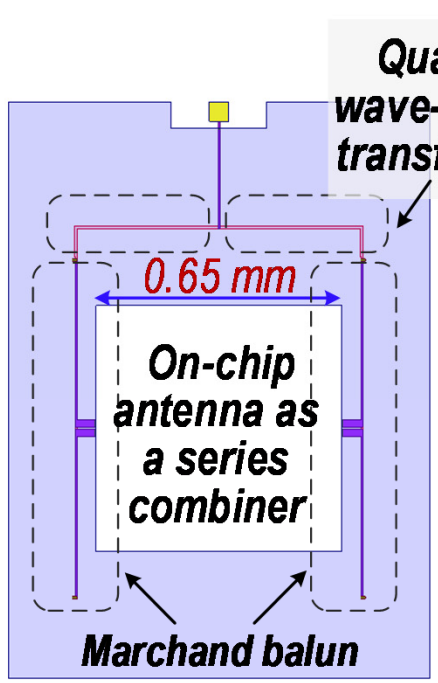
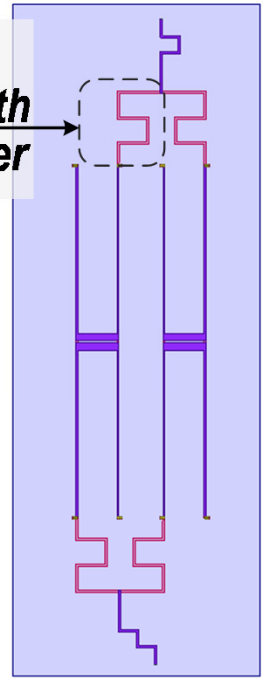
Antenna Characterization

- Power is divided equally into 4 feeds through Marchand baluns
- Back-to-back test structure de-embeds the loss of the antenna feeding network
- At 63/65/67GHz, antenna gains are 4.36/4.5/4.4dBi





On-chip antenna test structure with feeding network



Back-to-back test structure to de-embed the loss of the antenna feeding network

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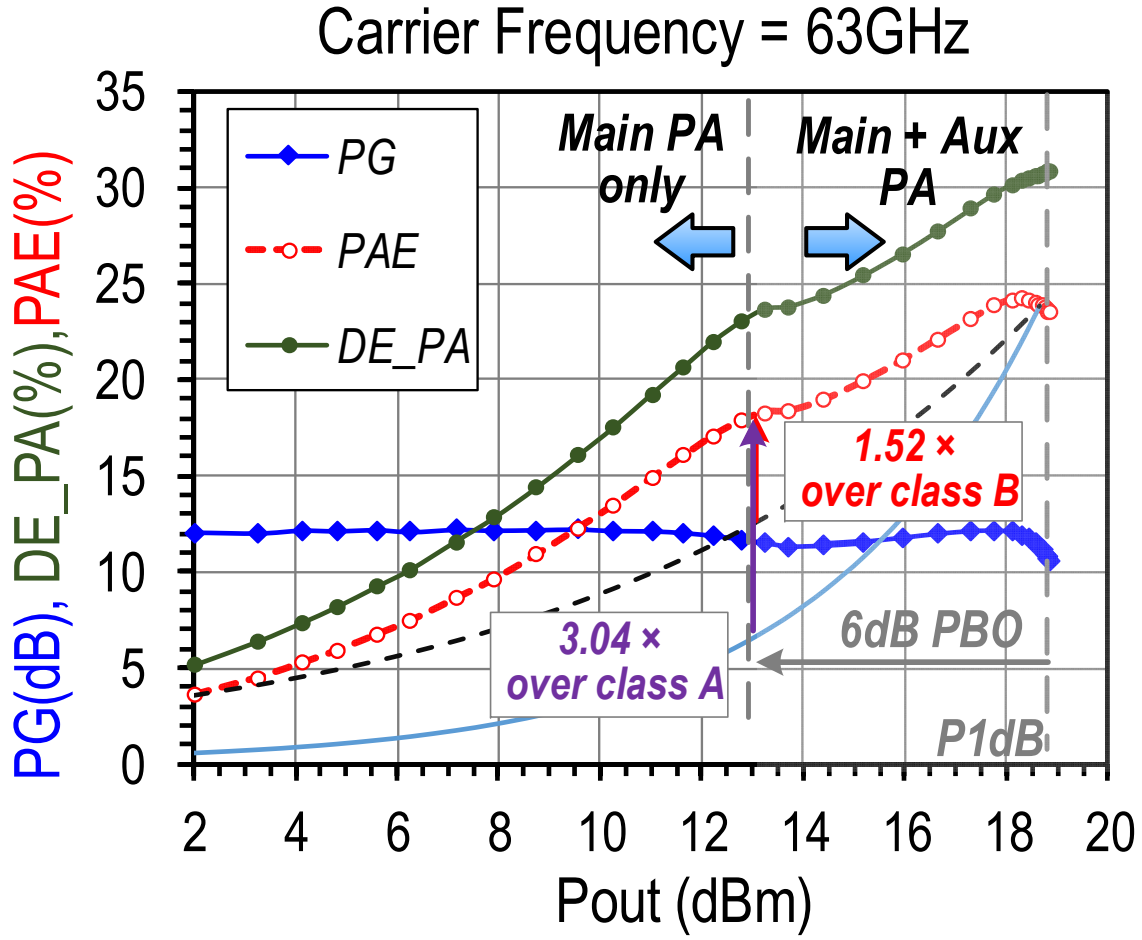
CW Performance

- **CW measurements at 63GHz:**

✓ +18.8 dBm P1dB

✓ 24% PAE $_{0dB\ PBO}$ and 18.3% PAE $_{6dB\ PBO}$

✓ 1.52 × PAE enhancement over class-B at 6dB PBO



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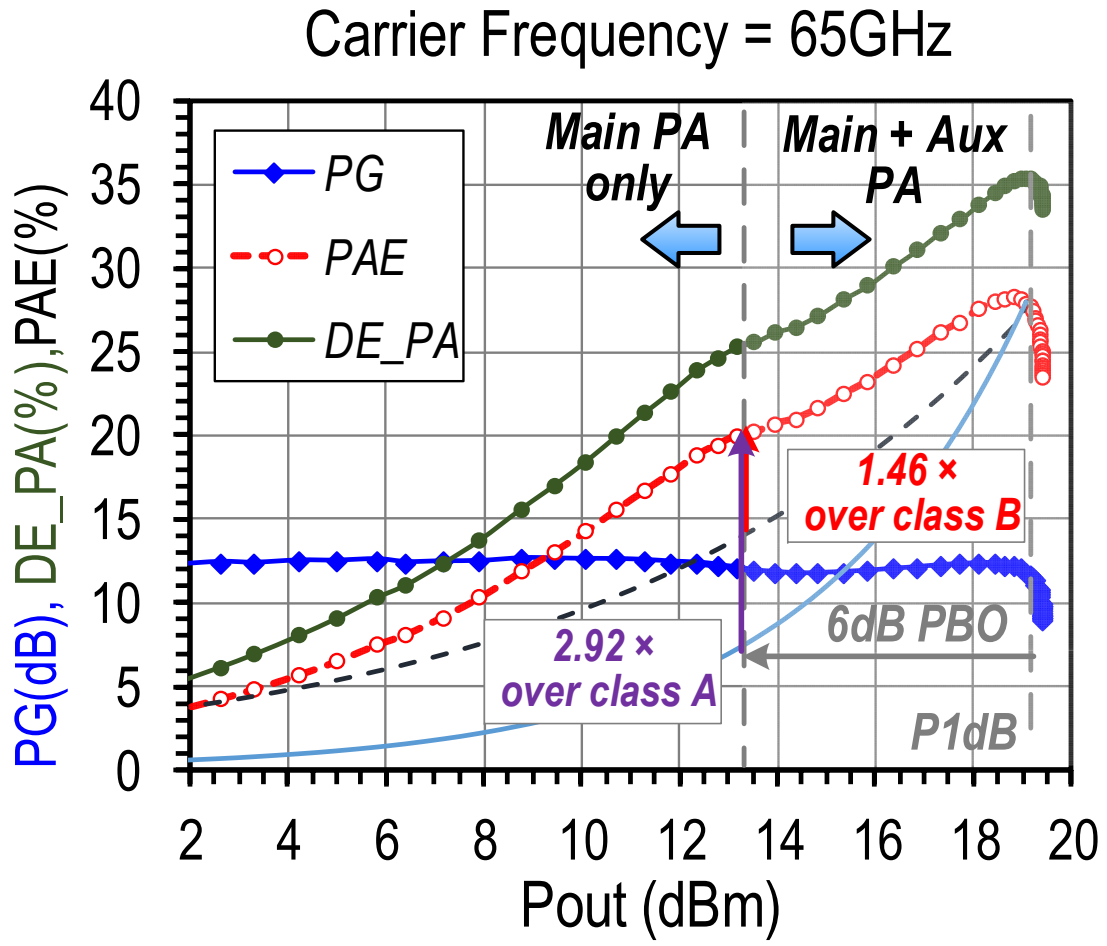
CW Performance

- **CW measurements at 65GHz:**

✓ +19.2 dBm P1dB

✓ 27.5% PAE $_{0dB\ PBO}$ and 20.1% PAE $_{6dB\ PBO}$

✓ 1.46 × PAE enhancement over class-B at 6dB PBO



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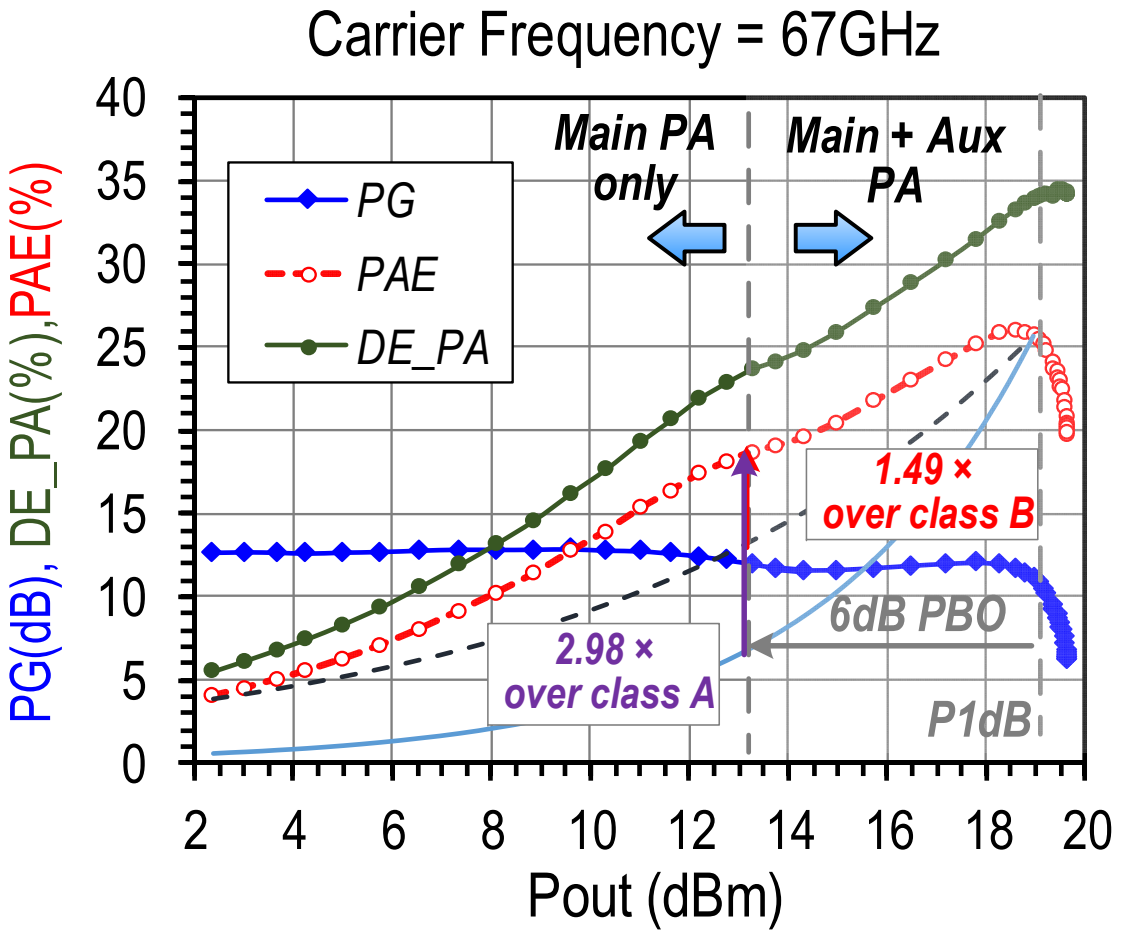
CW Performance

- **CW measurements at 67GHz:**

✓ +19dBm P1dB

✓ 25.1% PAE $_{0dB\ PBO}$ and 18.7% PAE $_{6dB\ PBO}$

✓ 1.49 × PAE enhancement over class-B at 6dB PBO



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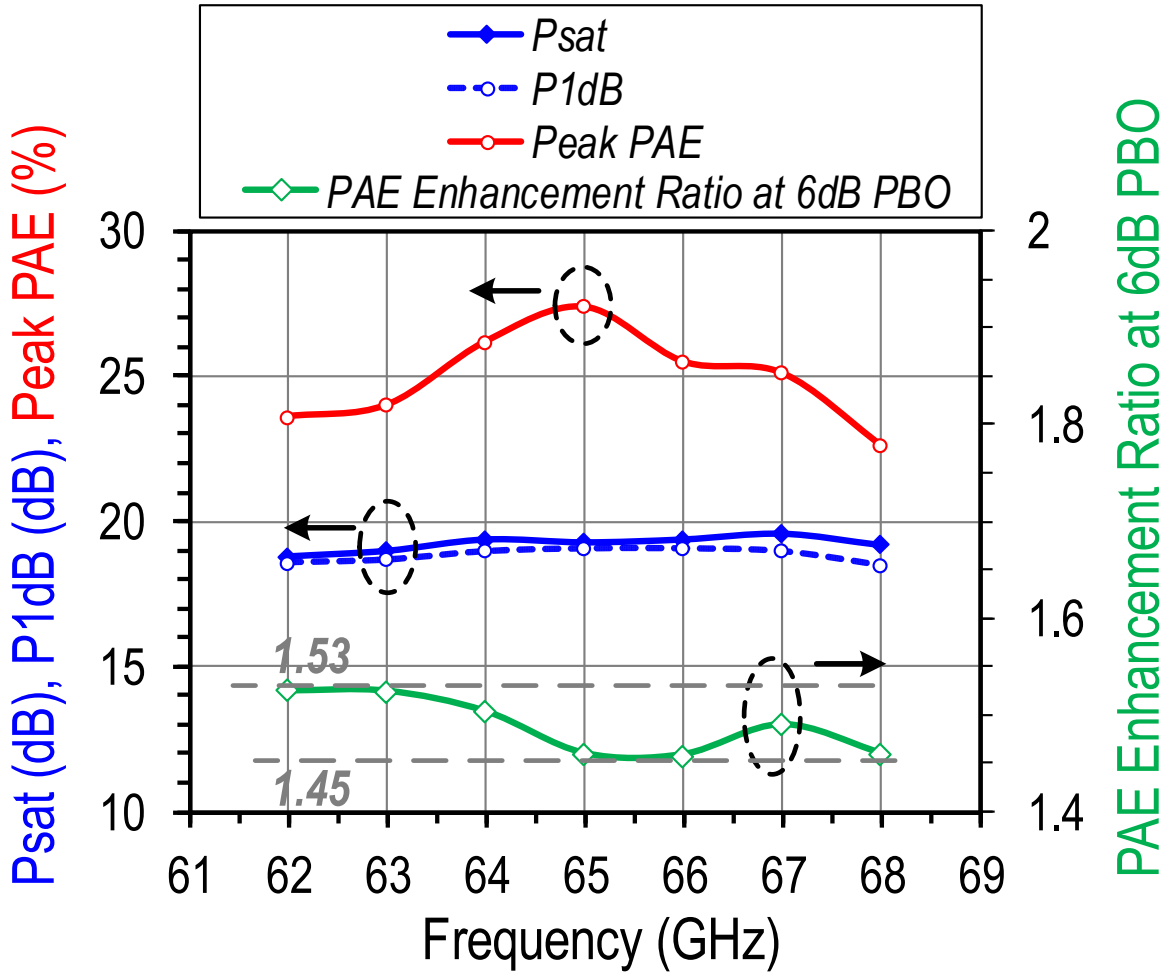
CW Summary

- **CW performance:**

✓ 1.45-1.53 × PAE enhancement over class-B at 6dB PBO



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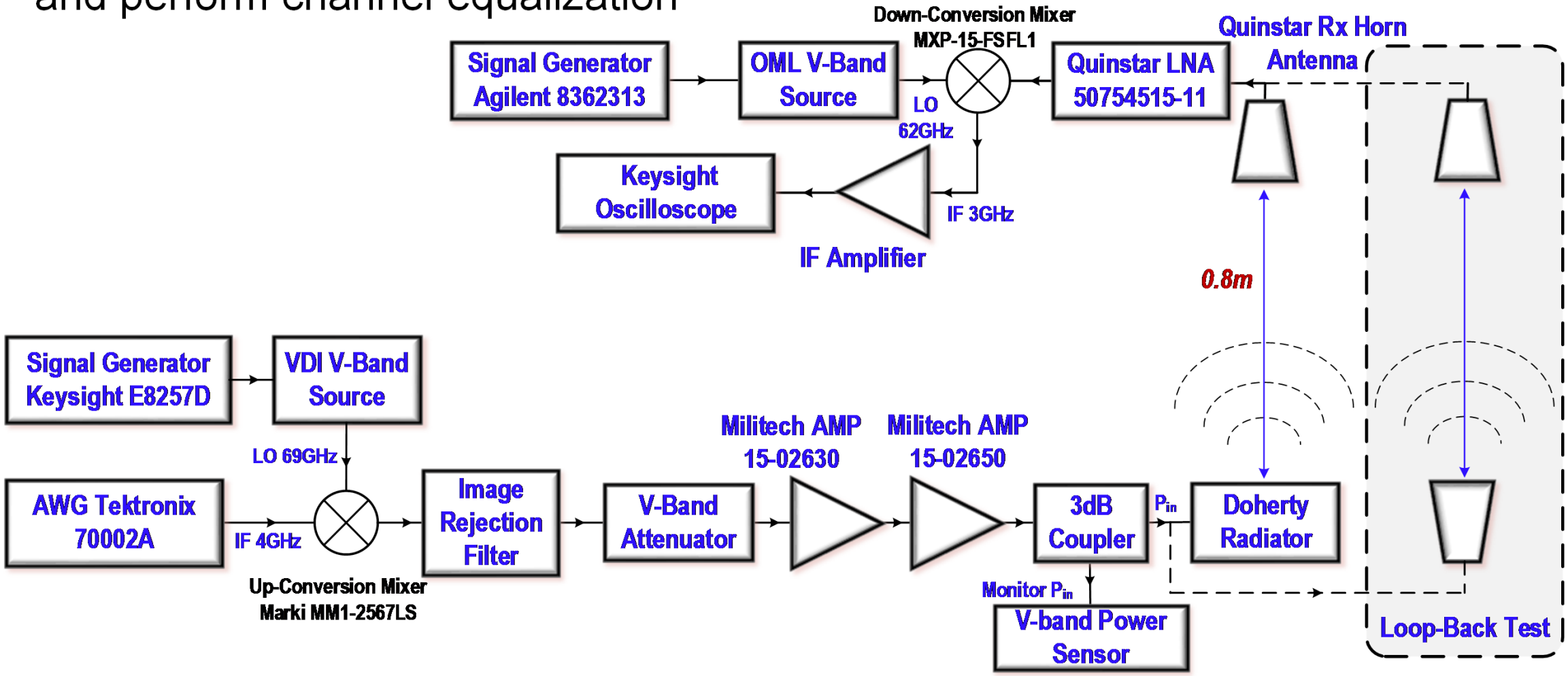
Dynamic Measurement Setup

- In loop-back test, two Horn antennas are utilized to characterize the EVM floor and perform channel equalization



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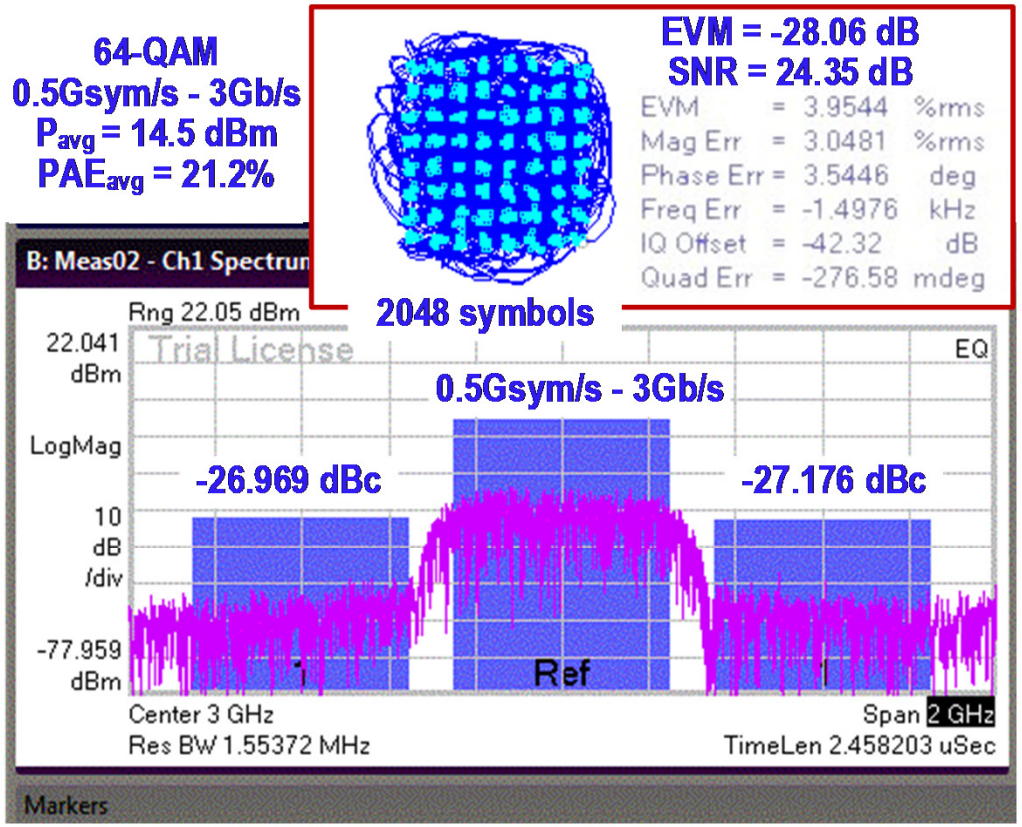
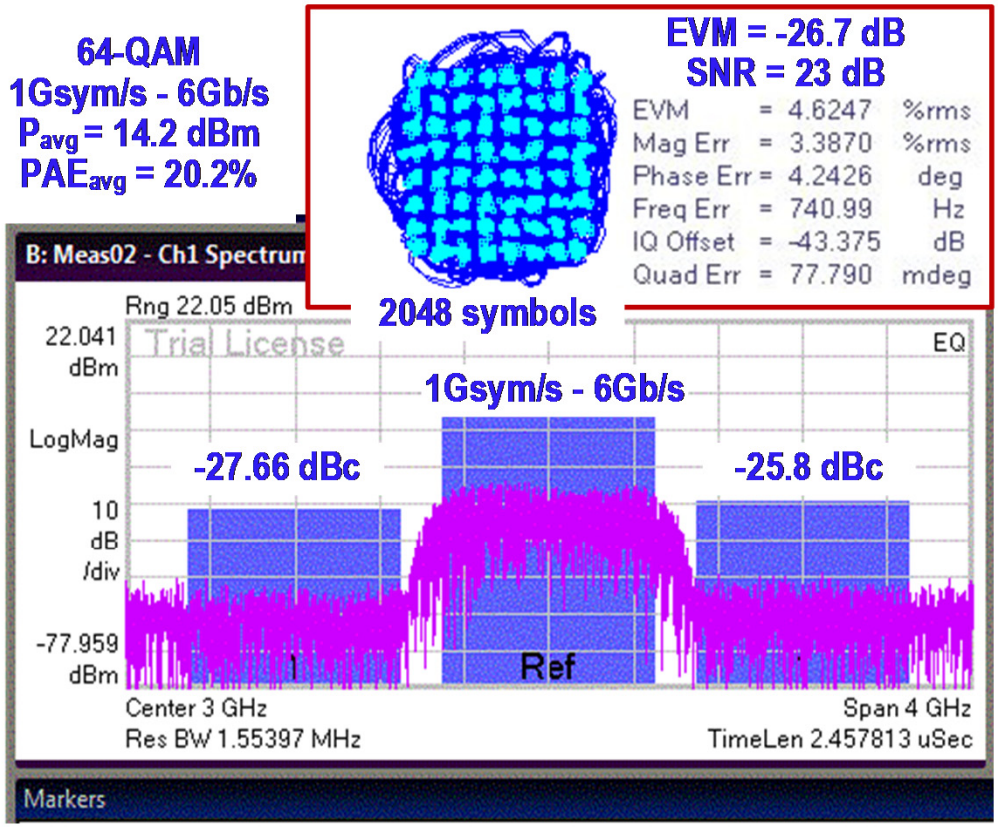
Dynamic Measurement

- Modulation test with 64-QAM, symbol rate = 0.5Gsym/s and 1Gsym/s
- Measurement is performed in boresight direction





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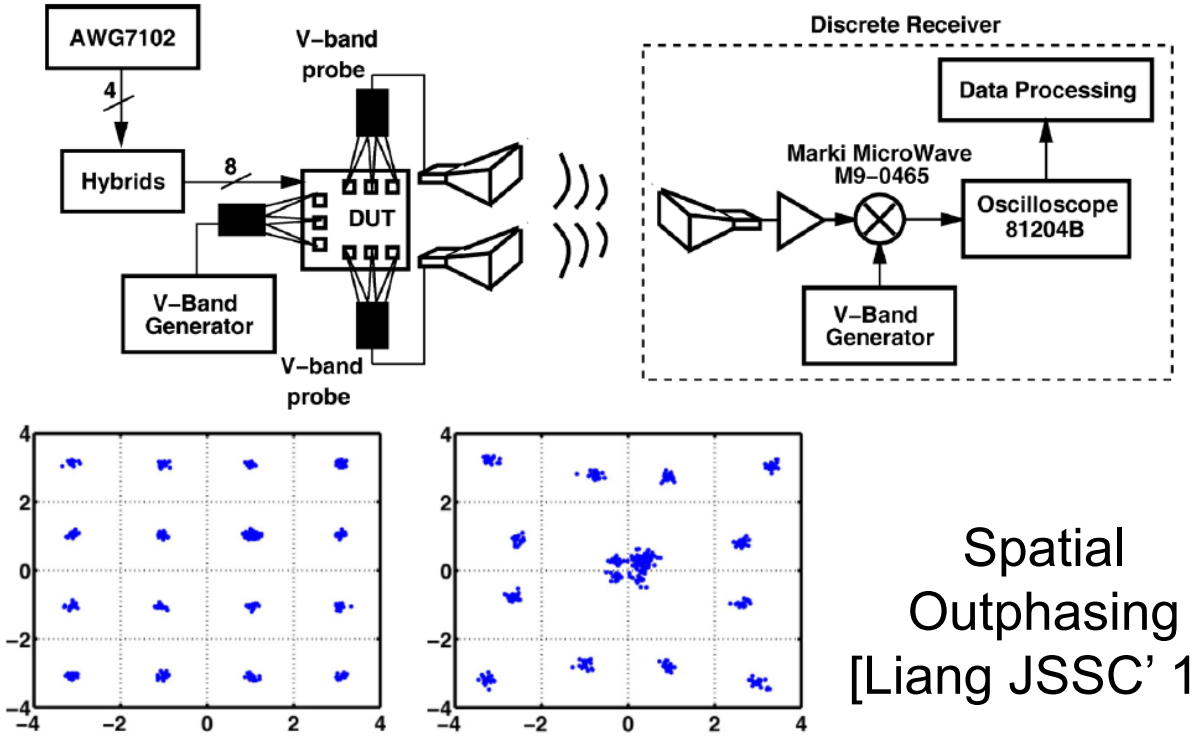
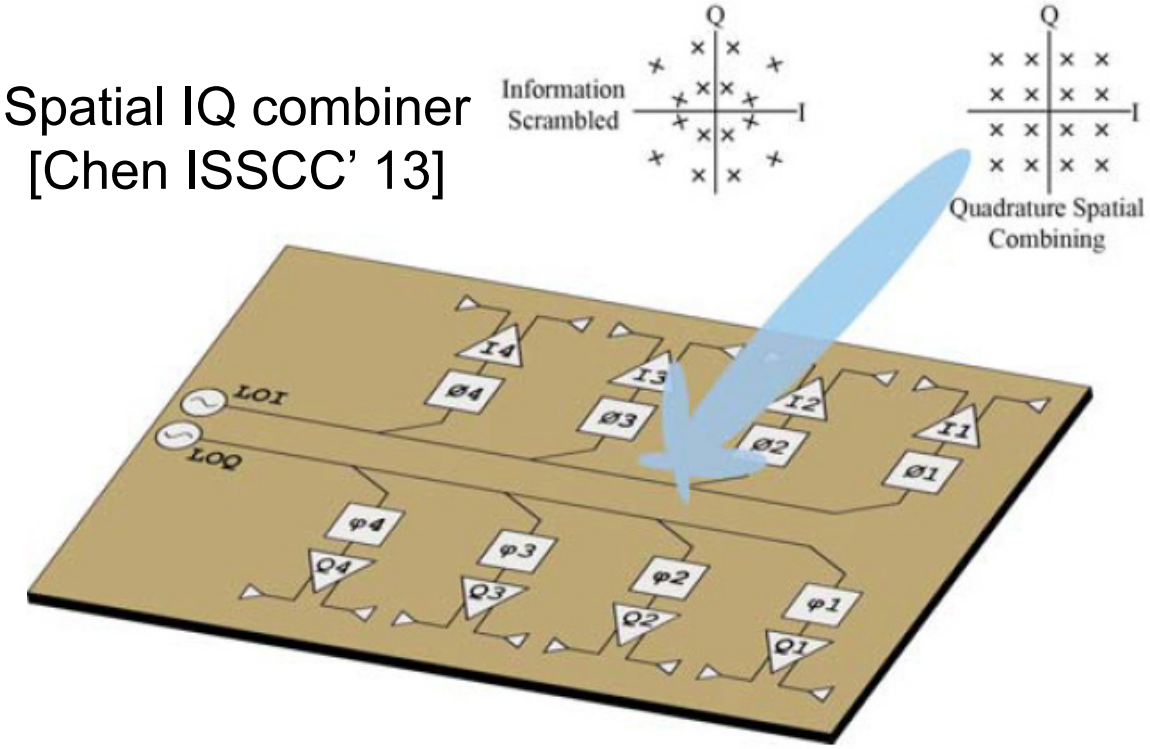
Dynamic Measurement

- Undistorted modulation only happens *at certain directions* in the design of Spatial Outphasing and Spatial IQ Combiner



Spatial Outphasing [Liang JSSC' 11]

Spatial IQ combiner [Chen ISSCC' 13]



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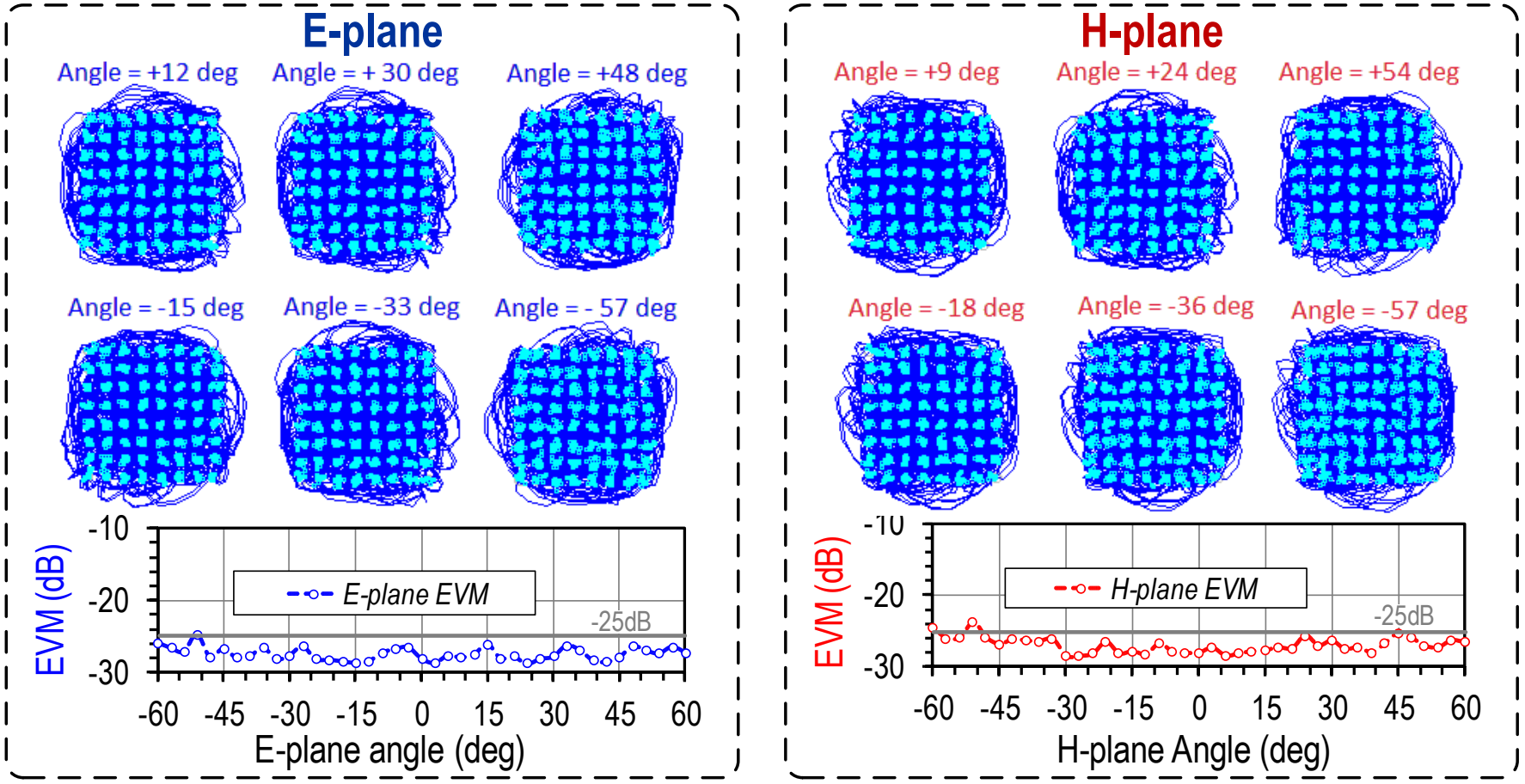
Dynamic Measurement

- In the Doherty Radiator, power is combined on the antenna before radiated out:
  → Constellation is maintained over the *entire antenna FoV*
- Undistorted modulation is observed in both E-plane and H-plane



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Doherty Radiator

- The proposed multi-feed antenna structure is *angle-independent:* constellation is maintained over entire antenna FoV
- This helps *establish reliable communication link* and *ease TX/RX alignment*
- The unit radiator, when integrated in a phased array, does not compromise antenna FoV → Suitable for massive MIMO applications

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Performance Comparison

	This work		Greene, JSSC' 17	Kaymaksut , TMTT'15	Chen, ISSCC' 13	Chi, ISSCC' 17	Khalaf, JSSC'16	Komijani, JSSC'07	Chappidi, JSSC'17	Bhat, TMTT'15
Architecture	Antenna-based Doherty		Doherty	Doherty	Spatial IQ Combining	Antenna Combiner	Digital Polar Tx	Class AB	Asymmetric Combiner	Stacked PA
Frequency (GHz)	65		62	72	60	60	60	77	55	42.5
P_{sat} (dBm)	19.4		17.5*	21	9.6	27.9	10.8	17.5	23.6	27.2
P_{1dB} (dBm)	19.2		17.1	19.2	9.6	25	7.4	14.5	19.9	21*
Peak PAE	28.3%		23.7%*	13.6%	28.5%	23.4%	29.8%	12.8%	27.7	10.7
PAE @ P_{1dB}	27.5%		23.7%	12.4%	28.5%	16.2%	15% *	11.8%*	15.7	5*
PAE @ 6dB PBO	20.1%		13%	7%	14.25%*	6%*	4.5% *	3%*	7%*	--
PAE Enhancement Ratio at 6dB PBO**	1.46		1.10	1.13	1	0.74	0.6	0.51	0.89	--
Mod. Scheme	64-QAM	64-QAM		64-QAM	16-QAM	64-QAM	16-QAM		64-QAM	
Data Rate	3Gb/s	6Gb/s		0.6Gb/s	6Gb/s	4.8Gb/s	6.7Gb/s		3Gb/s	
EVM	-28dB	-26.7dB	N/A	-25.6dB	-16.2dB	-25.4dB	-18.1dB	--	-21dB	--
P_{avg}	14.5dBm	14.2dBm		+15.9dBm	+6dBm*	+19.3dBm	+3.6dBm		14.8 dBm	
PAE_{avg}	21.2%	20.2%		7.2%	16.5%	5.3%	--		--	
Technology	45nm CMOS SOI		130nm SiGe BiCMOS	40nm CMOS	65nm CMOS	45nm CMOS SOI	40nm CMOS	120nm SiGe BiCMOS	130nm SiGe BiCMOS	45nm CMOS SOI

* Estimated from reported figures

** Compared to an idealistic class-B PA with the same PAE at P1dB

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Conclusion

- To the best of the authors' knowledge, this is the first time a Doherty output network is constructed on the antenna
- Together with high-speed adaptive biasing, the Doherty Radiator demonstrates substantial PBO efficiency enhancement and undistorted modulation transmission
- Compared with the reported 60-80GHz silicon PAs/transmitters, this work achieves
  - ✓ the best PAE PBO enhancement ratio at 6dB PBO
  - ✓ the highest PAE at 6dB PBO
  - ✓ the highest average PAE for 3Gb/s and 6Gb/s 64-QAM modulation transmission
- This demonstrates the PBO efficiency advantage of Doherty architecture

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Acknowledgement

- We would like to thank GlobalFoundaries for chip fabrication

- We would like to thank members of Georgia Tech GEMS lab for the technical discussions and supports

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A 69 to 79GHz CMOS Multiport PA/Radiator with +35.7dBm CW EIRP and Integrated PLL

B. Abiri, A. Hajimiri, California Institute of Technology, Pasadena, CA

Caltech

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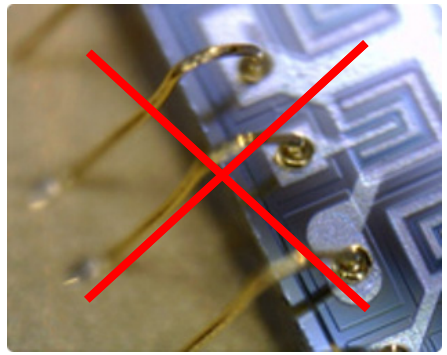
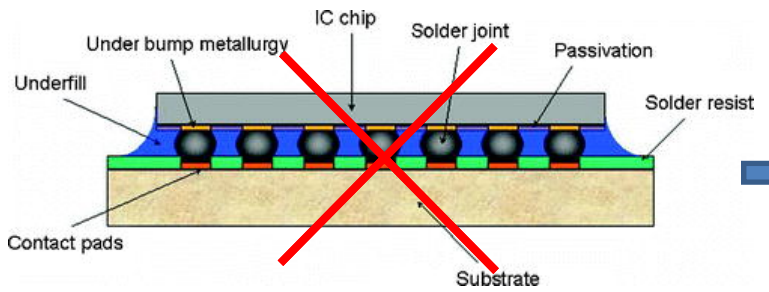
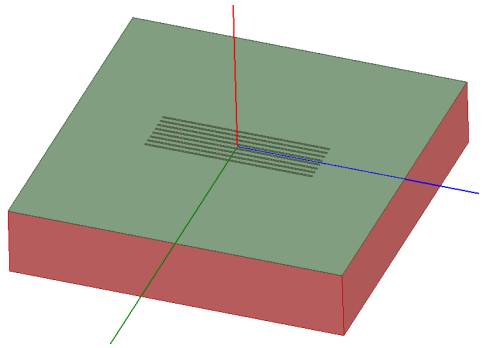
Why On-Chip Radiators at mm-Wave?



Wire-bonds are highly inductive & lossy at mm-Wave



Flip-Chip bump has smaller inductance, but requires expensive PCB/Interposer



On-chip Antenna is cheap and more predictable

- IC scaling has resulted in extremely fast transistors in CMOS process enabling mm-wave generation and manipulation.
- Expensive interfacing/antenna costs at mm-wave frequencies refutes use of CMOS technology.
- Solution is to integrate antennas on chip to reduce the cost and improve performance.

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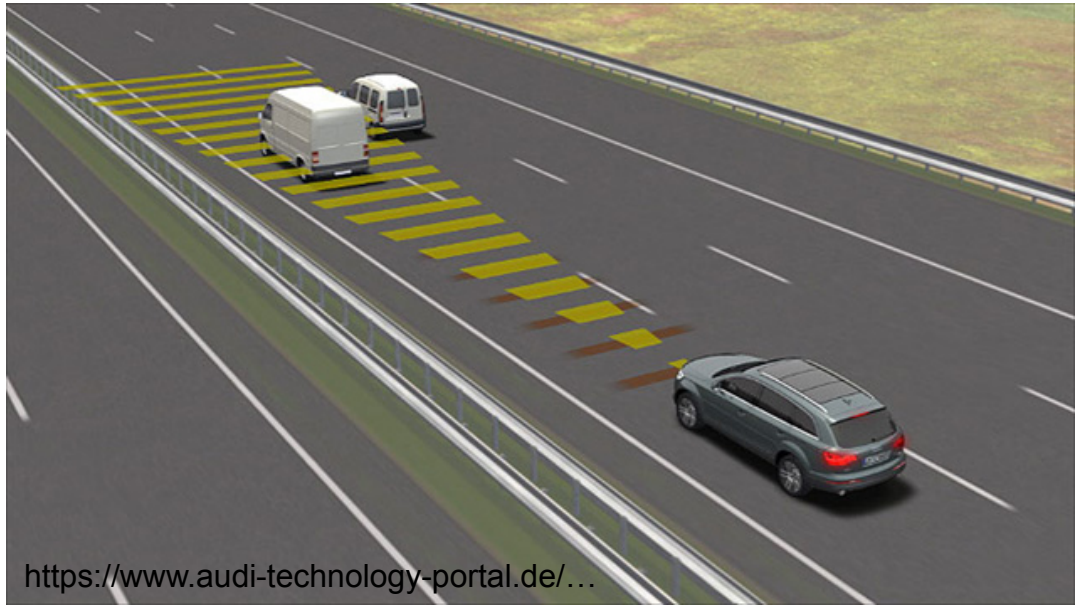
Output Power Matters



- Higher power transmitters allow for:
  - Longer range for automotive radars.
  - Ability to detect objects with smaller radar cross section.
  - Longer range for point-to-point communication links.
  - Higher data rates for point-to-point communication links.
  - Reduce the required antenna gain and size for point-to-point links.

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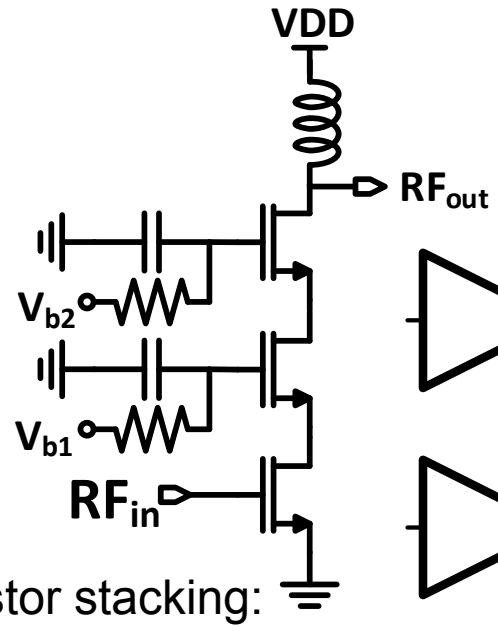
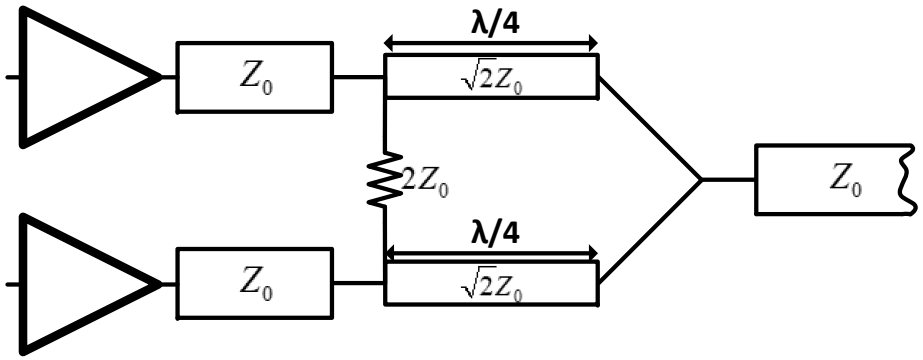
High Power Generation Approaches in CMOS



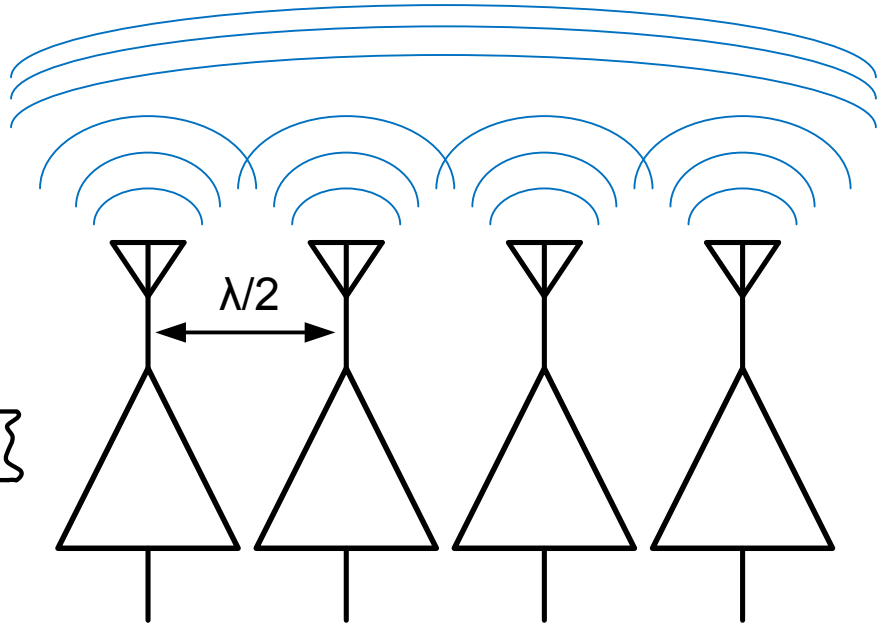
Transistor stacking:

✗ Lower efficiency due to larger switch resistance



Power combining circuits:

✗ Introduces extra loss.



Spatial power combining (SPC) in phased arrays

✗ Large empty area between antenna elements

- CMOS transistor scaling has forced lower supply voltages.
- Power combining and stacking are two main paths to enhance transmitted power.
- Spatial power combining through phased arrays is the most efficient way but is area hungry.

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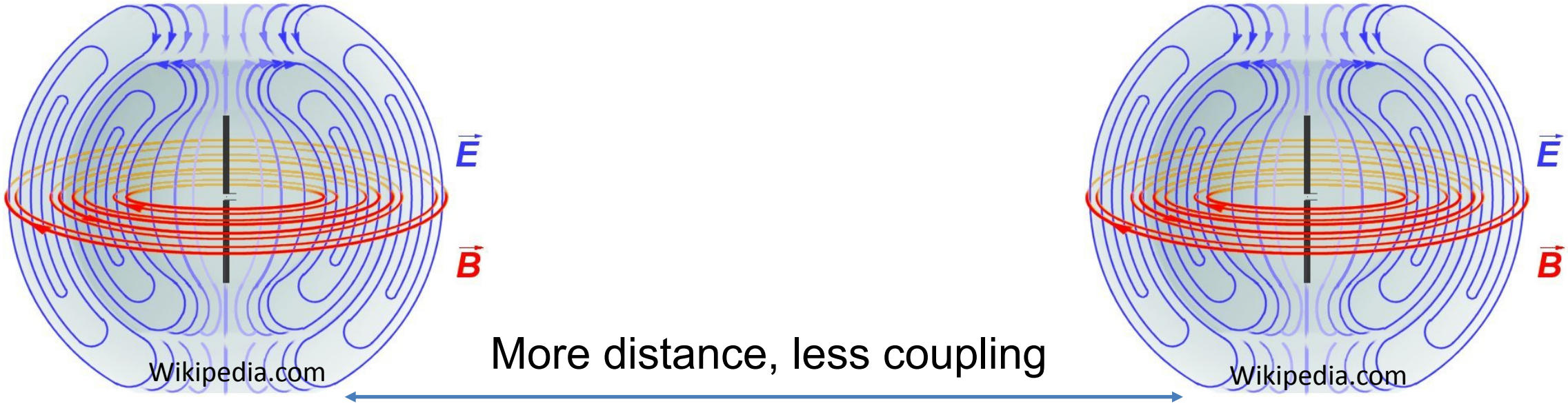
Why Space the Antennas Apart in Phased Arrays?



- Antennas produce strong electromagnetic fields nearby.
- Packing them closely will affect their properties due to coupling.
- Designers avoid dealing with coupling by placing them far apart.
- Precious silicon area is wasted to mitigate the coupling.

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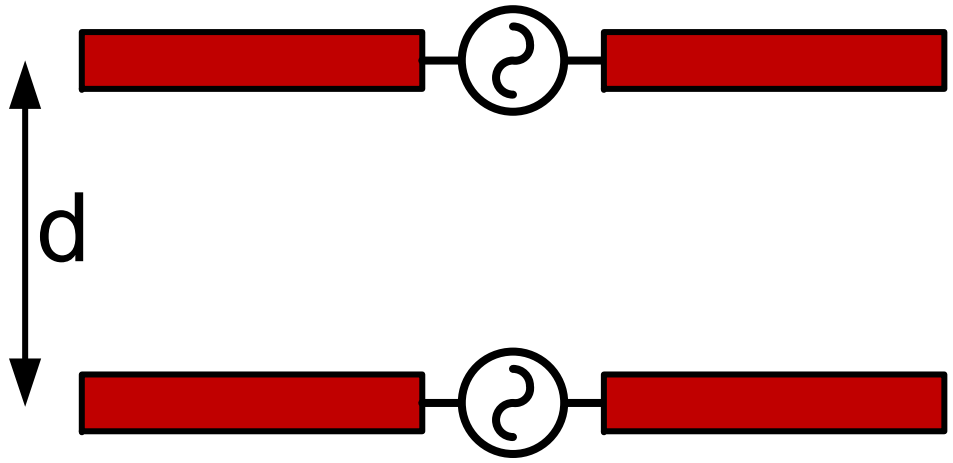
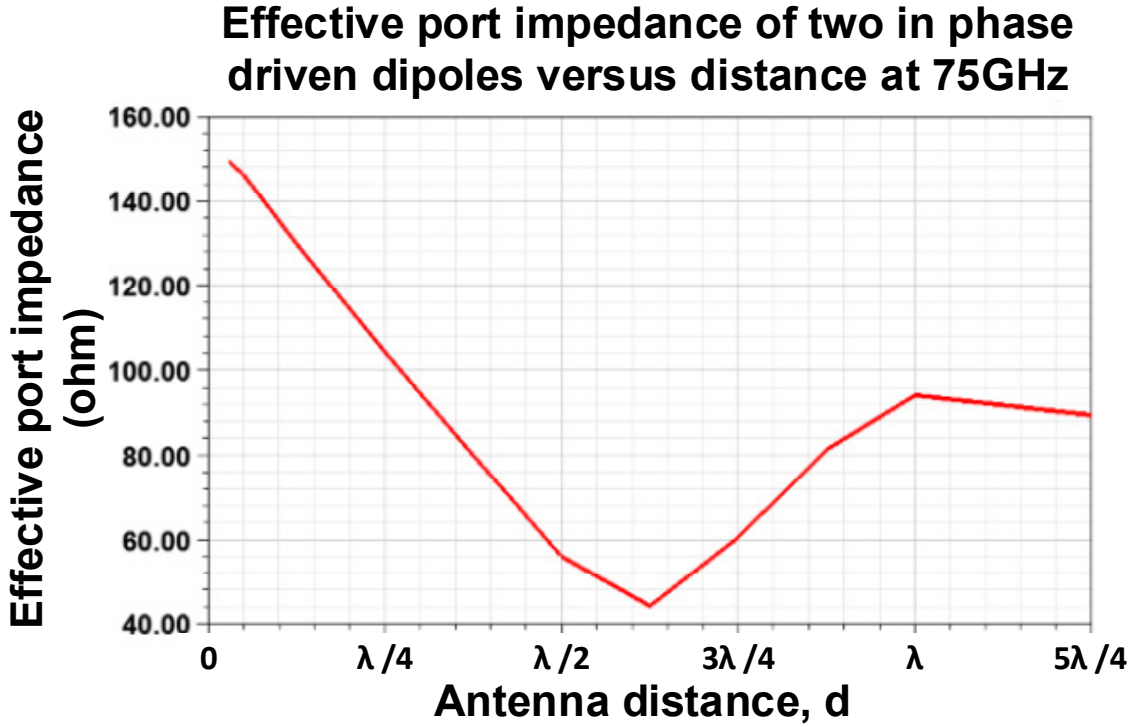
The Effect of Coupling on Dipole Antennas





- Coupling affects effective antenna impedance & radiation pattern.
- Antenna impedance sets how much power is accepted for a given voltage.
- Impedance seen by each driver doubles when two dipoles placed closely.
- For fixed driver voltage swing, doubling the impedance halves the accepted power by each antenna.

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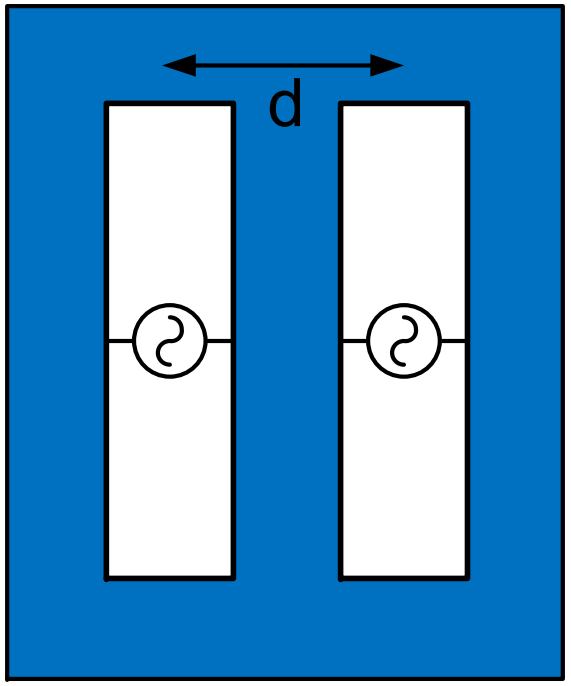
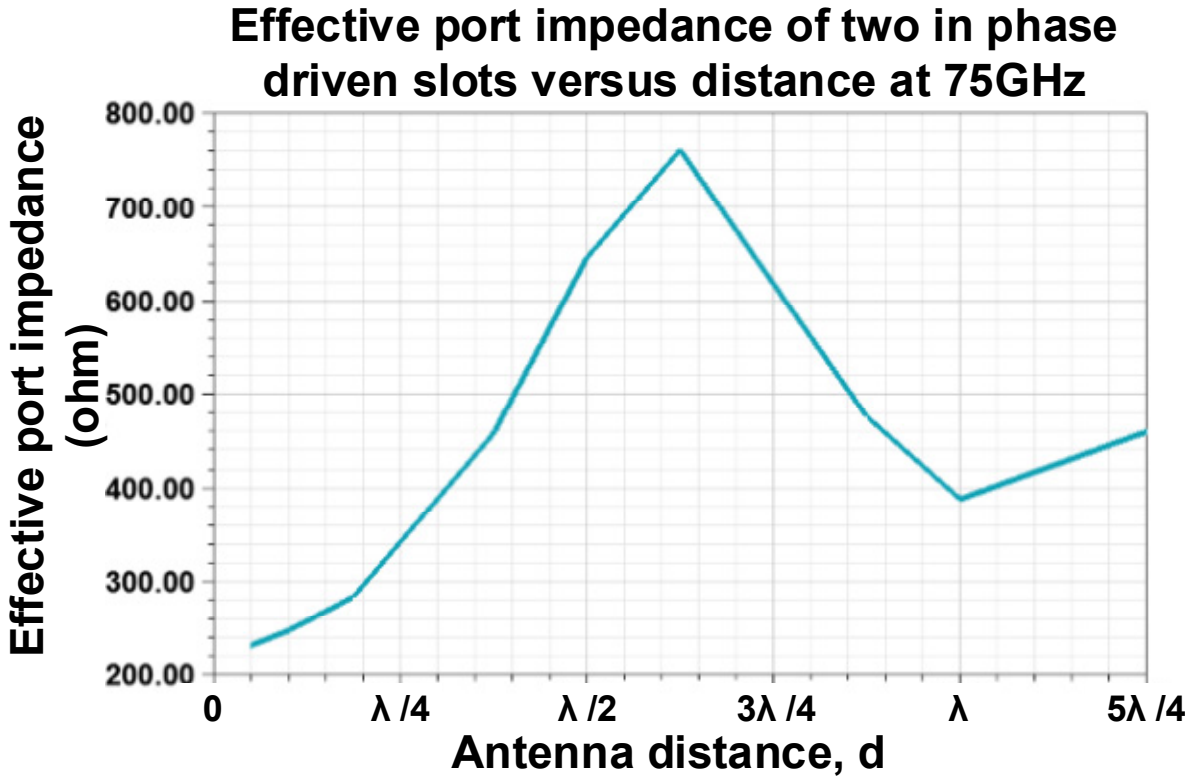
The Effect of Coupling on Slot Antennas





- Unlike dipole antenna, two closely placed slot antennas will load the driver with half of impedance.
- For fixed driver voltage swing, twice the power is delivered to each antenna.

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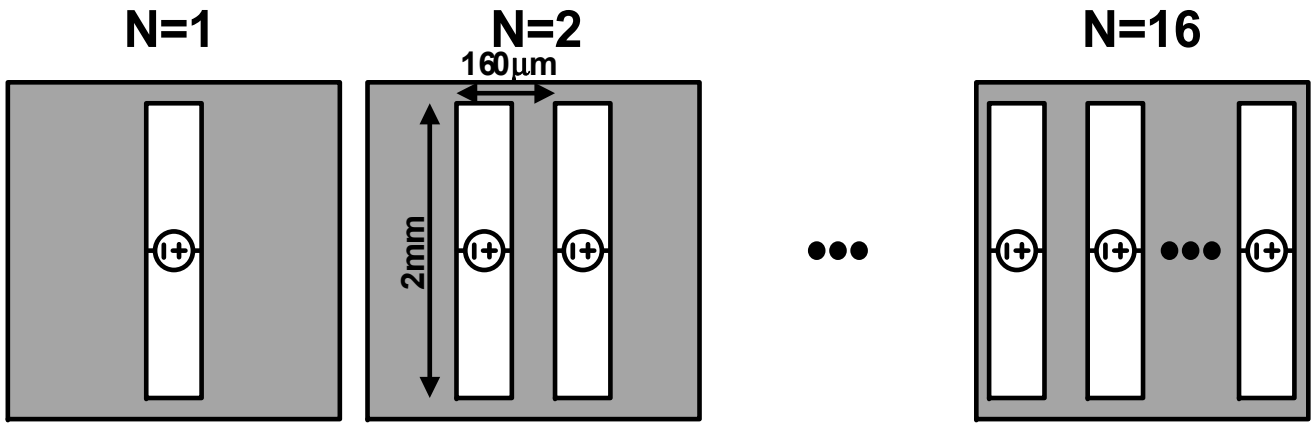
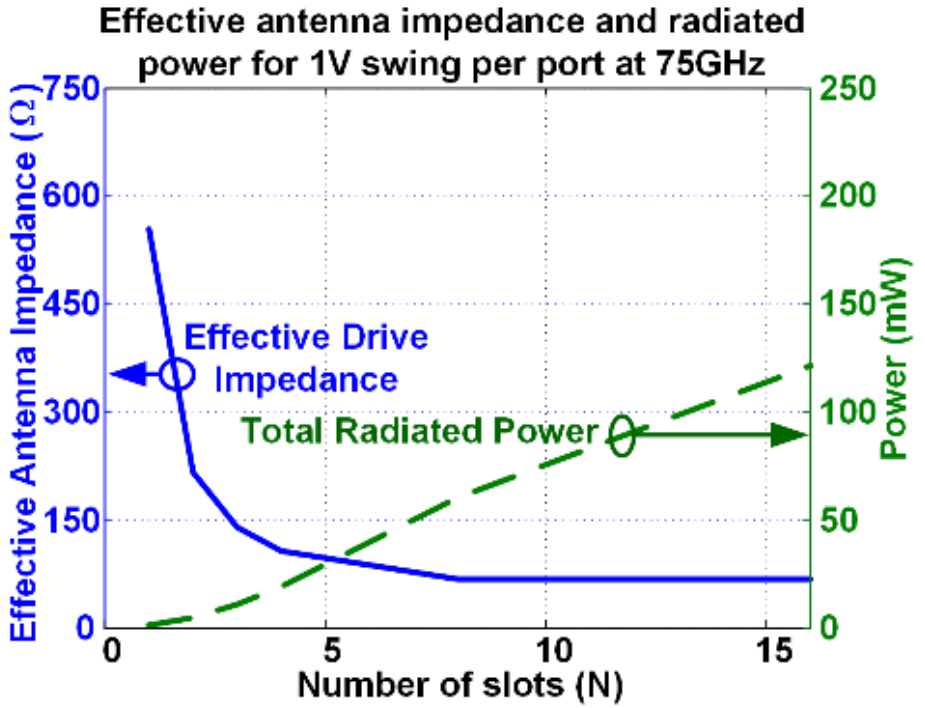
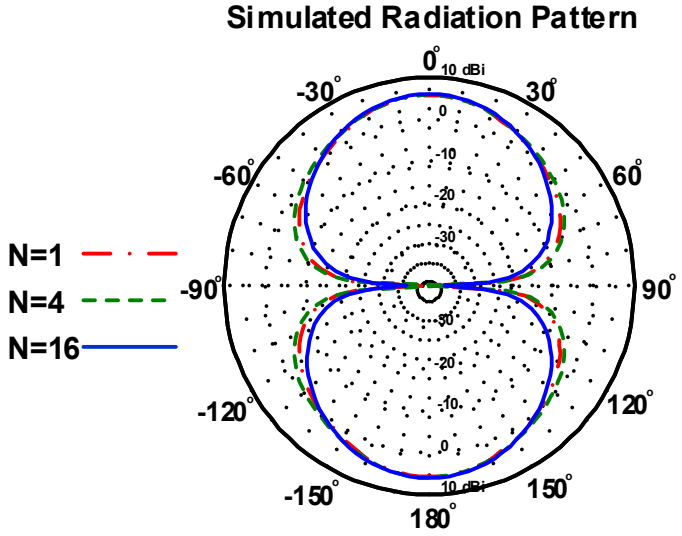
Impedance Scaling in Tightly Coupled Slot Arrays





- Addition of tightly coupled slots reduces impedance further.
- Impedance scaling continues 1/N trend until edge slots don't couple tightly.
- Total radiated power grows quadratically initially then linearly with N.

$$TRP = N \times \frac{V^2}{2R_0/N} = N^2 \times \frac{V^2}{2R_0}$$



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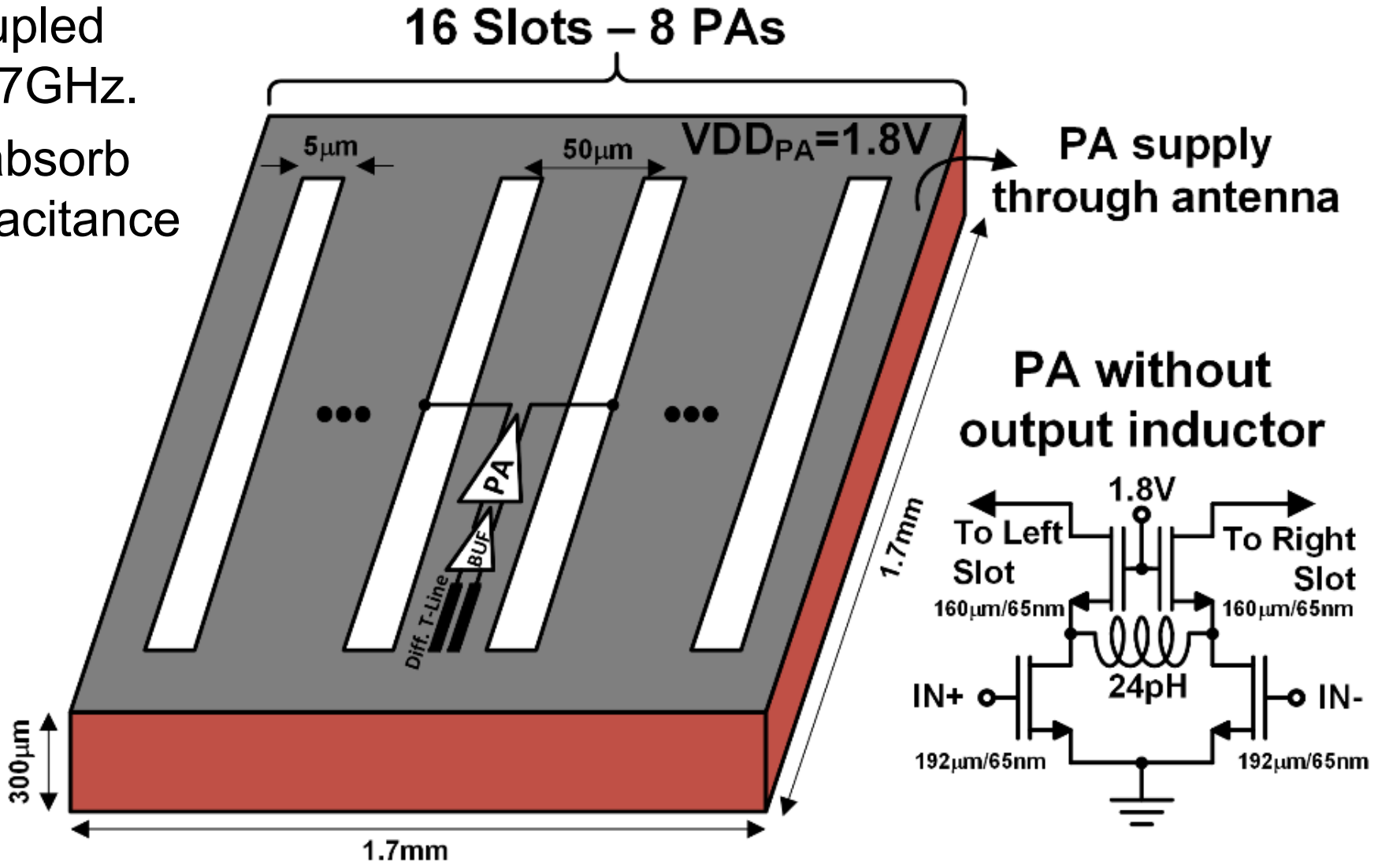
Implemented On-Chip Radiator

- A 16-element tightly coupled slot array designed at 77GHz.
- Slot array designed to absorb the output parasitic capacitance of transistors.
- 8 pseudo-differential pairs drive the 16 slots.
  - Cascode topology.
  - Resonant shunt inductor to resonate cascade node parasitic impedance and improve efficiency.
  - Biased by the antenna, no loss in RF choke.



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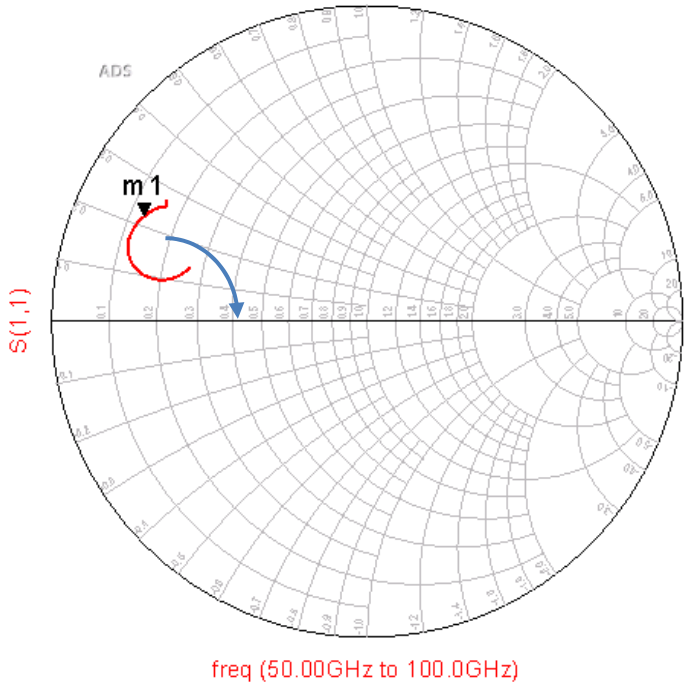
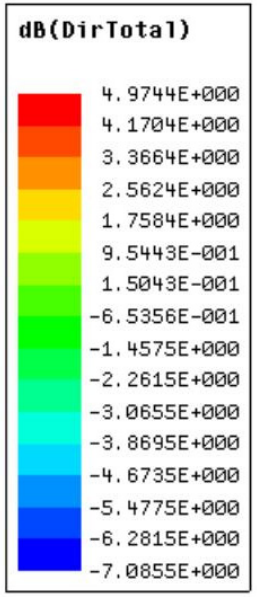
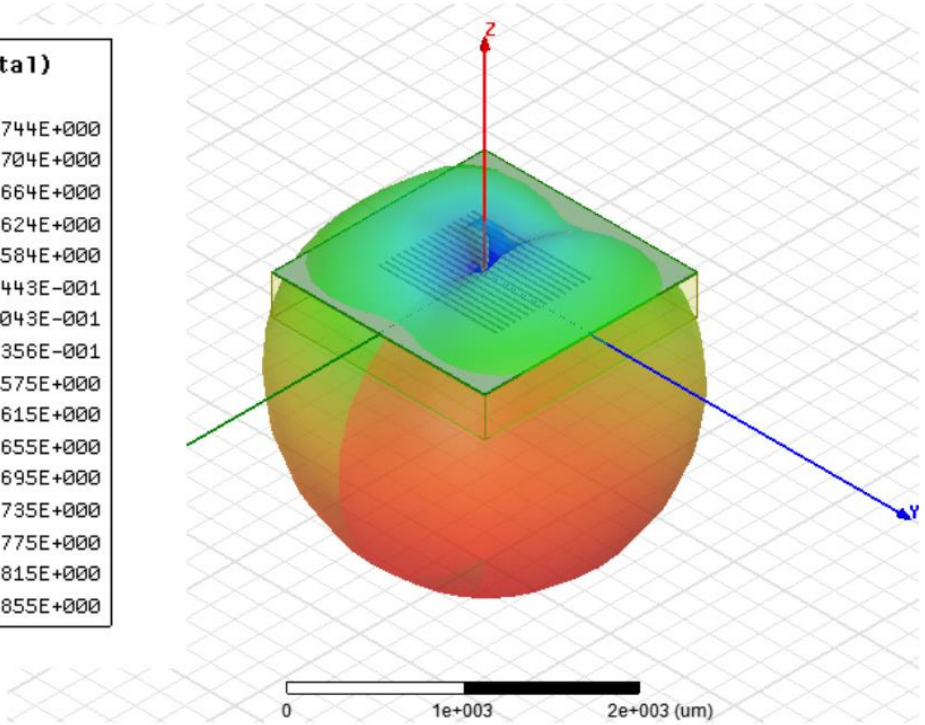
Simulated Impedance & Radiation Pattern



m1
freq=77.00GHz
S(1,1)=0.781 / 154.711
admittance = Y0 * (1.974 - j3.375)





- Antenna Impedance is 6.4+j11Ω which transforms to 25Ω after absorption of PA parasitic capacitance.
- Antenna maintains low Q (i.e. good radiation) over wide frequency range.
- Radiation from bottom of the chip.
  - 46% radiation efficiency, 5dBi Directivity (no lens/heat spreader).

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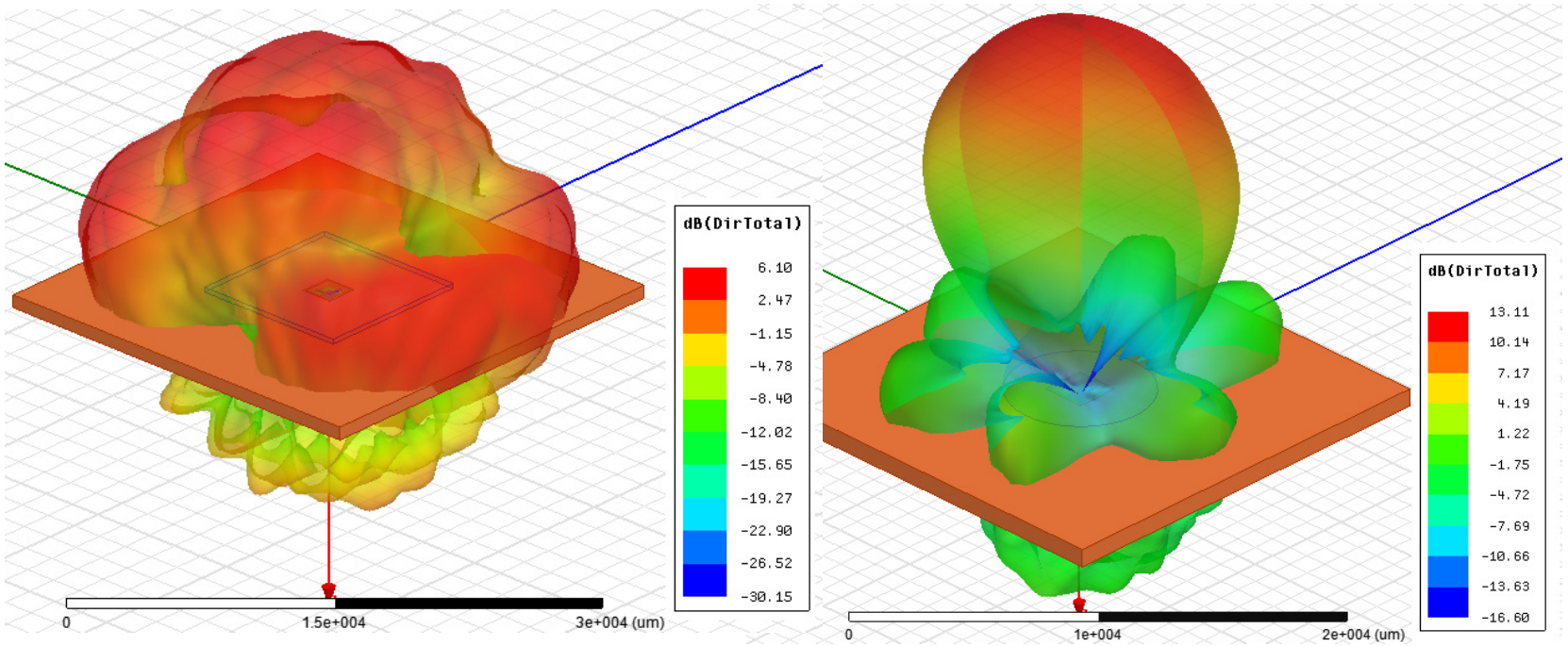
Effect of Heat Spreader on Radiation Pattern

Radiation pattern with planar dielectric heat spreader (1cmx1cmx0.3mm)



Radiation pattern with hemispherical dielectric heat spreader. (d=6.35mm)

- Substrate heat removal only possible with dielectric materials.
- A rectangular shaped planar heat spreader distorts the radiation pattern.
- Aluminum oxide half-ball heat spreader shows no radiation pattern distortion.
- Alumina half-ball forms a dielectric lens improving directivity to 13dBi at 73GHz.
- Radiation efficiency improves from 46% to 51%.

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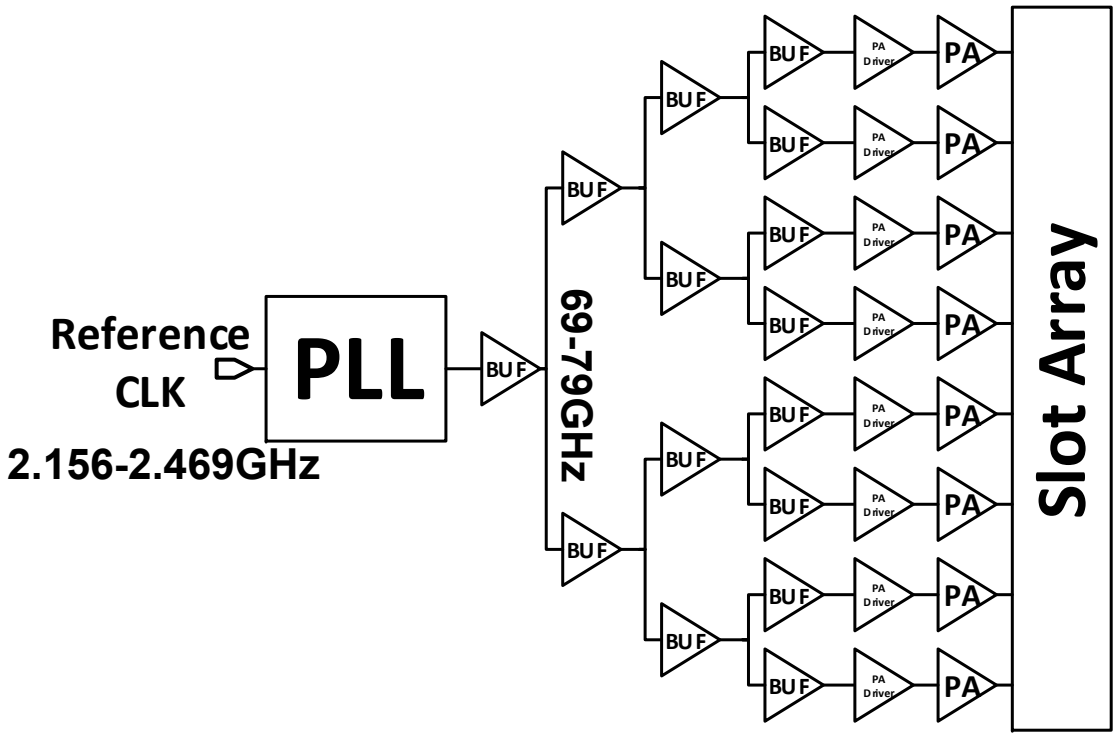
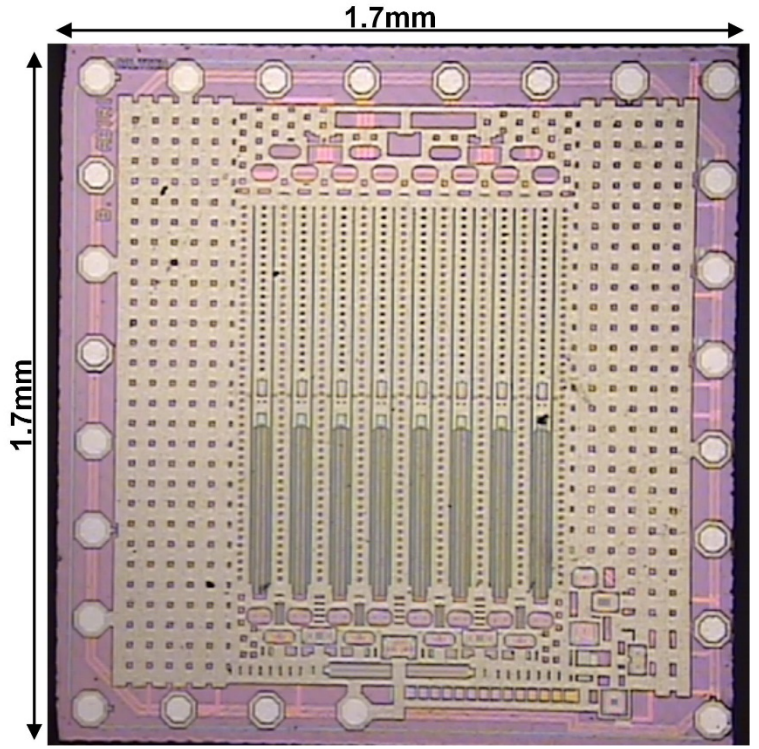
Implementation





- IC implemented in 65nm Bulk CMOS process.
- Radiator integrated with wide tuning range PLL.
- PLL allows synthesized chirp generation for radar applications.
- PLL also allows phase locking of multiple TX chips.

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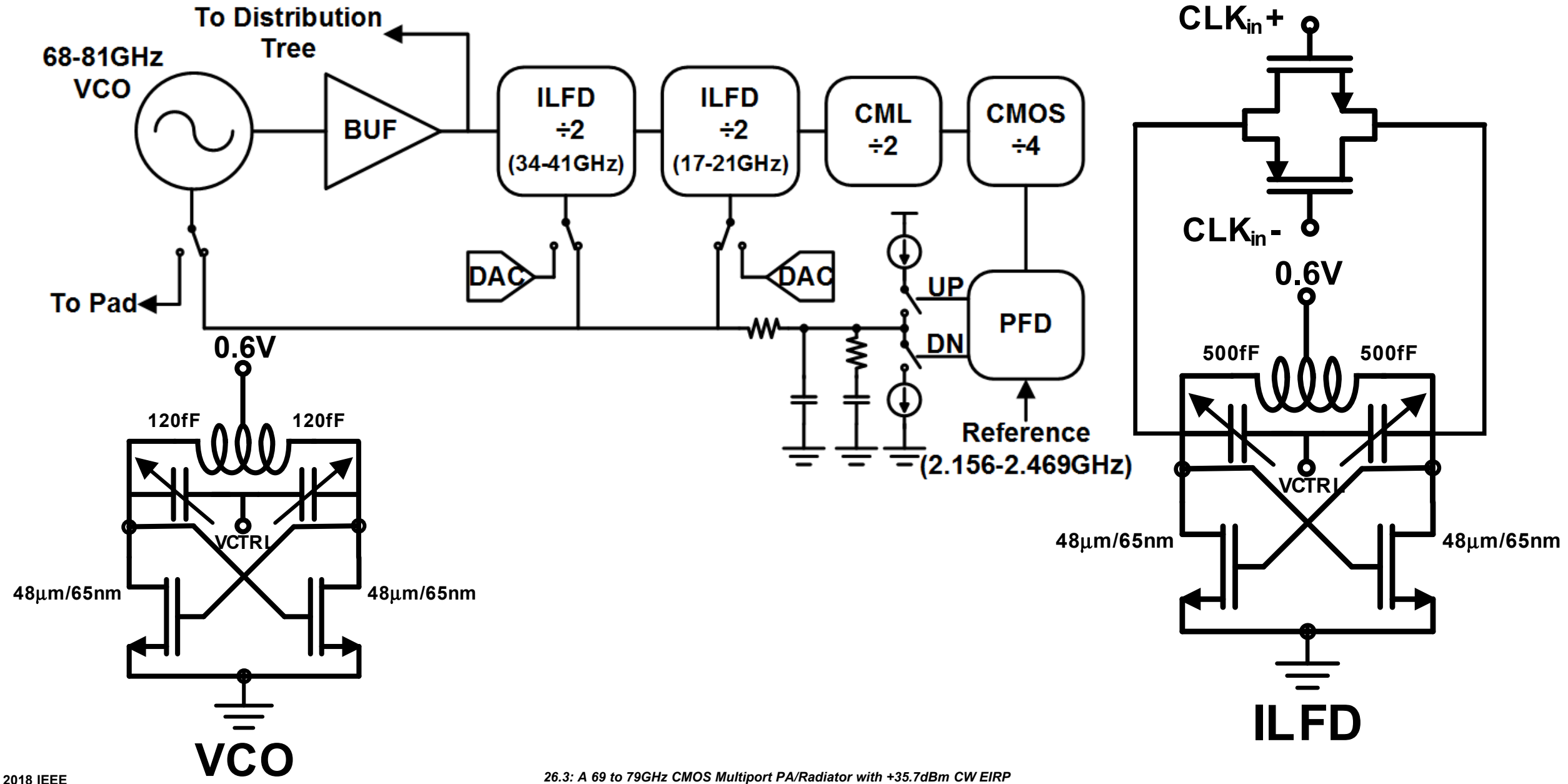
PLL Implementation



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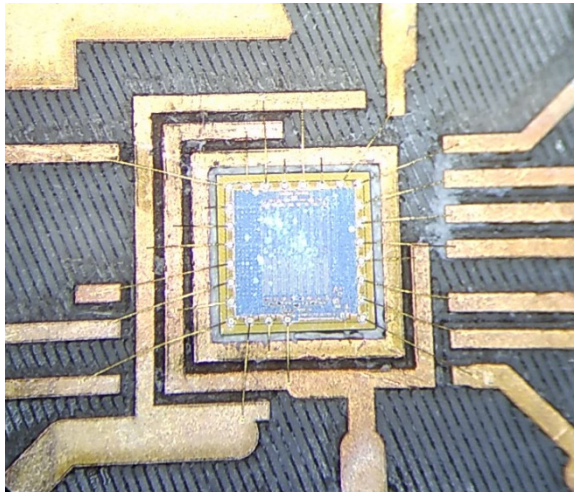
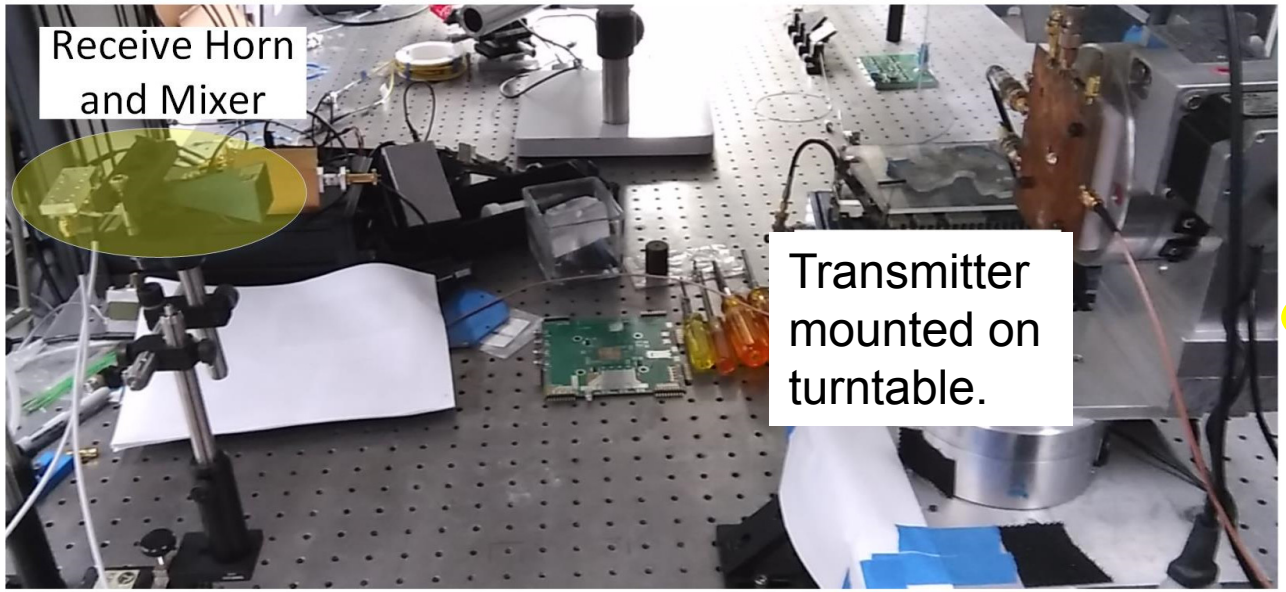
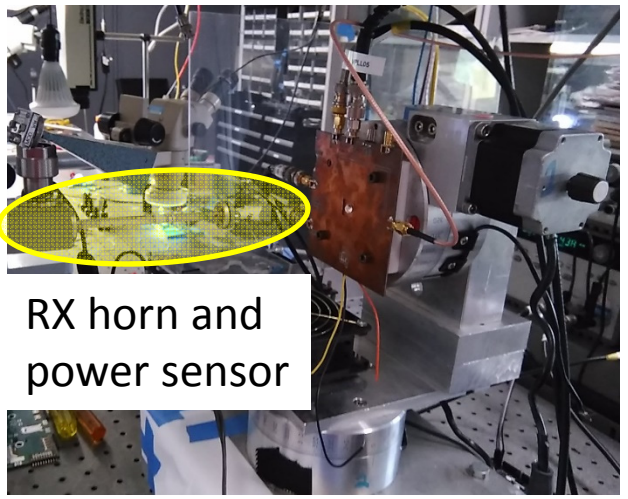
Measurement Setup







- PCB fabricated with cut for the chip.
- EIRP measurements utilized Agilent V8486A and W8486A Power sensors.
- Spectrum measurement performed by down-converting the signal using a fifth harmonic diode mixer.

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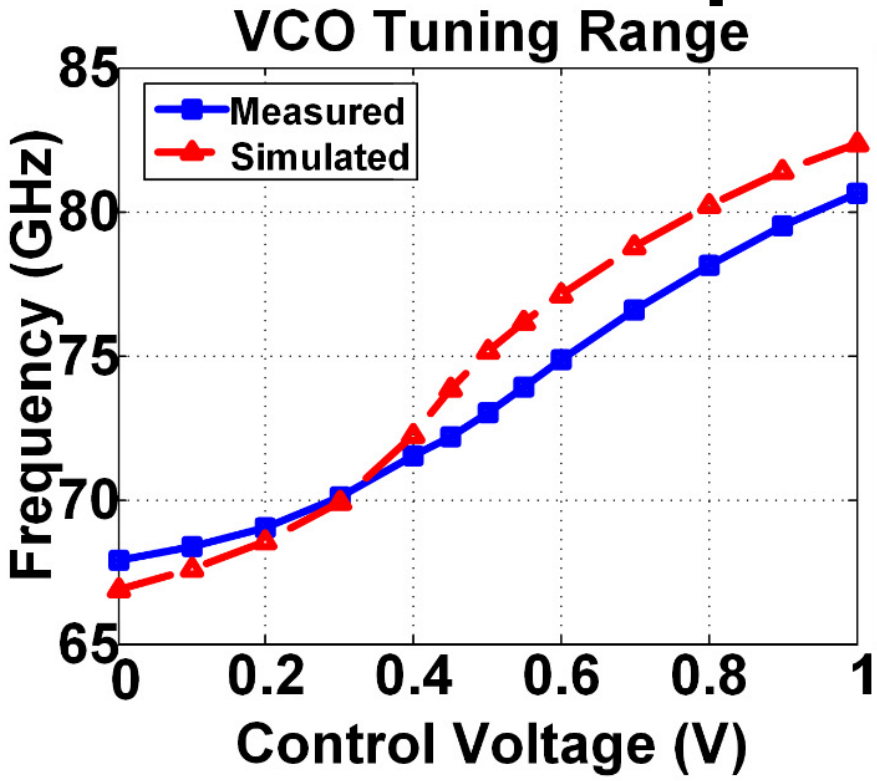
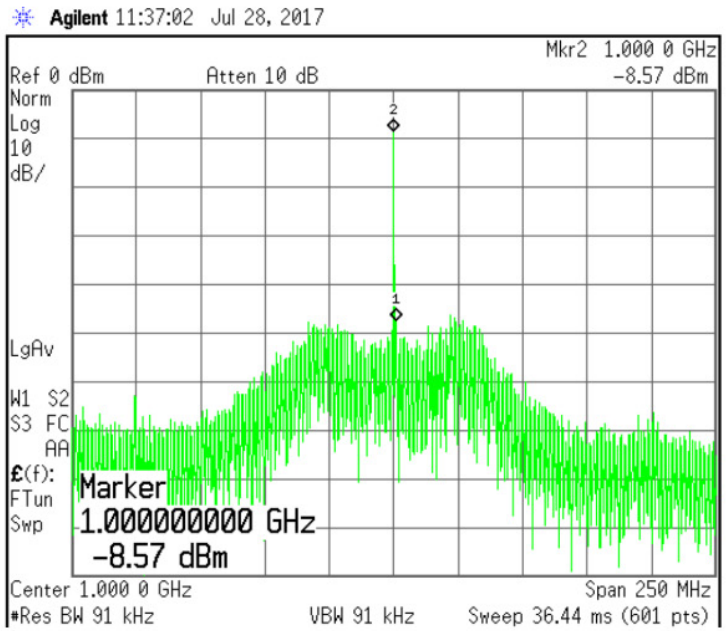
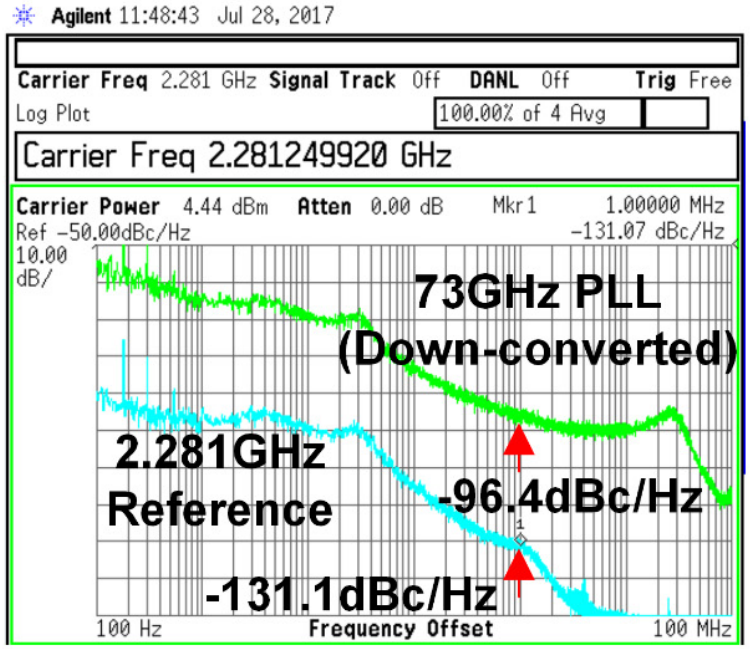
Spectrum Measurement





Measured spectrum of down-converted 73GHz radiation locked to reference.



Measured phase noise of reference and PLL down-converted spectrum.

- Measured VCO tuning range from 68GHz to 80.5GHz closely follows simulation.
- PLL locking range is from 69GHz to 79GHz.
- PLL phase noise is -96.4dBc/Hz at 1MHz offset.

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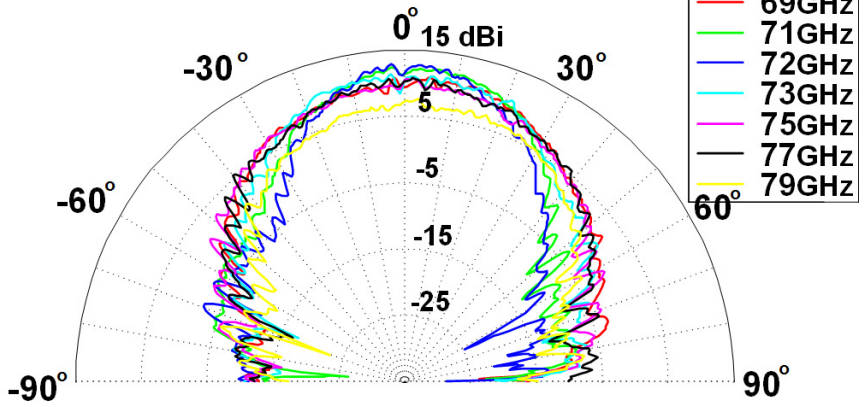
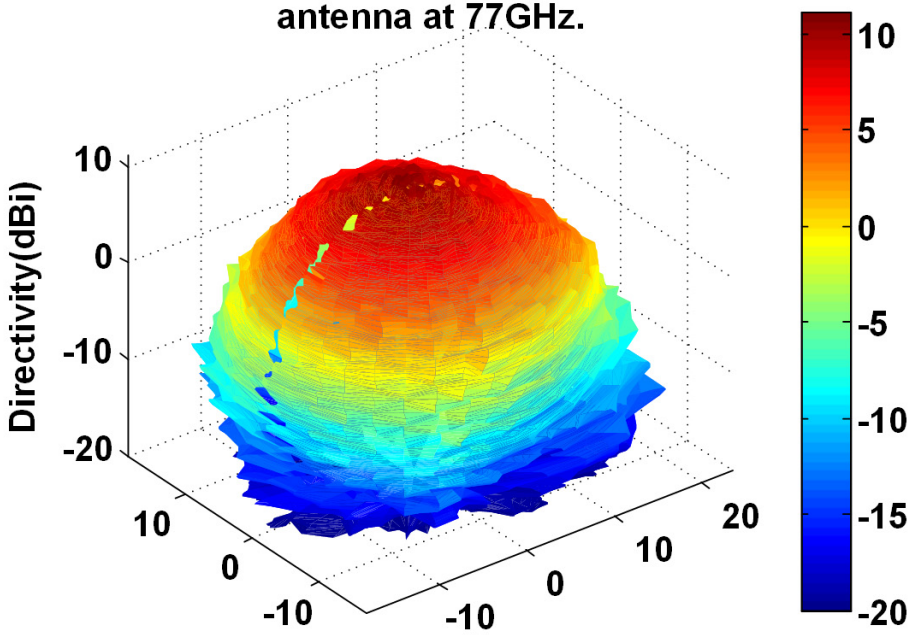
Pattern measurements

- Full 3D pattern measurement.
- Directivity and total radiated power directly obtained.

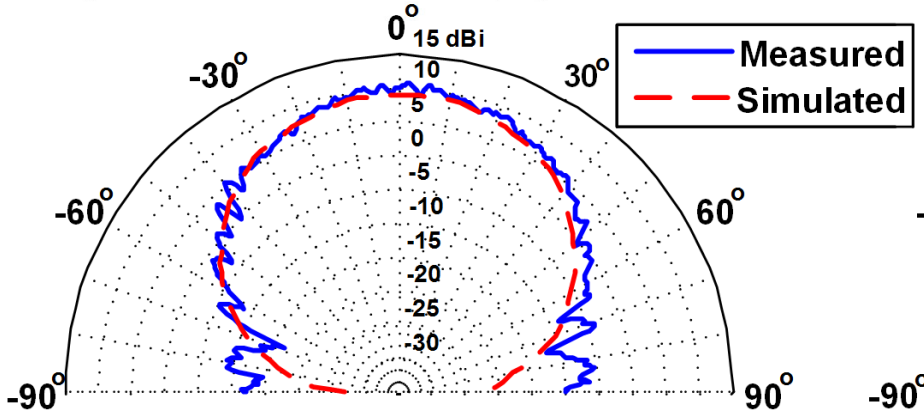
Measured directivity pattern of the on-chip antenna from 69GHz to 79GHz for ϕ=0° cut.



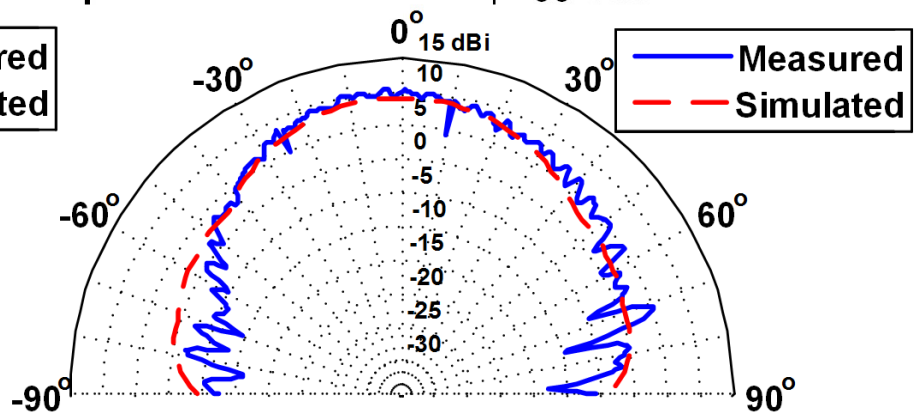
Measured directivity pattern of the on-chip antenna at 77GHz.



Measured vs. simulated directivity of the on-chip antenna at 77GHz for ϕ=0° cut.



Measured vs. simulated directivity of the on-chip antenna at 77GHz for ϕ=90° cut.



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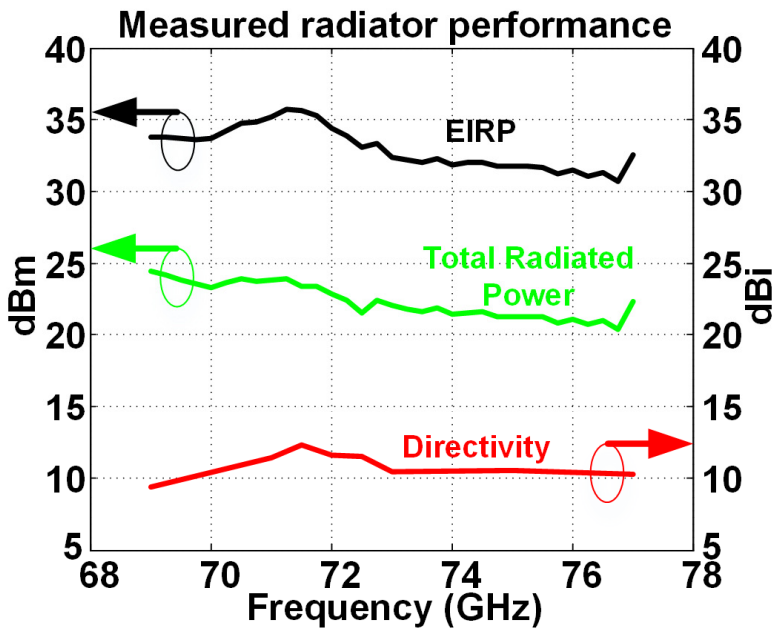
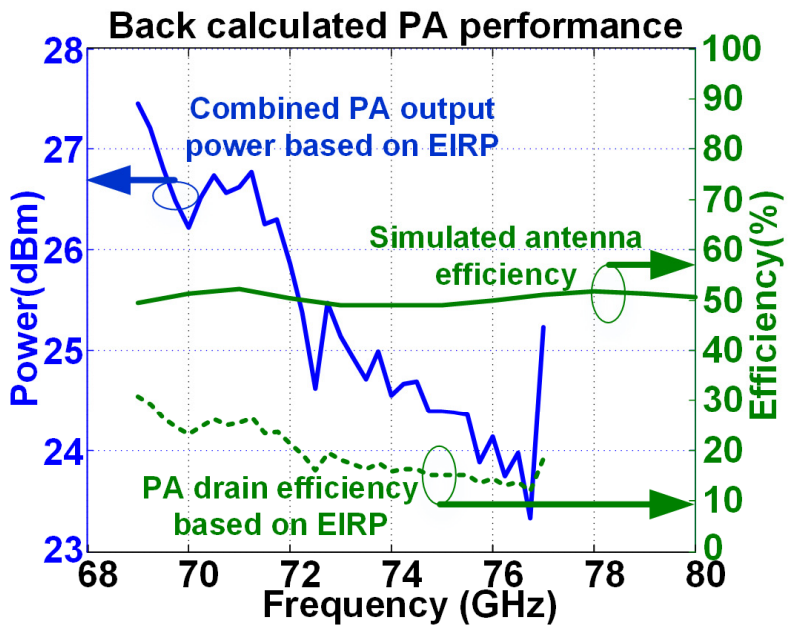
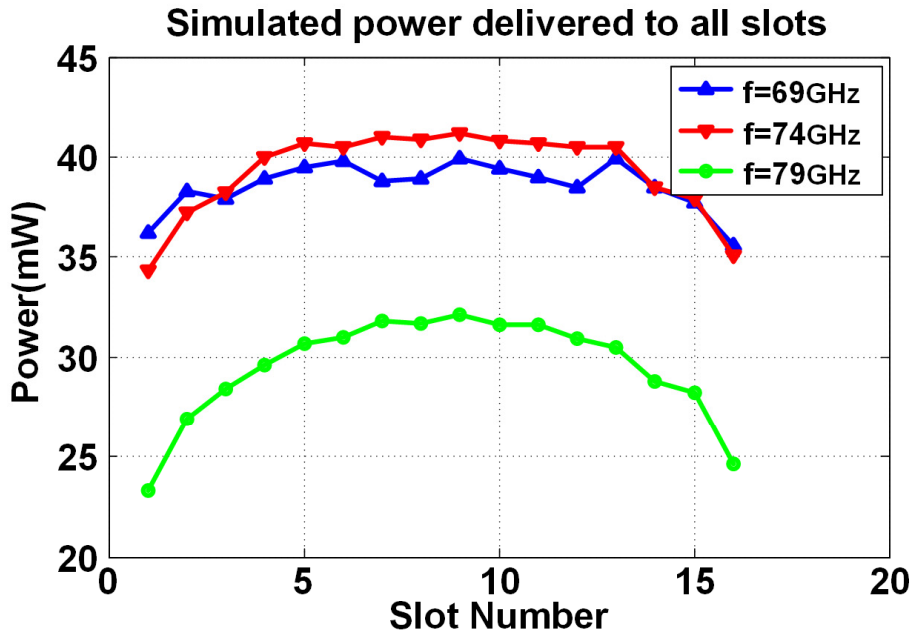
EIRP, TRP, and PA Power Measurement







- EIRP measured by subtracting horn antenna gain and removing free space loss from measured power at 3 different distances.
- Total radiated power was obtained by subtracting measured directivity from EIRP.
- Using simulated antenna efficiency, combined PA output power and efficiency is calculated.
- Not all PAs contribute equally. The difference is small.

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Table of Comparison

	[1]	[2]	[3]	[4]	[5]	**This Work**
Process	45nm SOI	32nm SOI	180nm SiGe	32nm SOI	65nm CMOS	**65nm CMOS**
Frequency(GHz)	53-63	58.3-60.5	108-114	134.5	88-99	**69-79**
EIRP(dBm)	33.1	17.1	24.5	6.0	35	**35.7**
On Chip Antenna	YES	NO	NO	YES	NO	**YES**
Radiator Directivity (dBi)	6.9	32.5	17	7.1	36 (Dish Antenna)	**12.2 @ 77GHz (Alumina Lens)**
Tot. Rad. Power (dBm)	26.2	N/A	7.5	-1.3	0	**24.4**
Radiation Efficiency	74.5% (Uses H. R. Substrate)	N/A	45%	39%	N/A	**52%**
PA Psat(dBm)	27.9	N/A	11	N/A	N/A	**27.4**
PA Efficiency	23.4% (PAE)	N/A	N/A	N/A	N/A	**30.75% (Drain Eff.)**
Phase Noise (dBc/Hz)	N/A	-113 @10MHz	N/A	N/A	-85.6 @1MHz	**-96.4@1MHz**
Total DC Power(W)	N/A	0.23	3.4	0.17	0.6	**PA+PLL/Distrib 1.81+0.55=2.36**
Chip Area(mm^2)	10.5	9 (RX+TX)	39	1.2	4.32 (RX+TX)	**2.9**

- [1] T. Chi et al., "17.3 A 60GHz on-chip linear radiator with single-element 27.9dBm Psat and 33.1dBm peak EIRP using multifeed antenna for direct on-antenna power combining," 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2017, pp. 296-297.
- [2] B. Sadhu et al., "A 60GHz packaged switched beam 32nm CMOS TRX with broad spatial coverage, 17.1dBm peak EIRP, 6.1dB NF at < 250mW," 2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), San Francisco, CA, 2016, pp. 342-343.
- [3] W. Shin et al., "A 108–114 GHz 4x4 Wafer-Scale Phased Array Transmitter With High-Efficiency On-Chip Antennas," in IEEE Journal of Solid-State Circuits, vol. 48, no. 9, pp. 2041-2055, Sept. 2013
- [4] S. M. Bowers, A. Safaripour and A. Hajimiri, "An integrated traveling-wave slot radiator," 2014 IEEE Radio Frequency Integrated Circuits Symposium, Tampa, FL, 2014, pp. 369-372.
- [5] P. N. Chen et al., "A 94GHz 3D-image radar engine with 4TX/4RX beamforming scan technique in 65nm CMOS," 2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers, San Francisco, CA, 2013, pp. 146-147.

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- Special thanks to Dr. Florian Bohn for helpful discussions.
- Dr. Amirreza Safaripour for assistance in measurement.
- Members of CHIC group for support and feedback.
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A 28GHz 41%-PAE Linear CMOS Power Amplifier Using a Transformer-Based AM-PM Distortion-Correction Technique for 5G Phased Arrays

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Outline

- Motivation
- Related prior arts
- Linear power amplifier (PA) architecture
- Measurement and simulation results
- Comparison
- Summary

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Motivation

- PAs for mmW 5G phased arrays expect to support:
  - High-order QAM signals with large channel bandwidth for high data-rate (e.g., 64, 512-QAM)
  - High-efficiency for longer battery life
  - High-linearity for low EVM and ACPR
    - Low AM-PM and AM-AM distortion
  - Use of silicon technology for low-cost
  - Highly robust architecture (e.g., high stability, PVT resilient)

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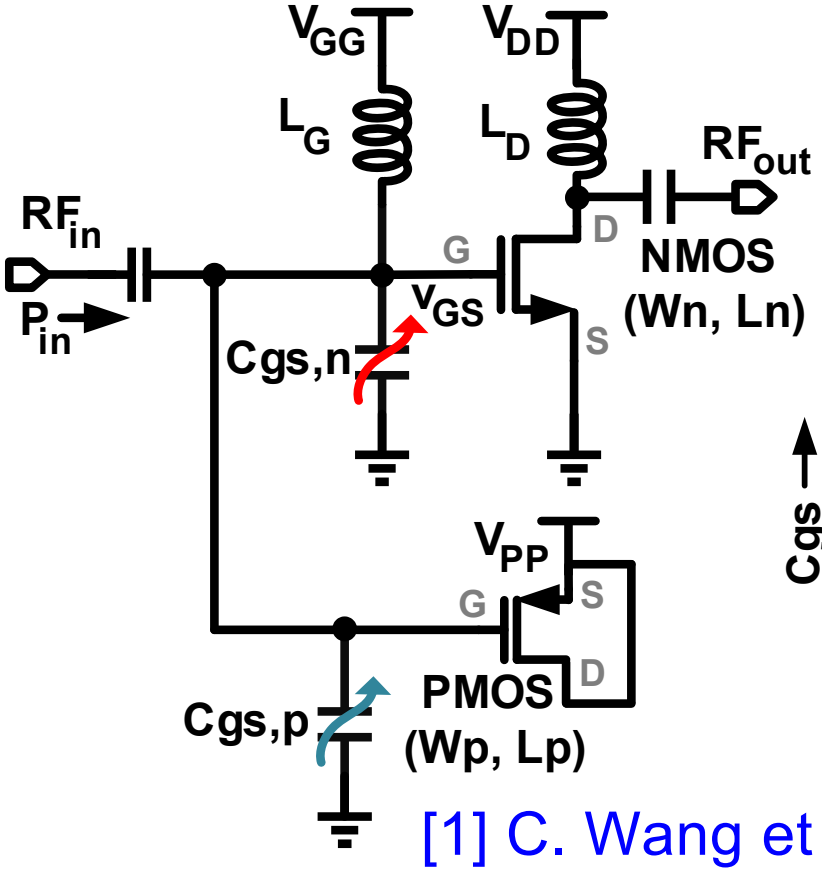
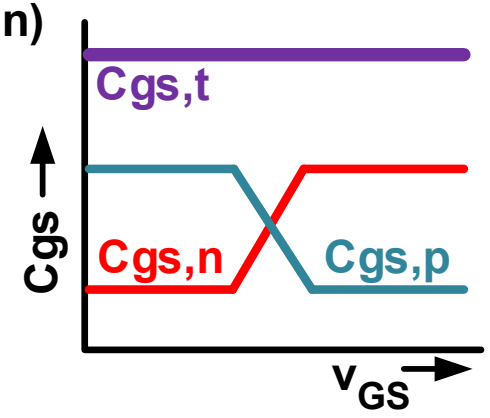
Related Prior Arts: AM-PM Cancellation

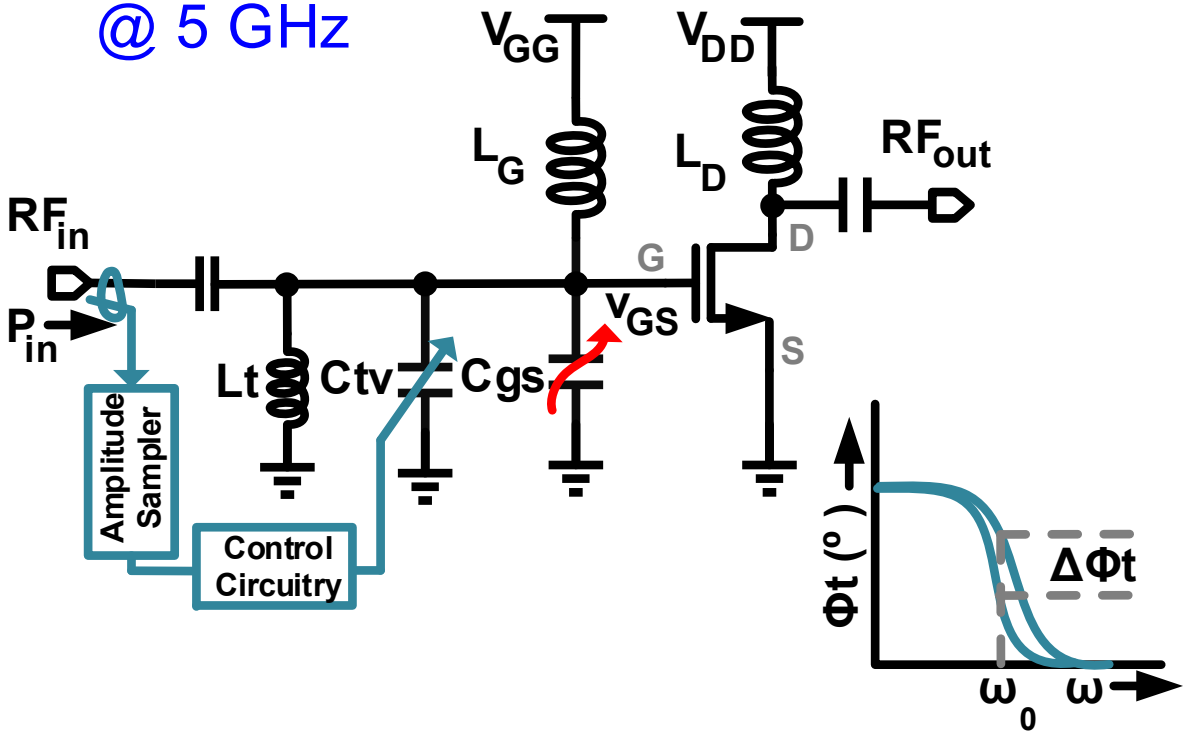


@ 1.75 GHz



[1] C. Wang et al., JSSC 2004

@ 5 GHz



[2] Y. Palaskas et al., JSSC 2006

- Gain and efficiency reduction in capacitive approaches
- Baseband operation
- Requires control circuitry

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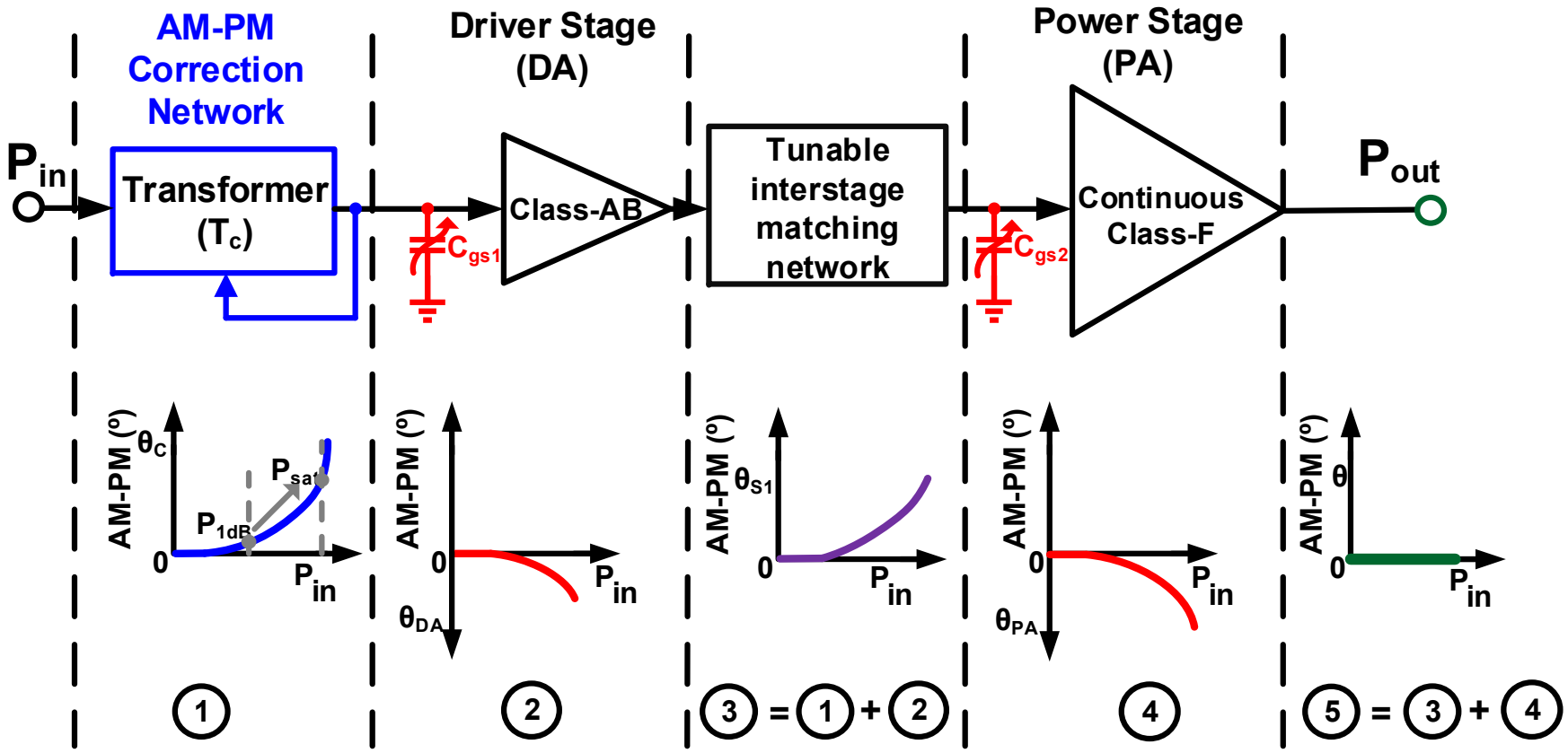
Linear PA Architecture



- θ_C: Phase of AM-PM correction network
- θ_{DA}: Phase of driver stage (DA)
- θ_{S1}: Phase after 1st stage
- θ_{PA}: Phase of power stage (PA)

- Non-linear C_{gs1} & C_{gs2} create phase distortion at large-signal input power
- AM-PM correction network compensates phase non-linearity over 2-stage
- Phase conditions: (i) $|\theta_C| > |\theta_{DA}|$, (ii) $\theta_{S1} = \theta_C + \theta_{DA}$, (iii) $\theta_{PA} = -\theta_{S1}$

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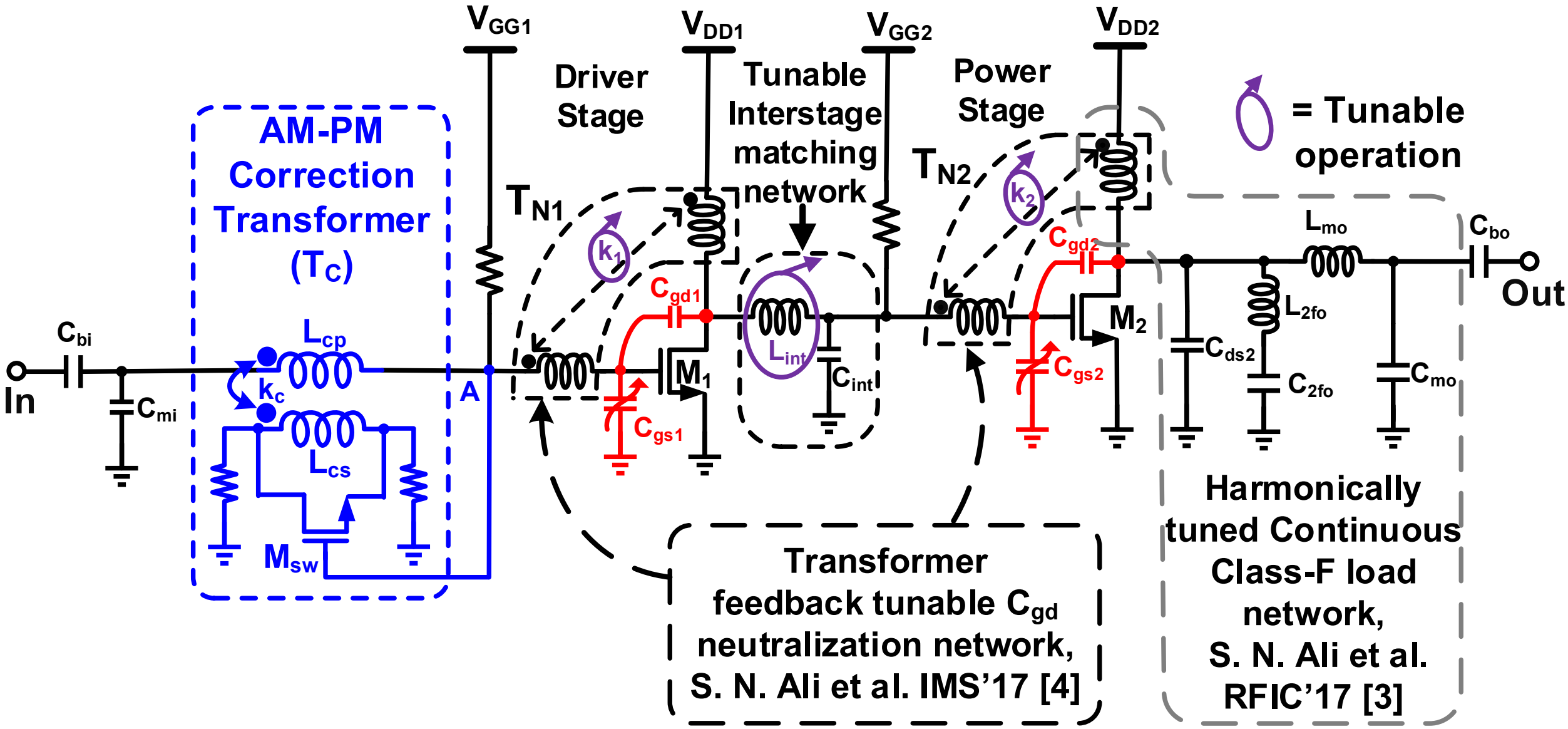
PA Architecture: Schematic



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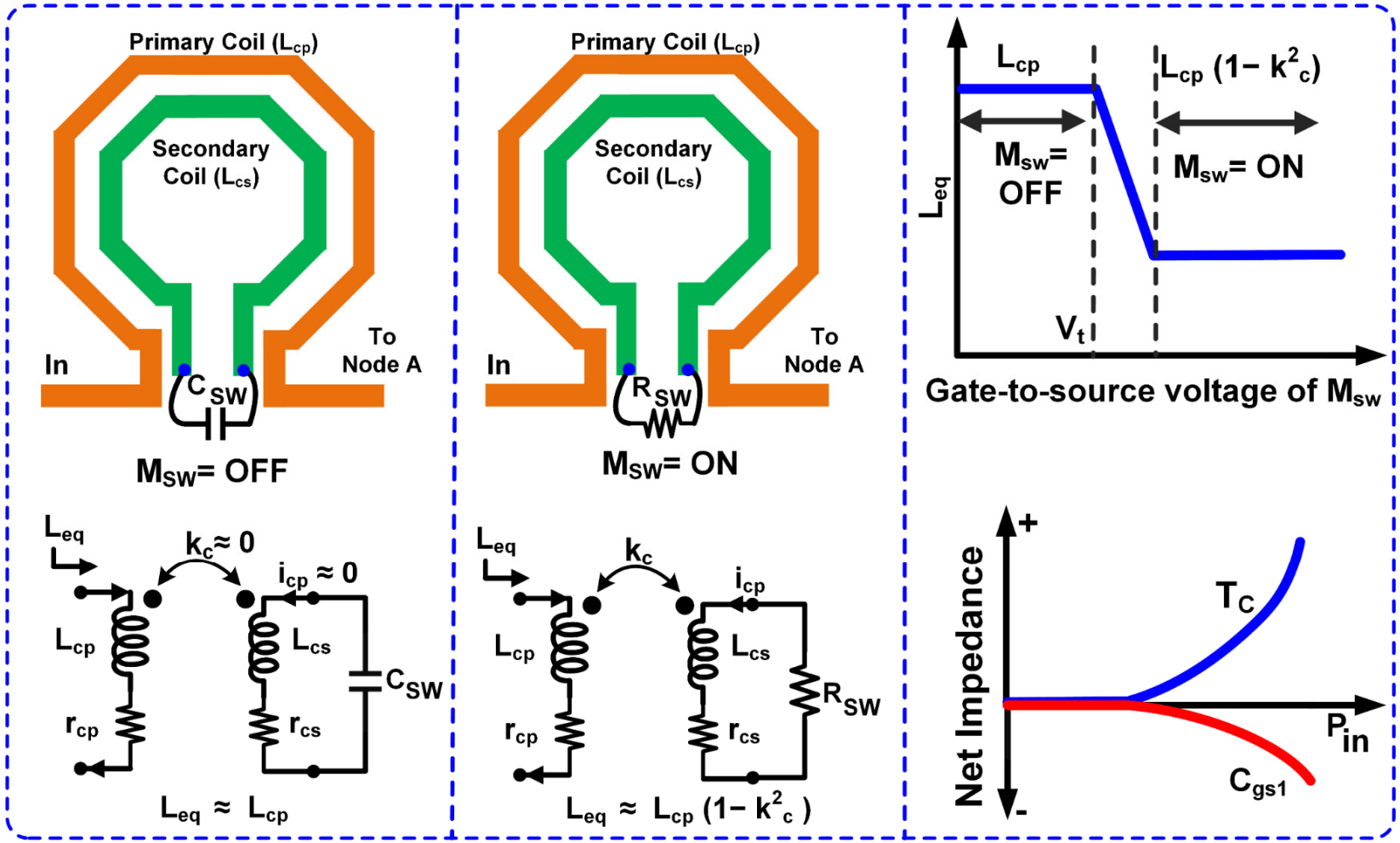
AM-PM Correction Transformer



- Transformer (T_C) creates opposite-shaped impedance of Z_{Cgs1}

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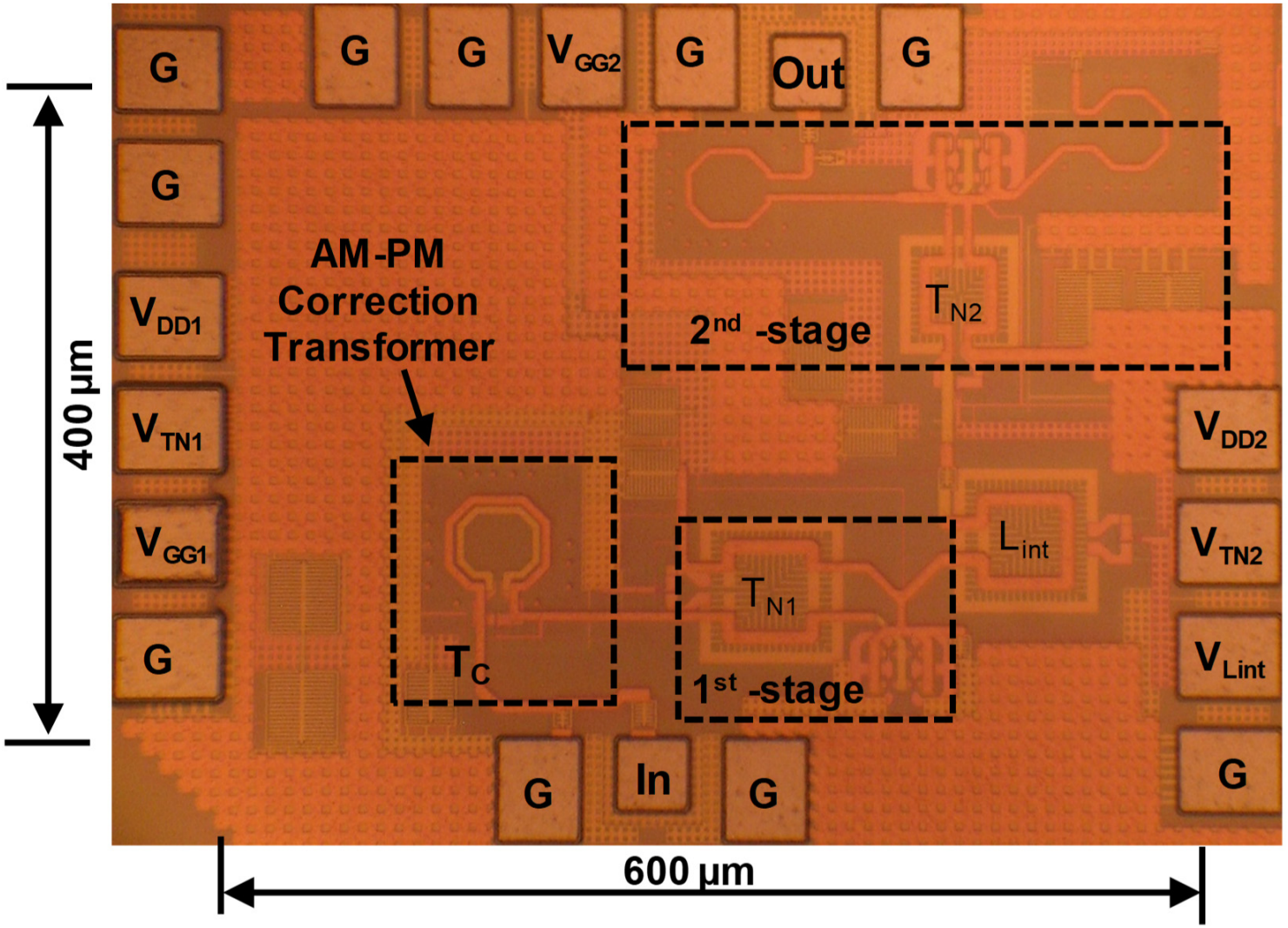
Die Micrograph



- Technology: 65nm CMOS
- Active area: 0.24 mm^2

- V_{TN1} & V_{TN2}: control voltage for tunable transformers
- V_{Lint} : control voltage for tunable inter-stage matching

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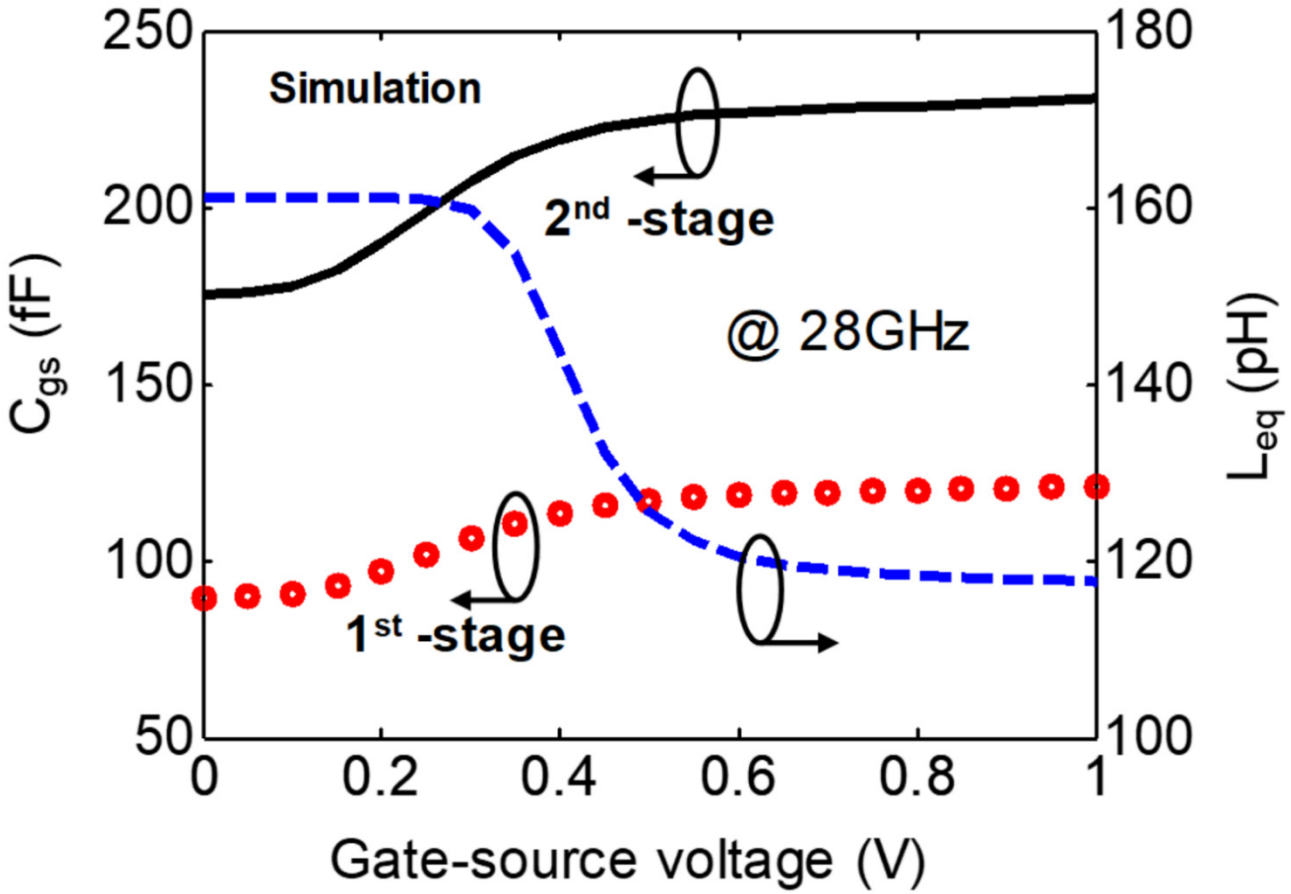
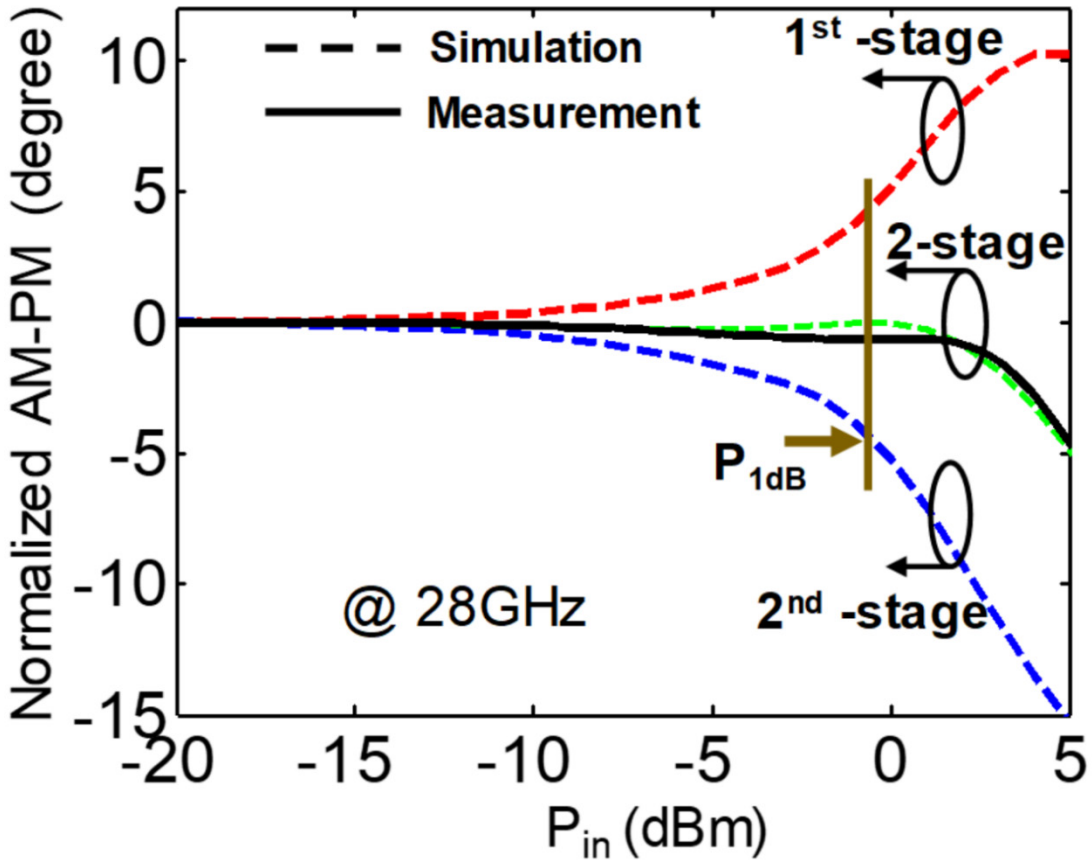
Results: C_{gs}, L_{eq} and AM-PM Distortion





- Measured |AM-PM| ≈ 0.7° @ P_{1dB}

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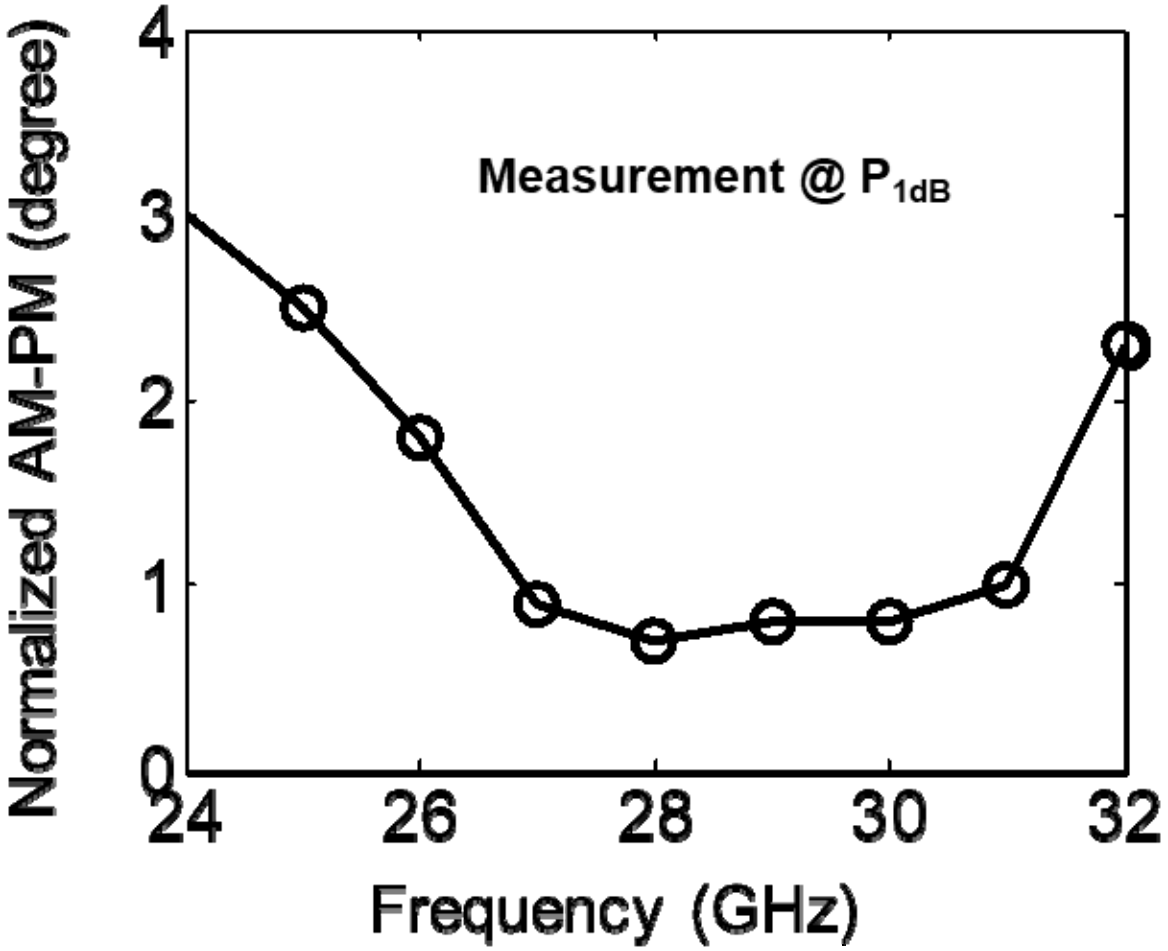
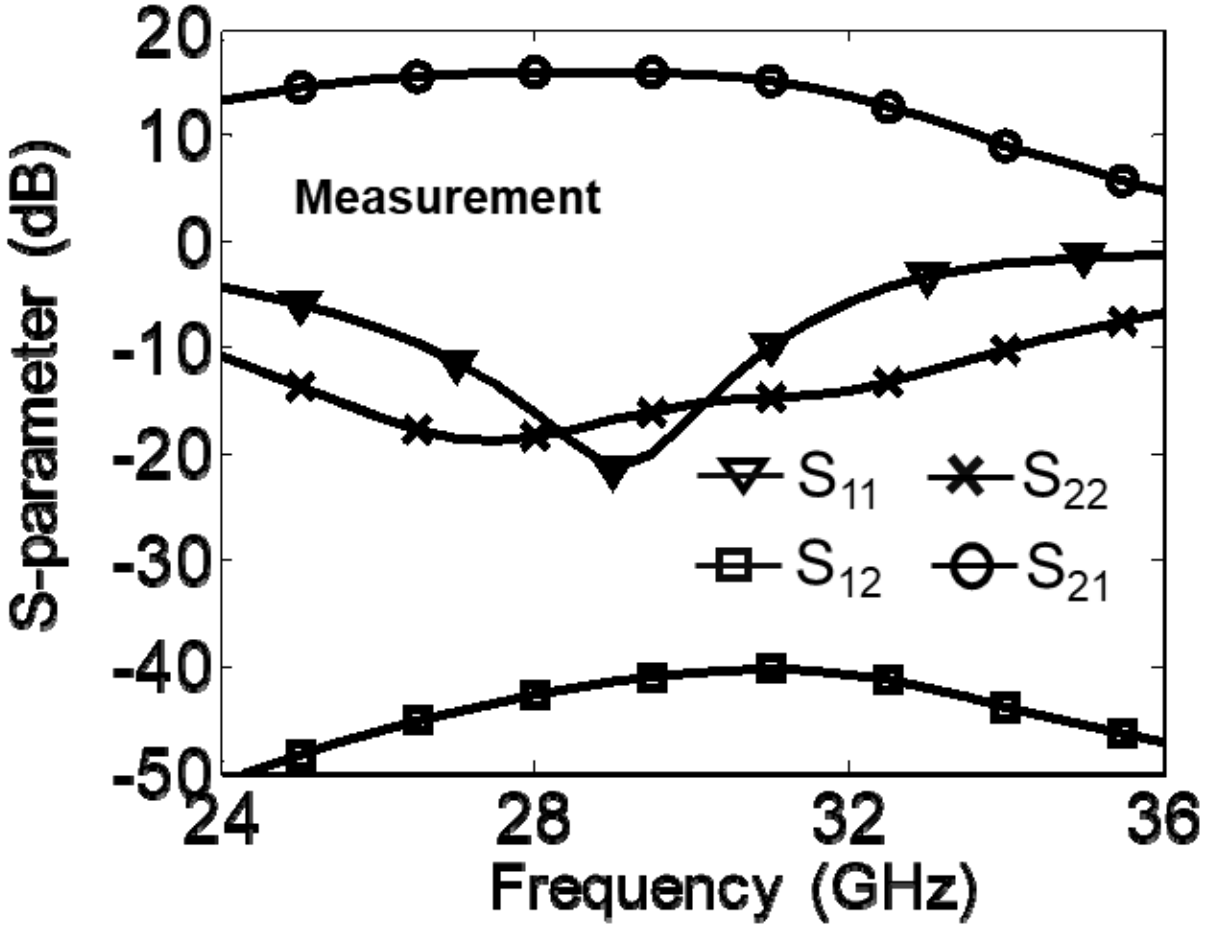
Measured Results: AM-PM & S-Parameters





- Measured |AM-PM| <1^{o} from 27-31GHz @ P_{1dB}

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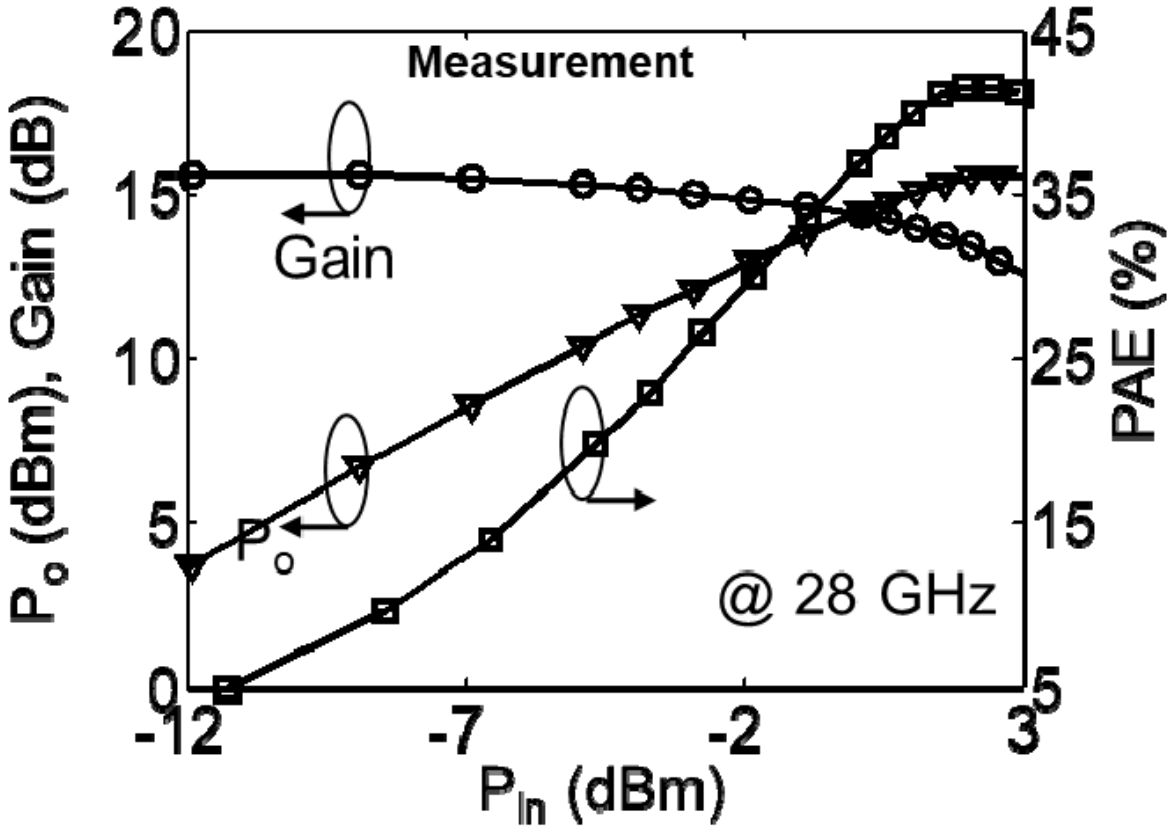
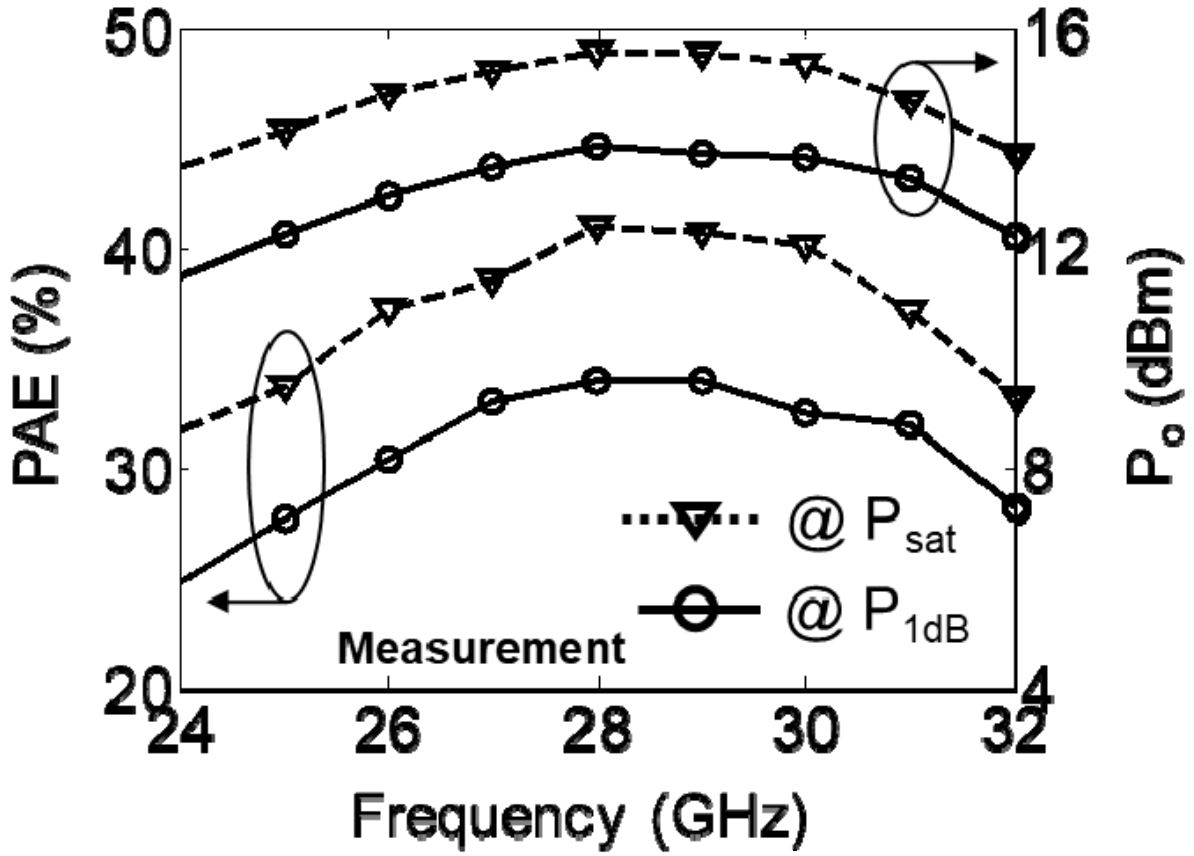
Measured Results: Large-Signal





- Peak PAE ≈ 41% @ 28GHz
- Peak P_{sat} ≈ 15.7dBm from 29GHz

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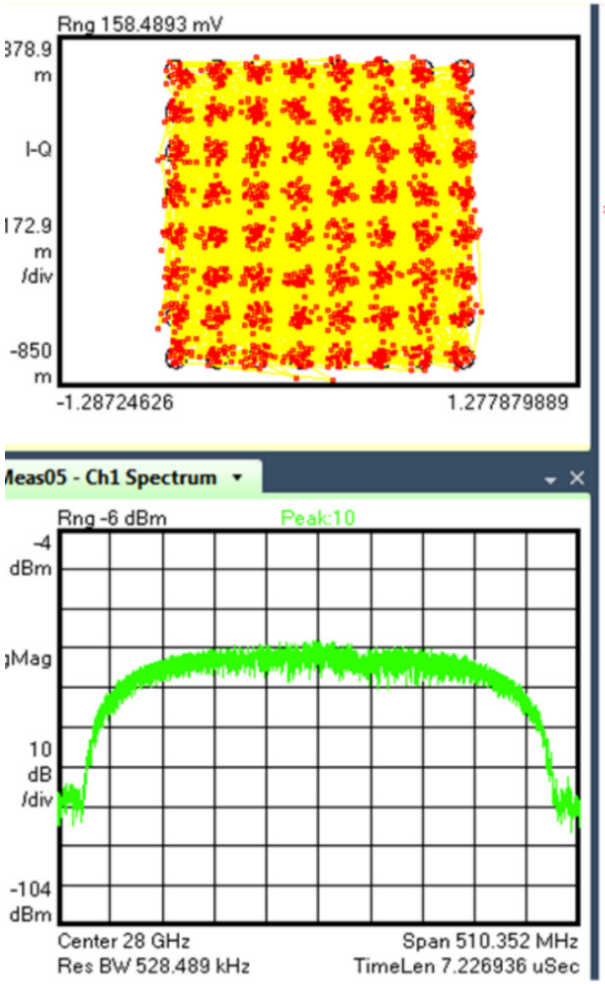
Measured Results: EVM and ACPR (1)

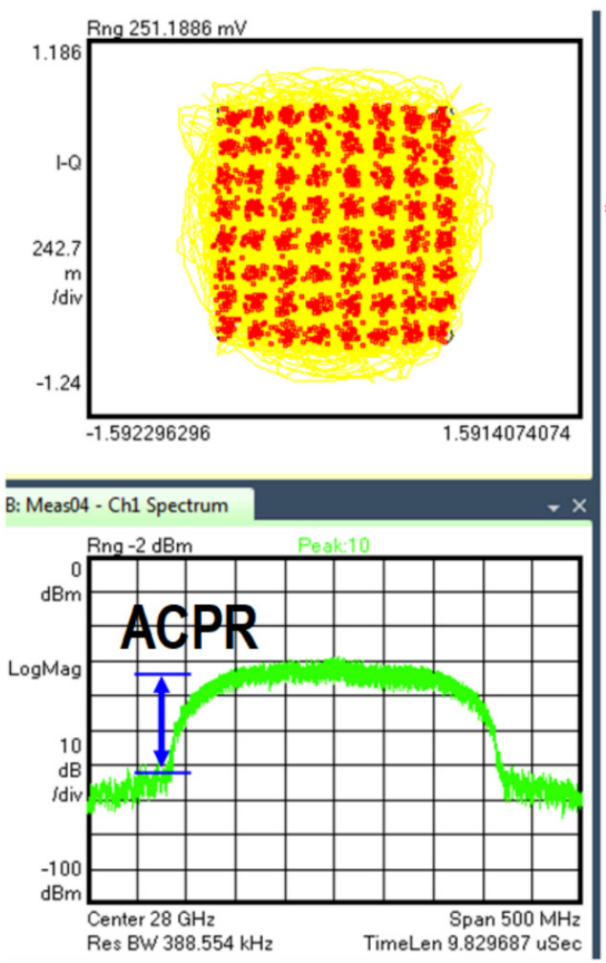



```
EVM        = 4.8078    %rms     13.710     % pk at sym
Mag Err    = 3.4340    %rms     -13.705    % pk at sym
Phase Err  = 4.6066    deg      31.496     deg pk at sym
Freq Err   = 409.06    Hz
IQ Offset  = -50.824   dB       SNR (MER) = 22.677
Quad Err   = 157.46    mdeg     Gain Imb  = 0.106

  0 35143F31 3E133106 15013D33 2A053B1B 1213(
 44 2C310015 3D3B2B15 333A071B 0A103919 0605(
 88 0B063104 15153F3B 3F173B2F 151B3E17 312E1
```

64-QAM
340MSymbol/s
$P_{o,avg}$ = 9.8dBm
PAE = 18.2%
EVM = -26.4dB (4.9%)
ACPR = -30dBc

```
 968 35323A0D 1A0E1A10 191C0627 06090225 2E191
1012 092E2116 37242C13 05011D36 2A273E0F 321E(
1056 340C3600 233A271E 0A323C0D 2608022F 2F1D1
1100 0B143330 061F0039 39030521 18360822 2A2F3
1144 0D2A093A 231E2236 2C270209 2A213E33 34063
1188 3A111916 07230C20 023F2D3D 0B2C3500 3D392
1232 1E02332C 05071D0A 2C3F0139 3302012B 31361
```




```
EVM        = 5.2438    %rms     13.986     % pk at sym  10
Mag Err    = 3.8312    %rms     -13.636    % pk at sym  16
Phase Err  = 4.7911    deg      37.095     deg pk at sym  17
Freq Err   = -640.86   Hz
IQ Offset  = -50.545   dB       SNR (MER) = 21.913      dB
Quad Err   = 148.72    mdeg     Gain Imb  = 0.095      dB

  0 16052318 220A2A3F 3D3F2B3D 372A2D3F 0B383710
 44 08262A07 3B0F101B 1C12250E 1C10251A 1E183010
 88 37342E33 14033726 2D070709 08242A13 39070509
 13
 17
 22
 26
 30
 35
 39
 44
 48
 52
 57
 61
 66
 70
 74
 79
 83
 88
 92
```

64-QAM
250MSymbol/s
$P_{o,avg}$ = 10.4dBm
PAE = 19.3%
EVM = -25.61dB (5.2%)
ACPR = -29dBc

```
 968 191A061B 00113D13 2F05191E 06330401 17372E2D
1012 28252A19 38030F20 1C3C2122 302C1B04 11151737
1056 21063504 3D112F11 1B161321 0435103F 193A031E
1100 121D082C 2B033126 10011F36 3E25361A 201E3C35
1144 392F0119 3602232E 25161F20 3C392100 35383B09
1188 3F153B3B 17132B05 311A1619 20083F39 3F033927
1232 01293122 10291B26 14012F32 2E0F121B 08102D1E
```

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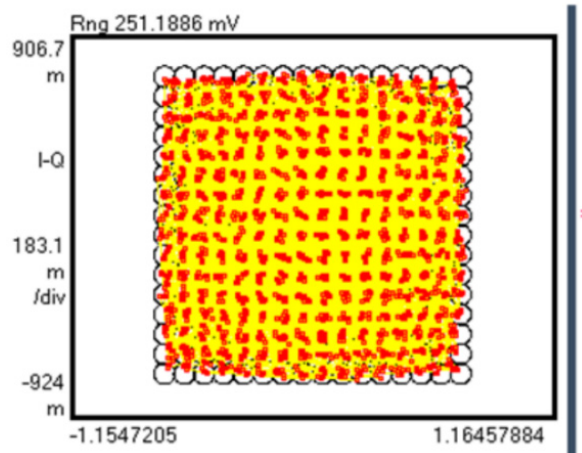
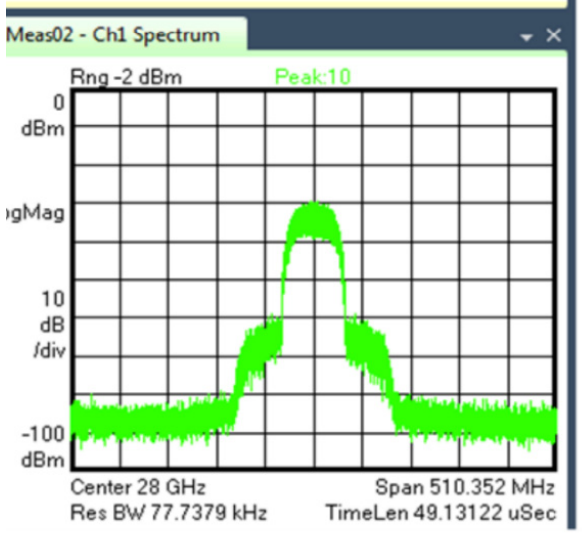
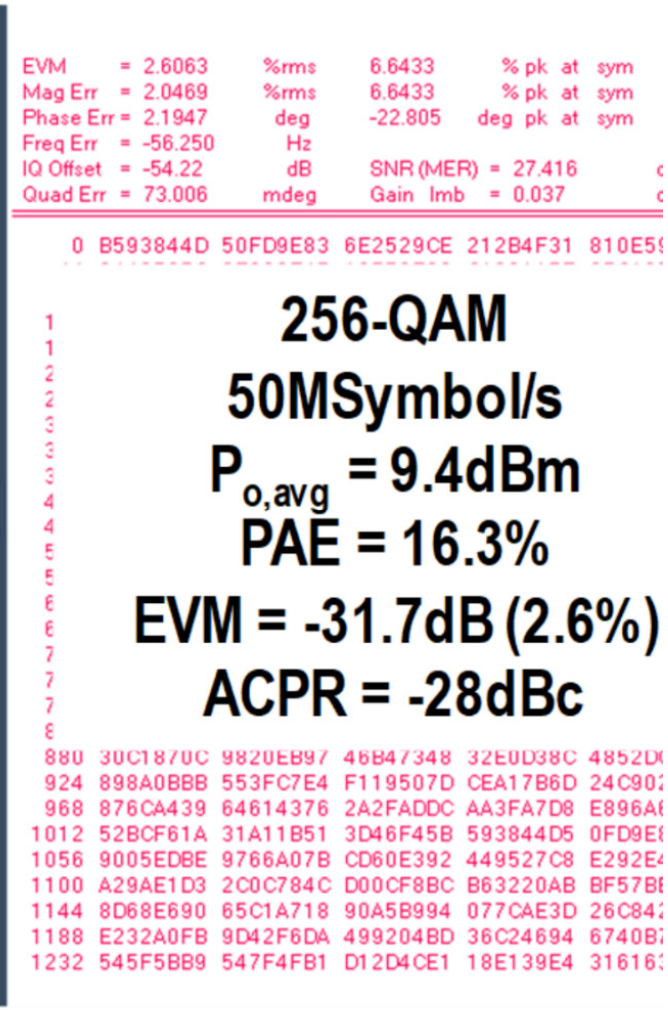
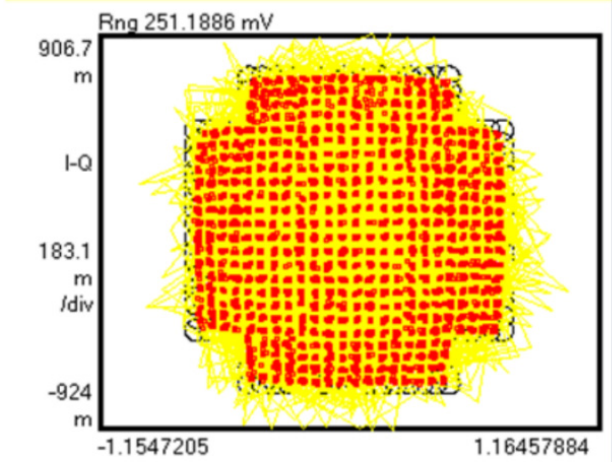
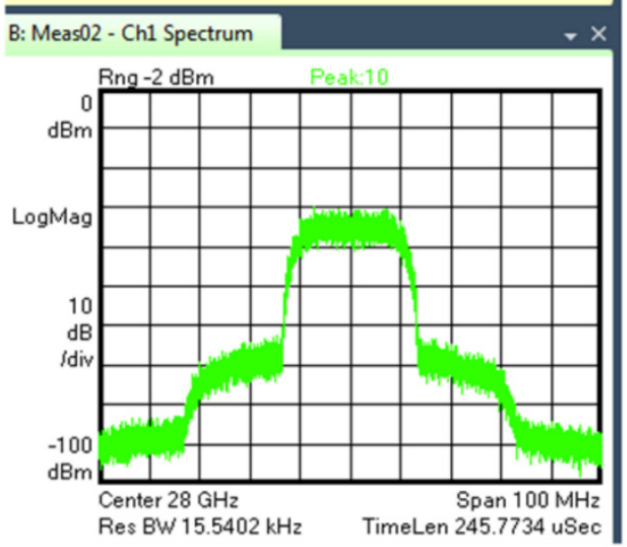
Measured Results: EVM and ACPR (2)

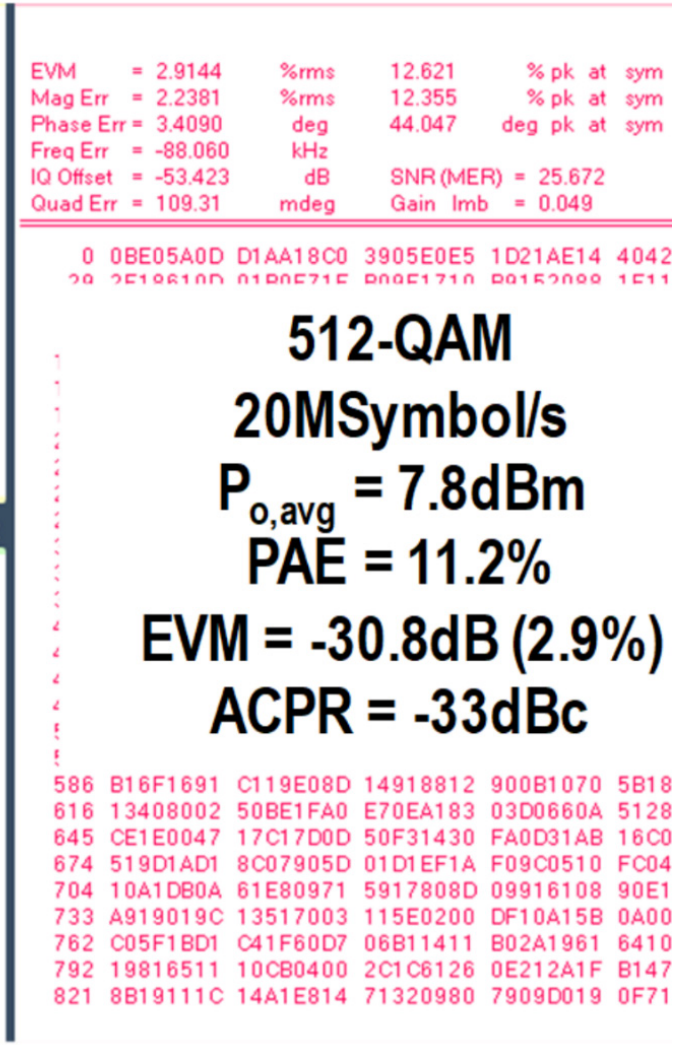












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Comparison

Ref.	This Work	JSSC'16 [6]	ISSCC'17 [7]	TMTT'16 [8]	RFIC'17 [9]
Tech.	65nm CMOS	28nm CMOS	130nm SiGe	28nm CMOS	28nm CMOS
Freq. (GHz)	28	30	28	28	34
V_{DD} (V)	1.1	1.0	1.5	1.1	0.9
Gain (dB)	15.8	15.7	18.2	10	20.8
$P_{o,sat}$ (dBm)	15.6	14	16.8	14.8	16.6
PAE_{1dB} (%)	34.7	34.3	19.5	35.2	12.6
PAE_{max} (%)	**41**	35.5	20.3	36.5	24.2
AM-PM (°) @P_{1dB}	0.7	NA	NA	NA	1.1
Modulated Signal Measured Results [n-QAM, Data-rate $P_{o,avg}$, PAE EVM, ACPR]	64, 340Msym/s **+9.8dBm, 18.2%** -26.4dB, -30dBc	64, 250Msym/s +4.2dBm, 9% -25dB, -26.4dBc	64, 1000Msym/s +7.2dBm, NA -26.6dB, -25.4dBc	64, 80Msym/s +6.8dBm, 16.5% -27.4dB, -34dBc	64, 337Msym/s +10.1dBm, 5.8% -25dB, -32.1dBc
	256, 50Msym/s **+9.4dBm, 16.3%** -31.7dB, -28dBc	NA	NA	NA	NA
Topology	Transformer based AM-PM correction	Inductive source degeneration	Doherty	2nd harmonic short, common-source	PMOS varactor based AM-PM compensation

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Summary

- Transformer based pre-distortion for low AM-PM
- AM-PM correction in mmW domain
- High linearity results with high efficiency
- Capable to operate with high-order QAM (64/256/512) signals
- No additional control circuitry and extra power consumption
- Attractive linear PA solution for silicon based 28GHz 5G phased arrays

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Reference List

[1] C. Wang et al., “A Capacitance-Compensation Technique for Improved Linearity in CMOS Class-AB Power Amplifiers,” *IEEE JSSC*, vol. 39, no. 11, pp. 1927-1937, Nov. 2004.

[2] Y. Palaskas et al., “A 5-GHz 20-dBm Power Amplifier with Digitally Assisted AM-PM Correction in a 90-nm CMOS Process,” *IEEE JSSC*, vol. 41, no. 8, pp. 1757-1763, Aug. 2006.

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[4] S. N. Ali et al., “Reconfigurable High Efficiency Power Amplifier with Tunable Coupling Coefficient Based Transformer for 5G Applications,” *IEEE IMS*, pp. 1177-1180, June 2017.

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[6] S. Shakib et al., “A Highly Efficient and Linear Power Amplifier for 28-GHz 5G Phased Array Radios in 28-nm CMOS,” *IEEE JSSC*, vol. 51, no. 12, pp. 3020-3036, Dec. 2016.

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[9] M. Vigilante and P. Reynaert, “A 29-to-57GHz AM-PM compensated class-AB power amplifier for 5G phased arrays in 0.9V 28nm bulk CMOS,” *IEEE RFIC*, pp. 116-119, June 2017.

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  - Keysight Technologies

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A Compact Dual-Band Digital Doherty Power Amplifier Using Parallel-Combining Transformer for Cellular NB-IoT Applications

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Hao Min, Hongtao Xu

Fudan University, Shanghai, China

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Outline

- Background
- Digital Doherty Operation
- Circuit Implementation
- Measurement Results
- Conclusions

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NB-IoT Capabilities

Easy Deployment

3GPP A GLOBAL INITIATIVE

Cellular system

Better Coverage

+20dB vs GSM

Low Power Consumption

10+ years battery life

Low Cost

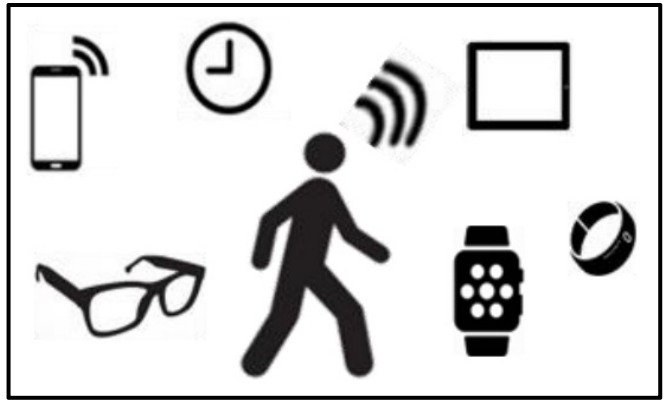
Just a few $

Massive Connections

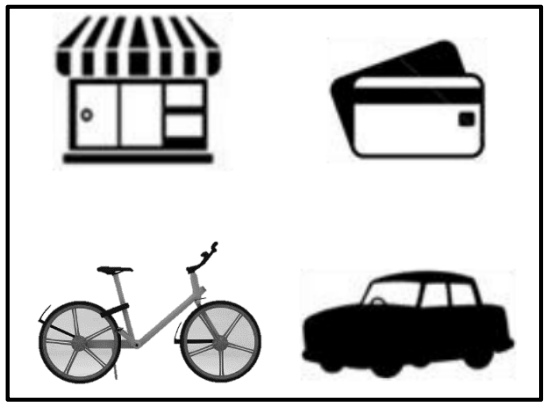
>50k per cell

NB-IoT for Low-Power Wide-Area Use Cases

Smart Home



Smart Personal



Smart Public

Smart Industry

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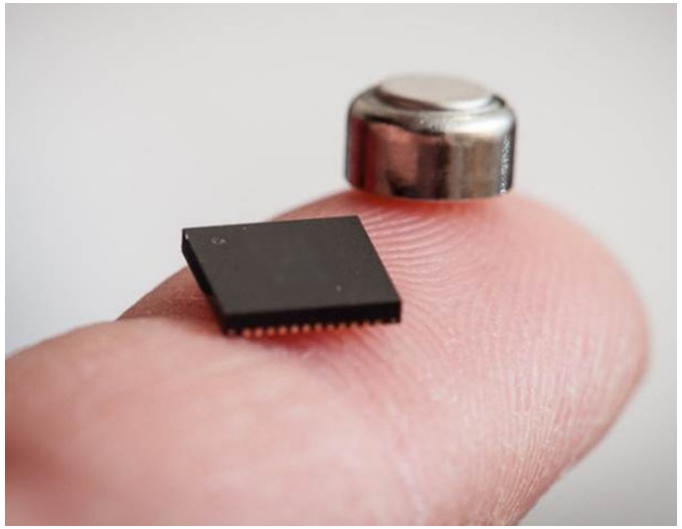
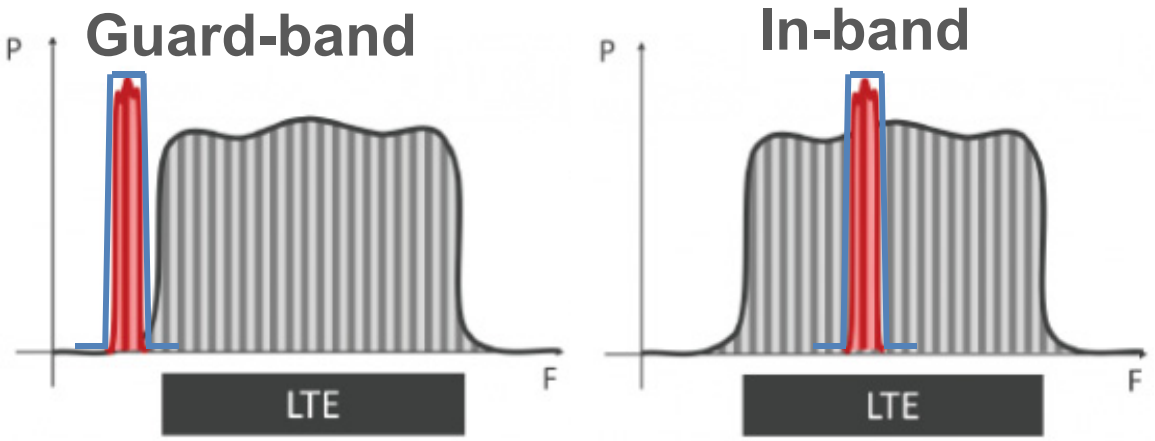
Challenges

- Low cost
- Low power consumption
- Small form factor
- Fast time to market
- Low voltage operation



VS

- LB/HB dual-band operation
  (699-915MHz & 1710-1980MHz)
- Max. 23dBm average Pout
- 12-subcarrier with high PAPR
- Low out-of-band emission



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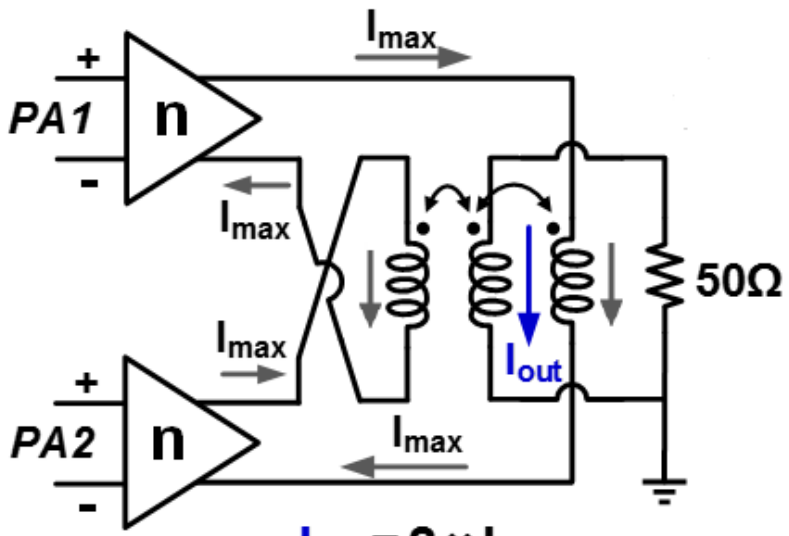
Digital Doherty Operation (1)

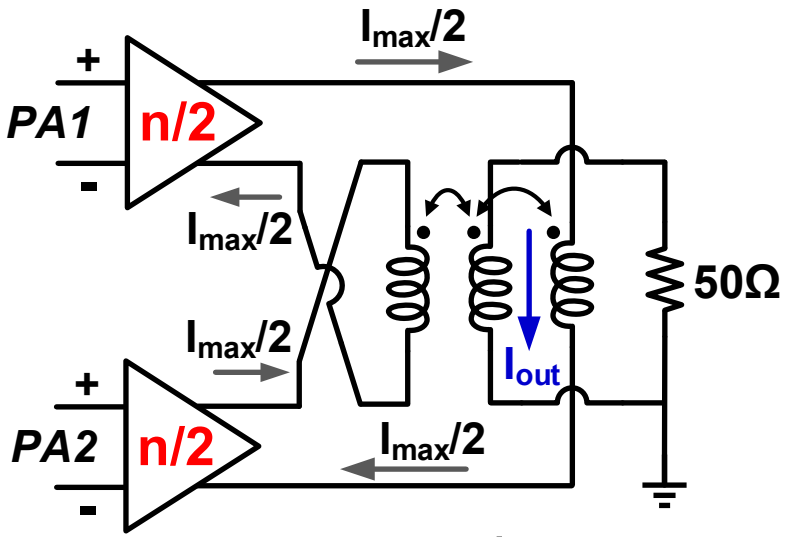
Peak Power



$I_{out} = 2 \times I_{max}$

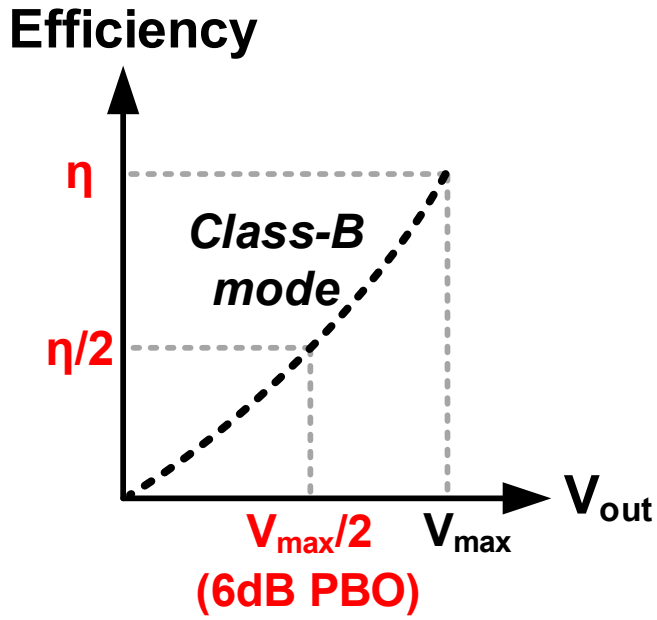
$R_{L_PA1} = R_{L_PA2} = 50\Omega$

6dB PBO Class-B Mode



$I_{out} = 2 \times I_{max}/2 = I_{max}$

$R_{L_PA1} = R_{L_PA2} = 50\Omega$



- 3-coil current-mode combiner
- Quasi-differential PA pairs

- Class-B mode: 50% efficiency degradation @6dB PBO

*R_{L_PA}: The single-ended impedance seen by each PA.

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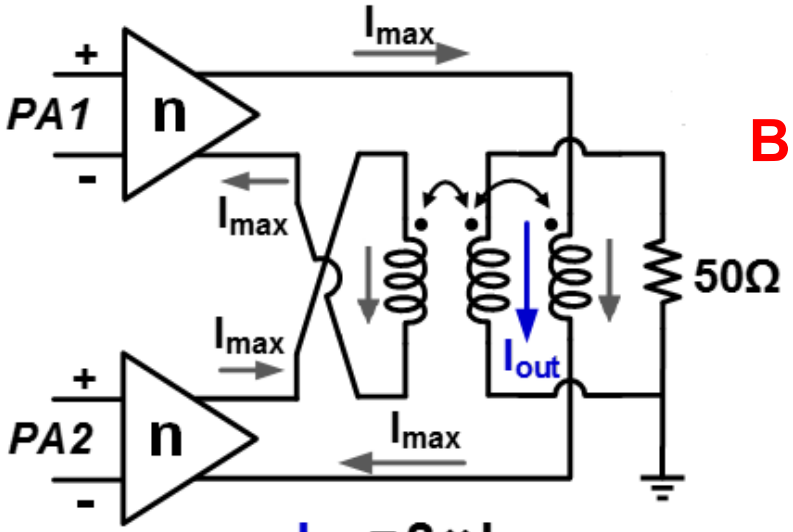
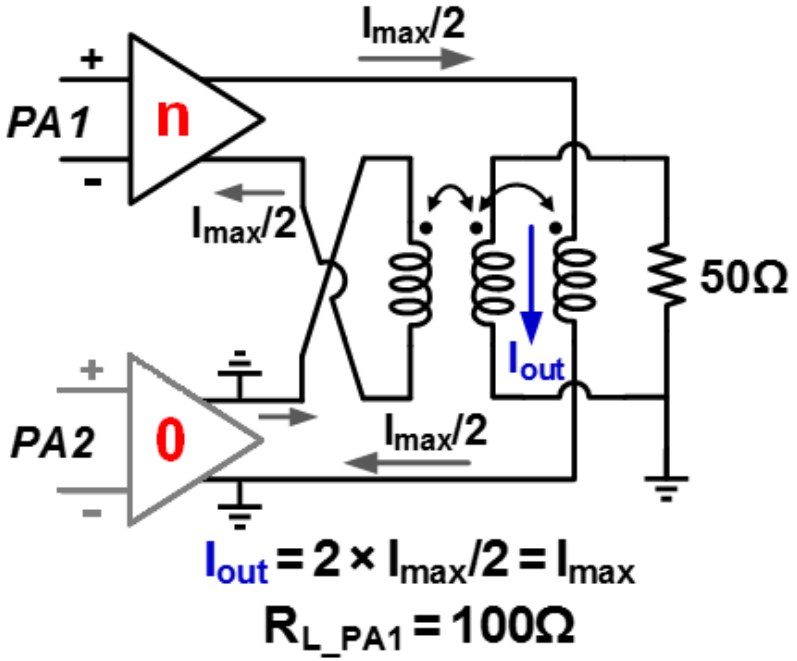
Digital Doherty Operation (2)

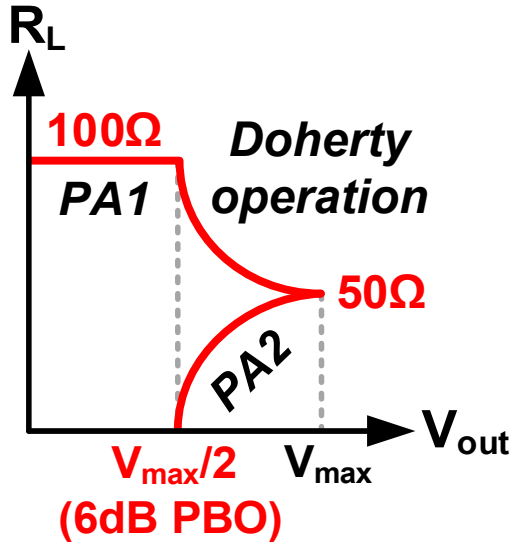
Peak Power

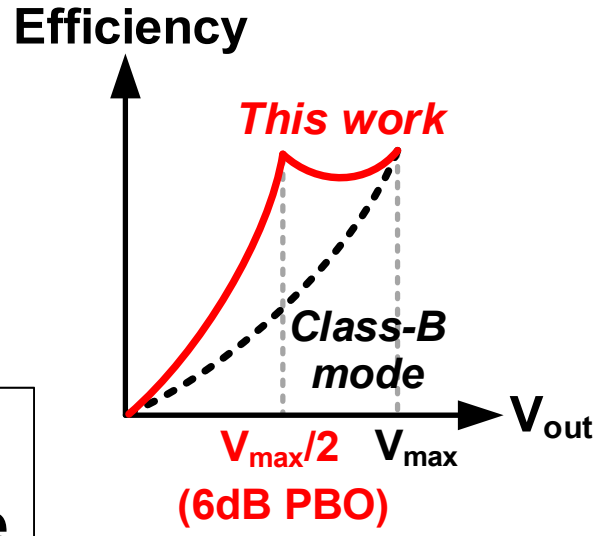


Backoff η Boost

6dB PBO This work







- Digital Doherty: digital PA + parallel transformer combiner
- Dual-band coverage + backoff η boost + ultra-compact size

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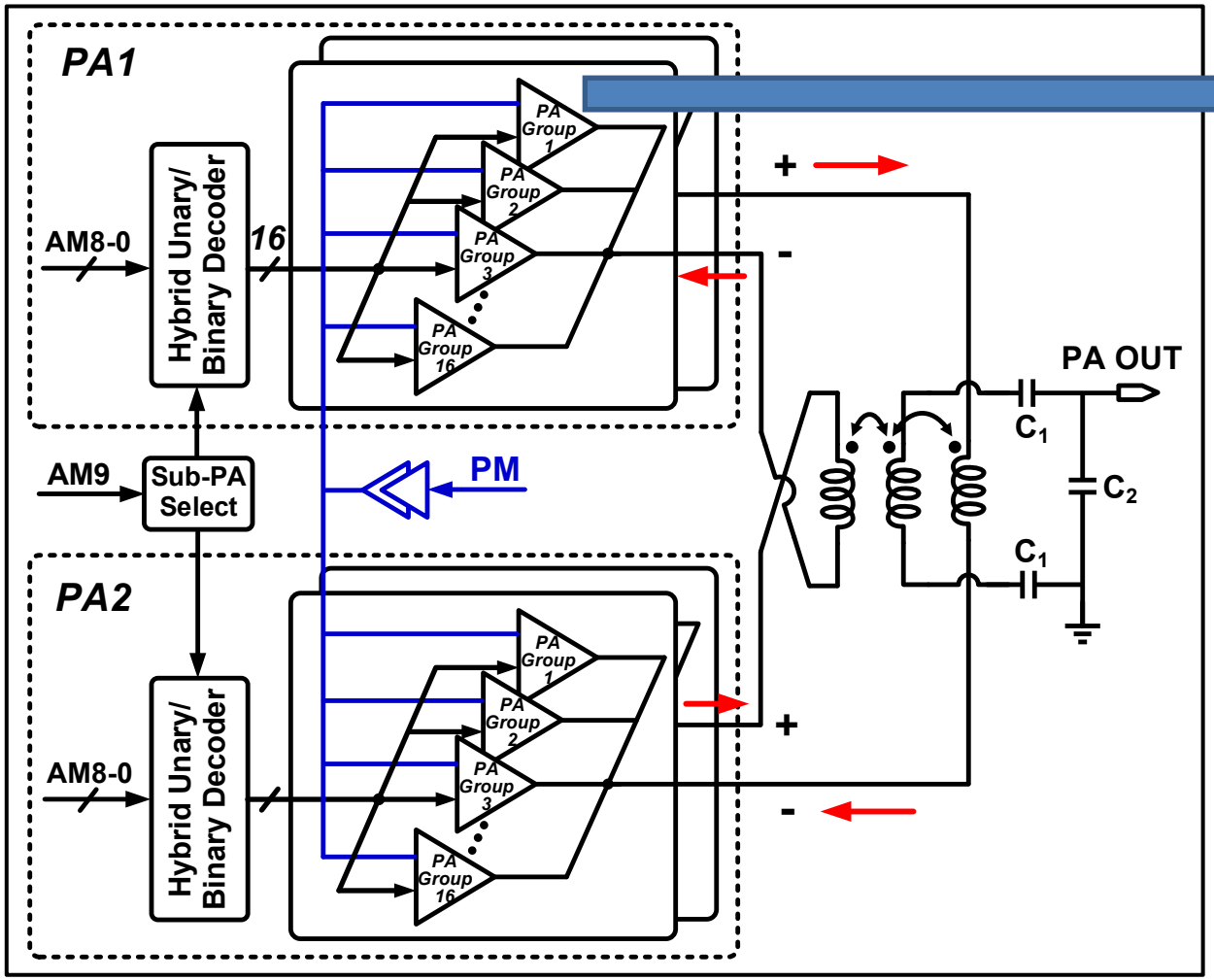
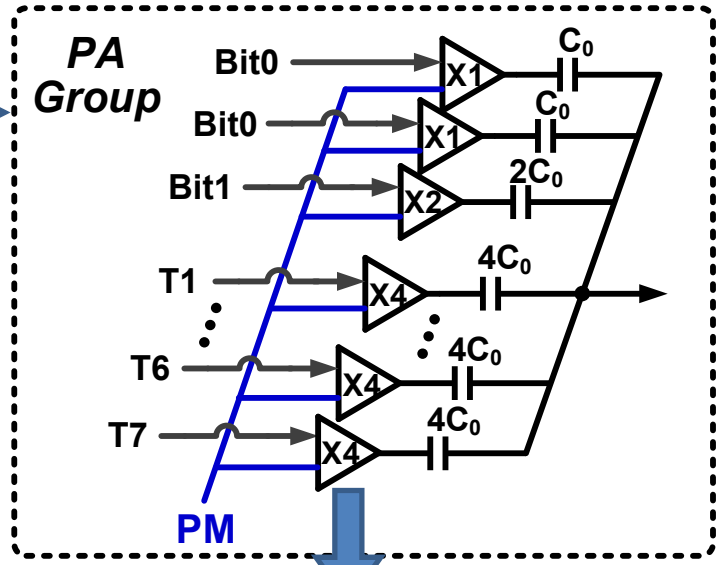
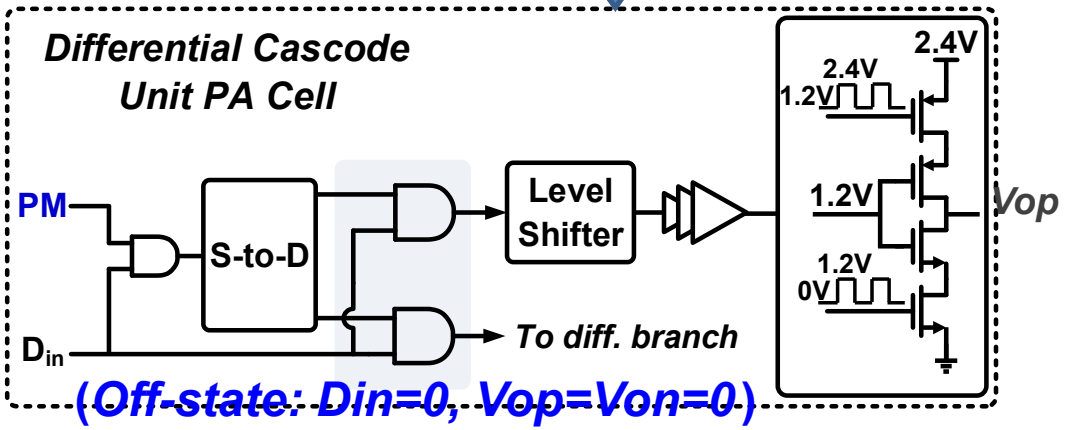
Block Diagram







- 10-bit resolution: two 9-bit sub-PAs with hybrid unary/binary arrays
  - Sub-PA: 16 PA groups (4 MSBs), each group has 7 thermo + 2-bit binary-code cells
- Cascode inverter Class-D topology to obtain high output power

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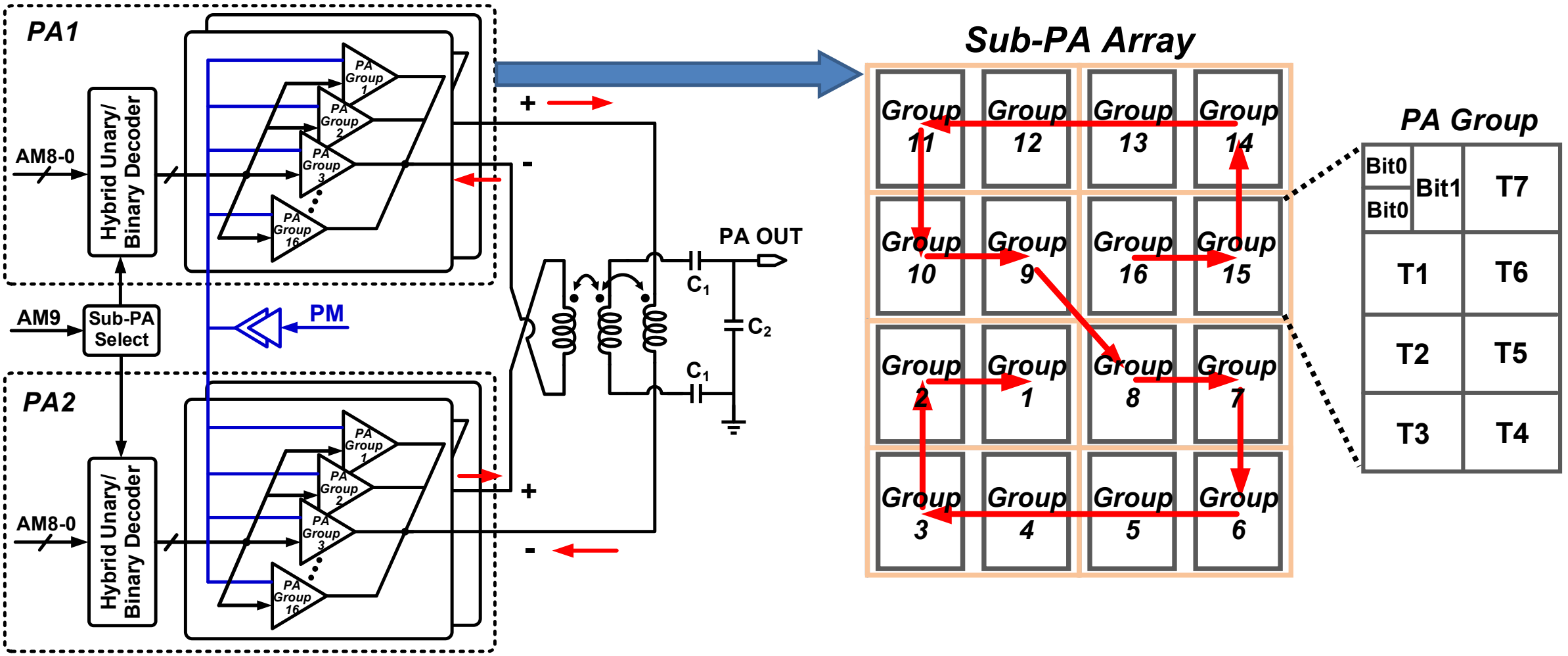
PA Array Floorplan



- PA group arrangement with “snake” traverse movement to improve DNL
- Minimize layout mismatch and achieve better resolution

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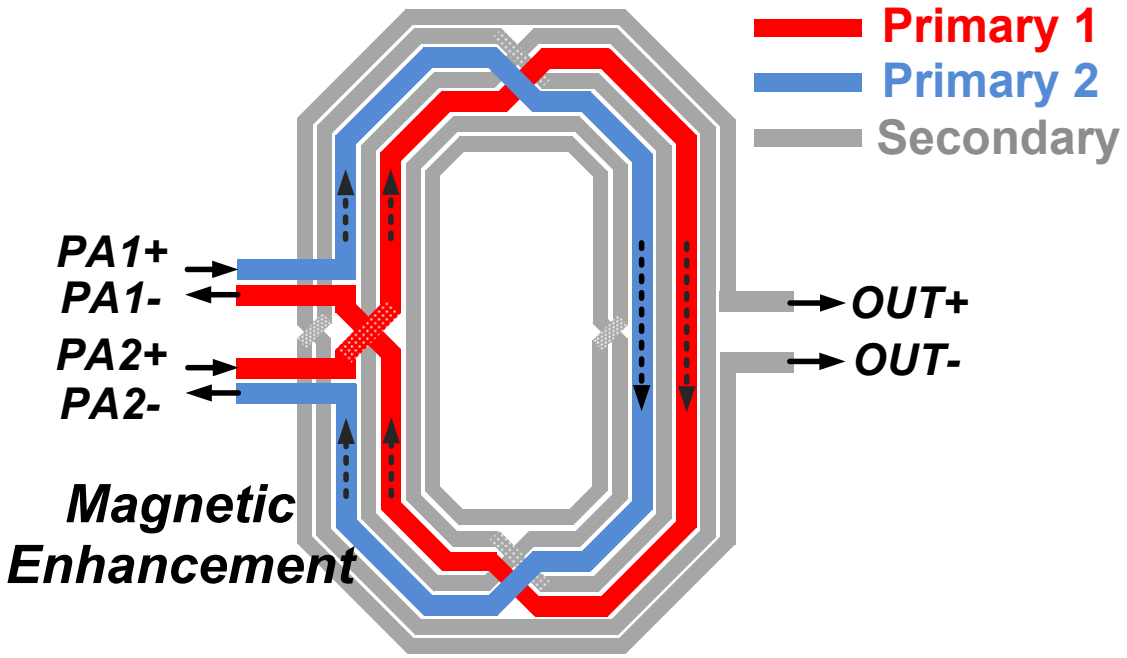
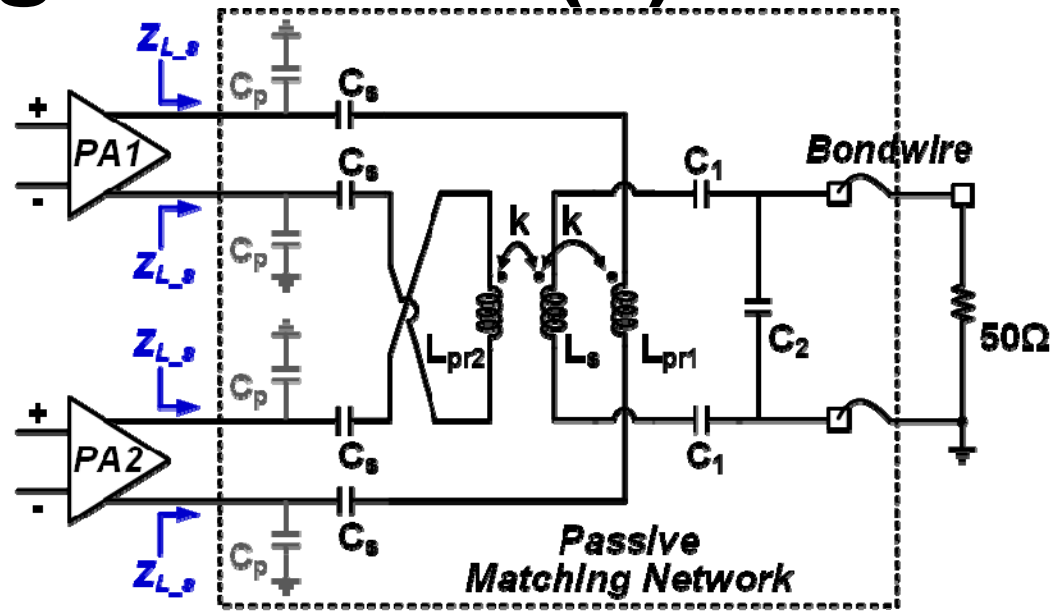
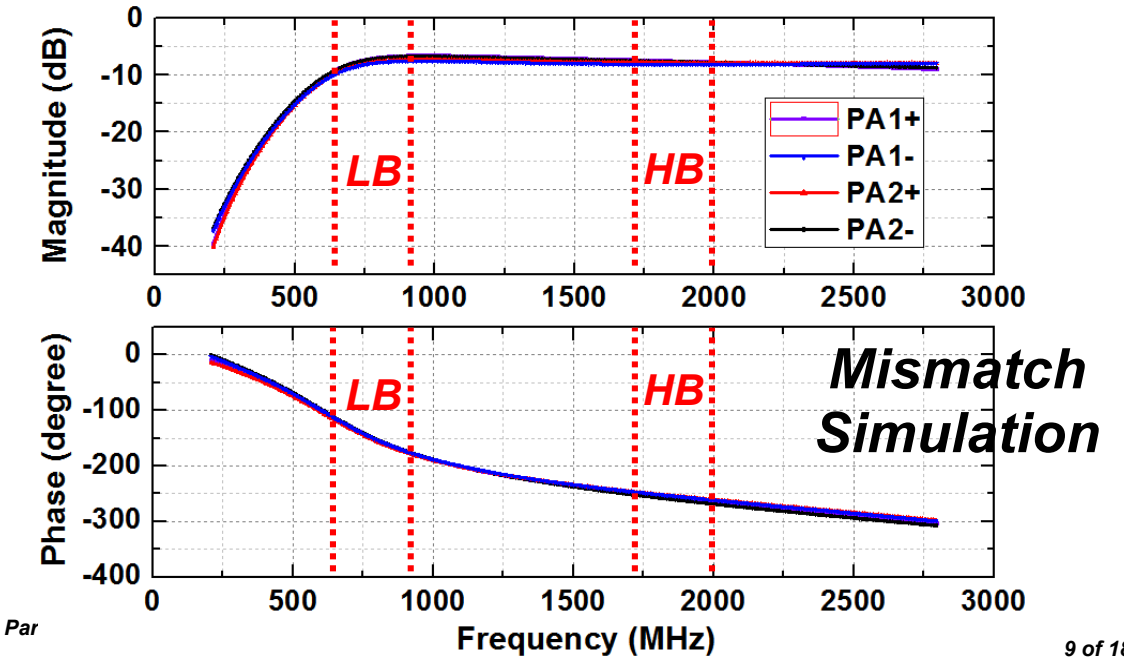
Dual-Band Matching Network (1)





- A compact single-transformer footprint
- Good differential symmetry
- Magnetic enhancement and increase Lpr
- Size reduction and lower loss
- 340um*500um, esp. Sub-GHz design



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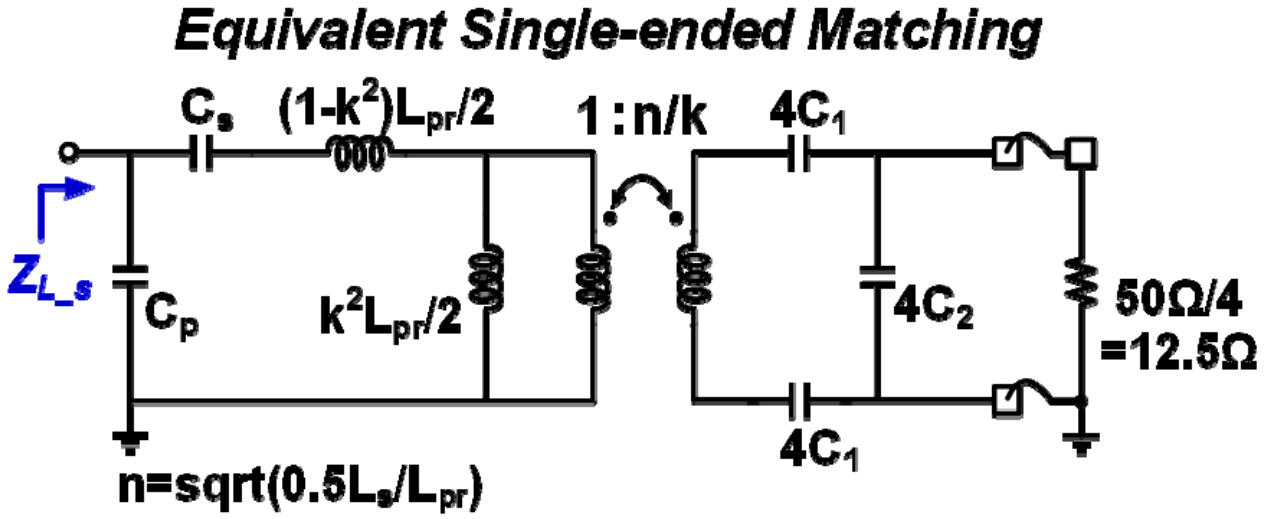
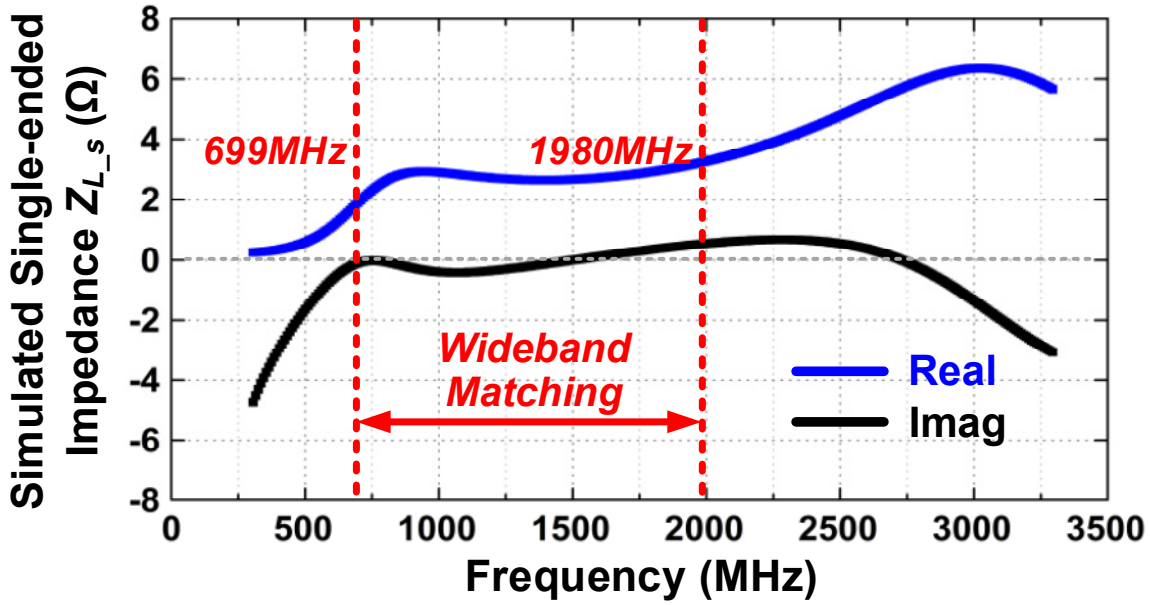
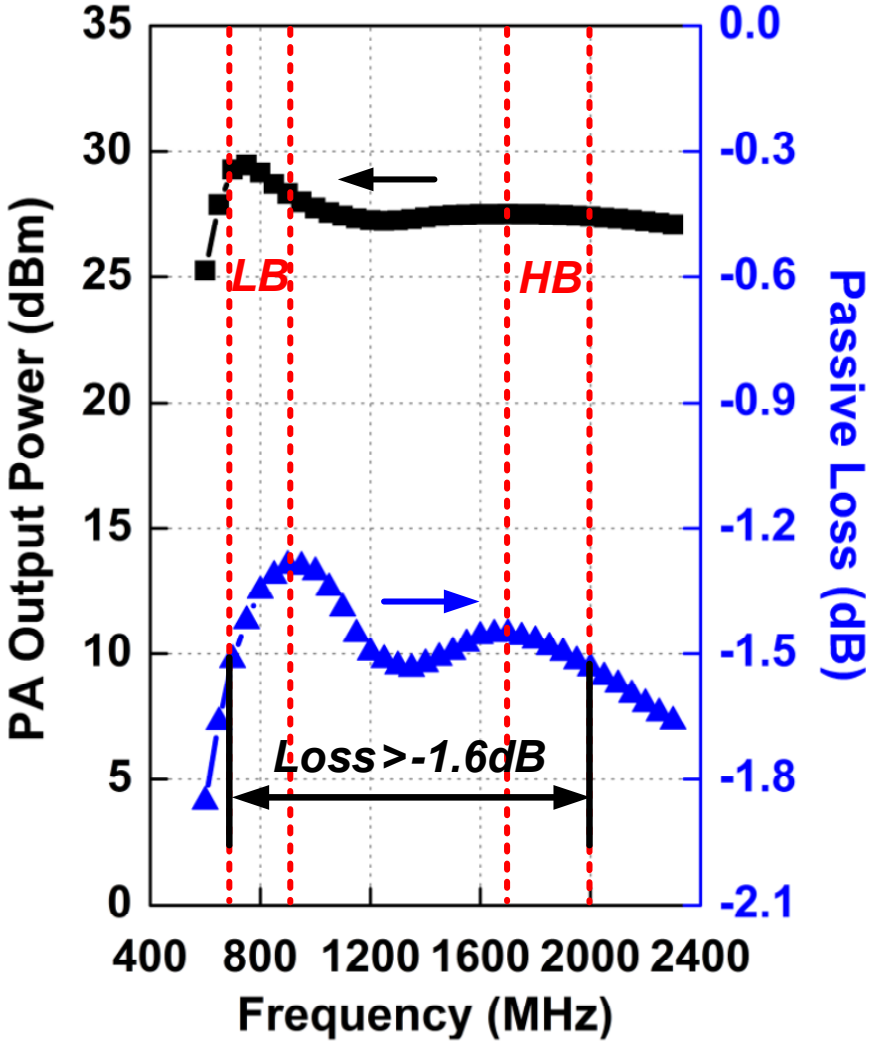
Dual-Band Matching Network (2)





Simulated PA Pout and Passive Loss



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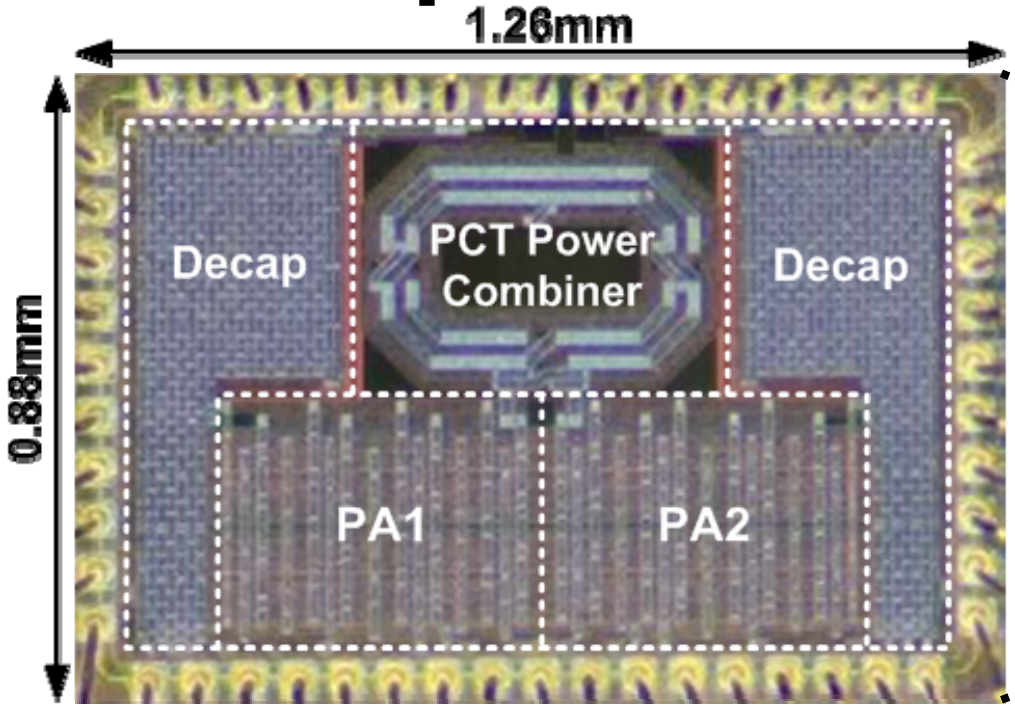
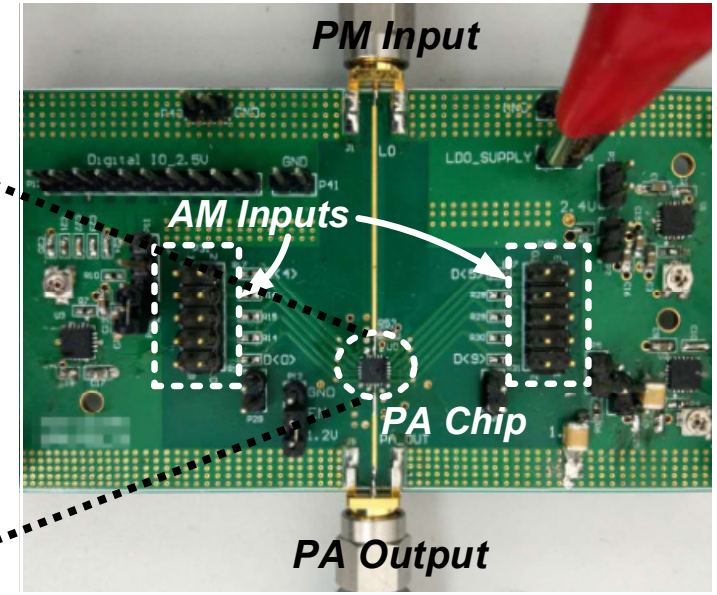
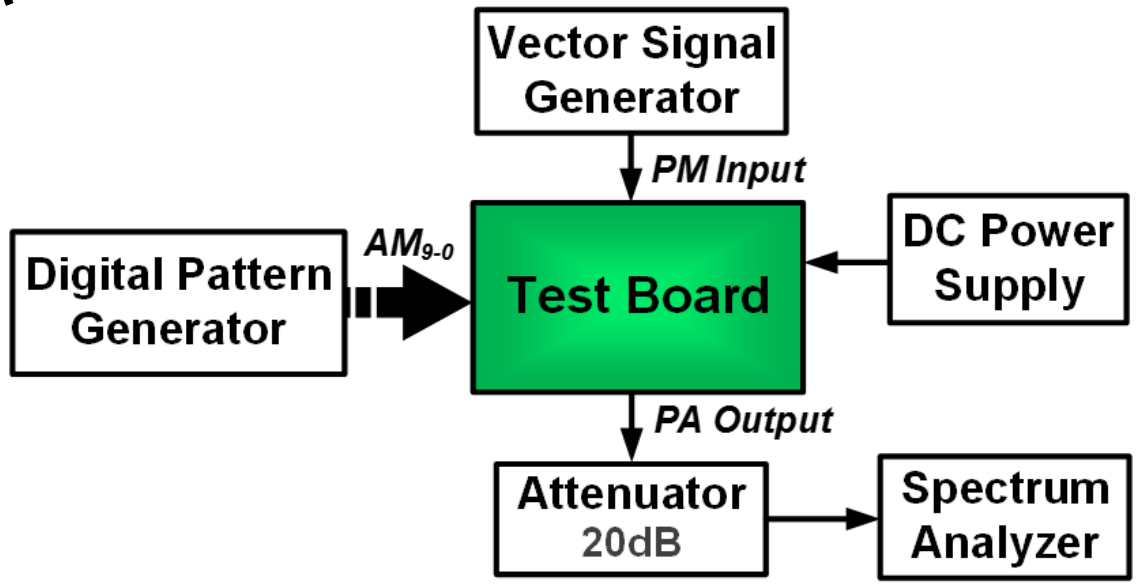
Chip Photo & Measurement Setup





- 55nm CMOS
- Chip area: 1.1mm^2 (including ESD I/O pads and 1.2nF decap)
- QFN package
- Dual power supplies: 2.4V & 1.2V
- PAE = Pout / Pdc(all blocks)



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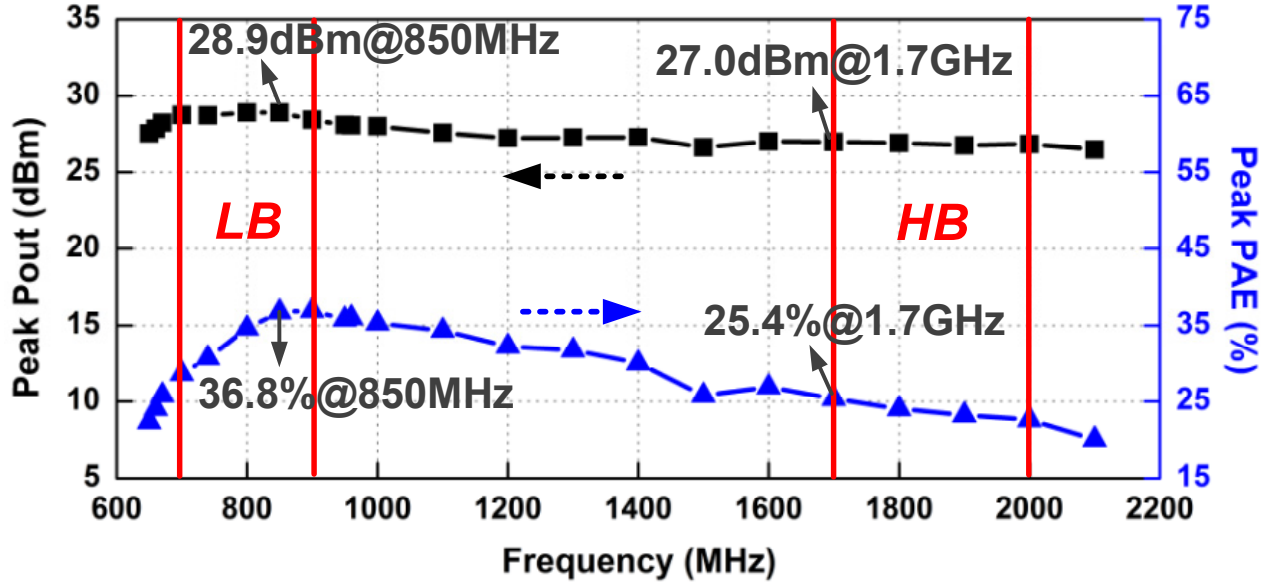
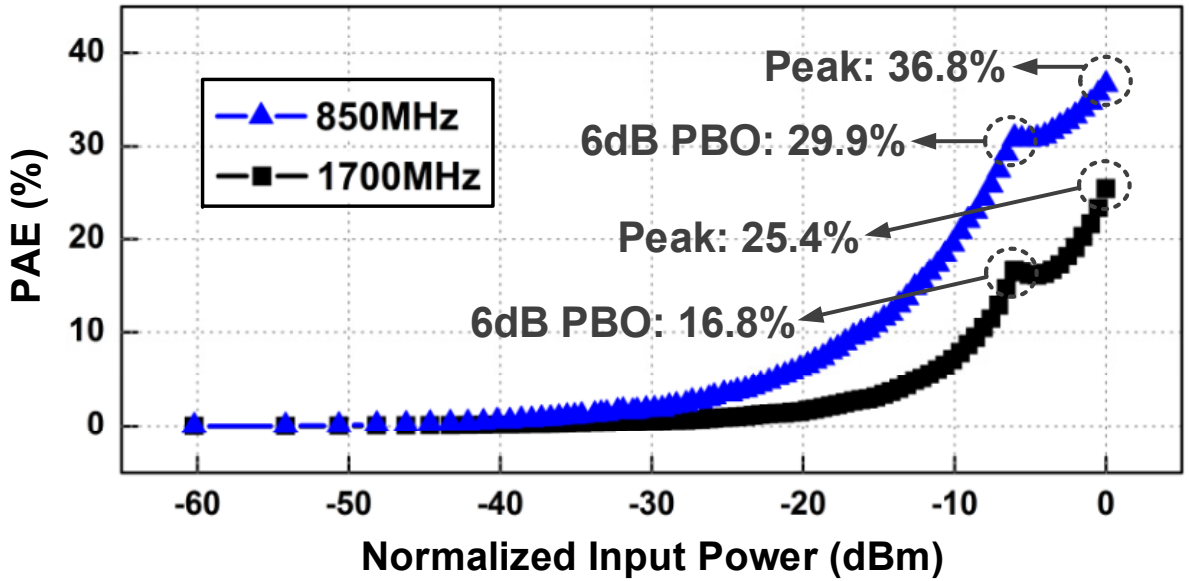
Measured CW Performance





- **LB**
  - 28.9dBm peak Pout
  - 36.8% peak PAE
  - 0.3dB power deviation
- **HB**
  - 27.0dBm peak Pout
  - 25.4% peak PAE
  - 0.2dB power deviation
- **Doherty Load**
  - LB: 29.9% PAE @6dB PBO
  - HB: 16.8% PAE @6dB PBO

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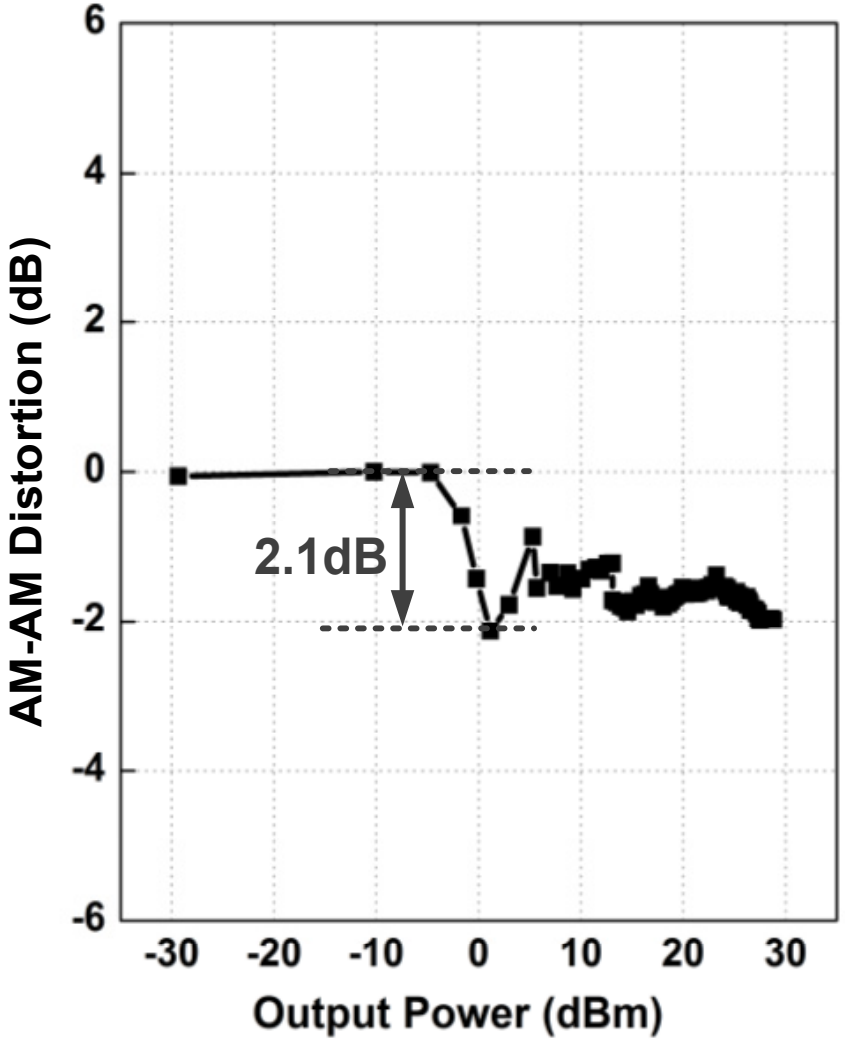
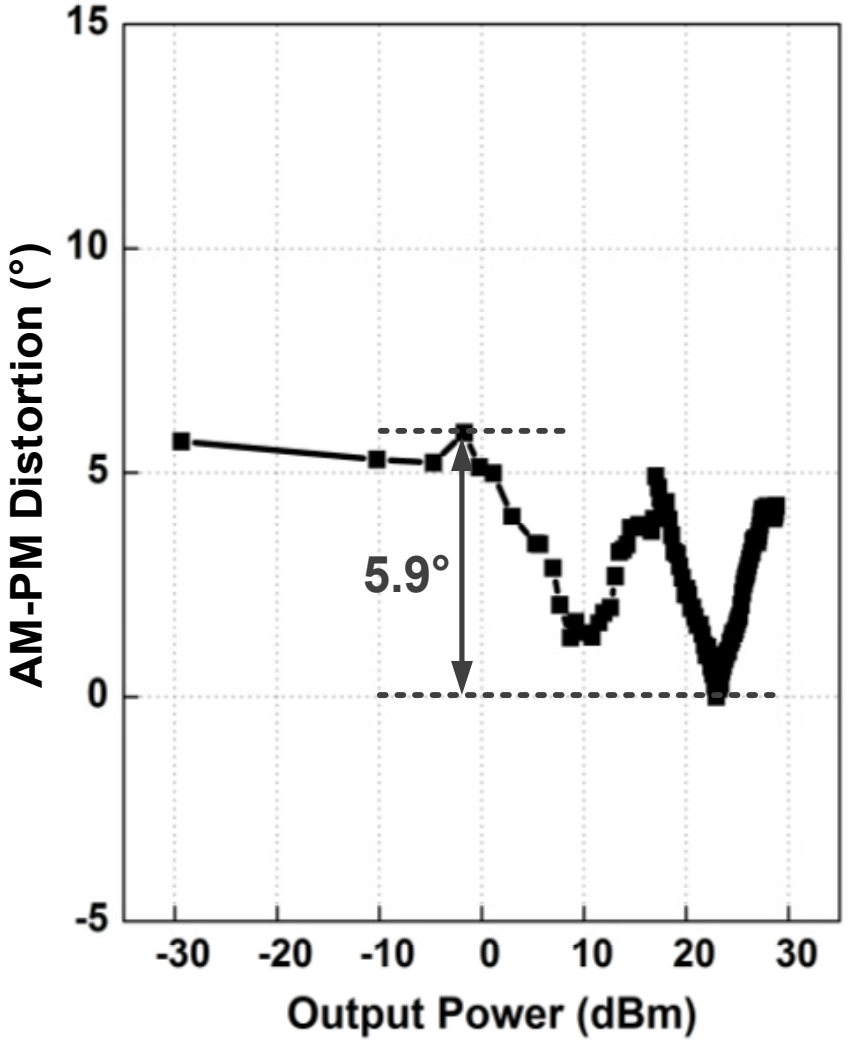
Measured AM-AM/AM-PM Nonlinearity





- **AM-AM distortion: 2.1dB**
- **AM-PM distortion: 5.9°**

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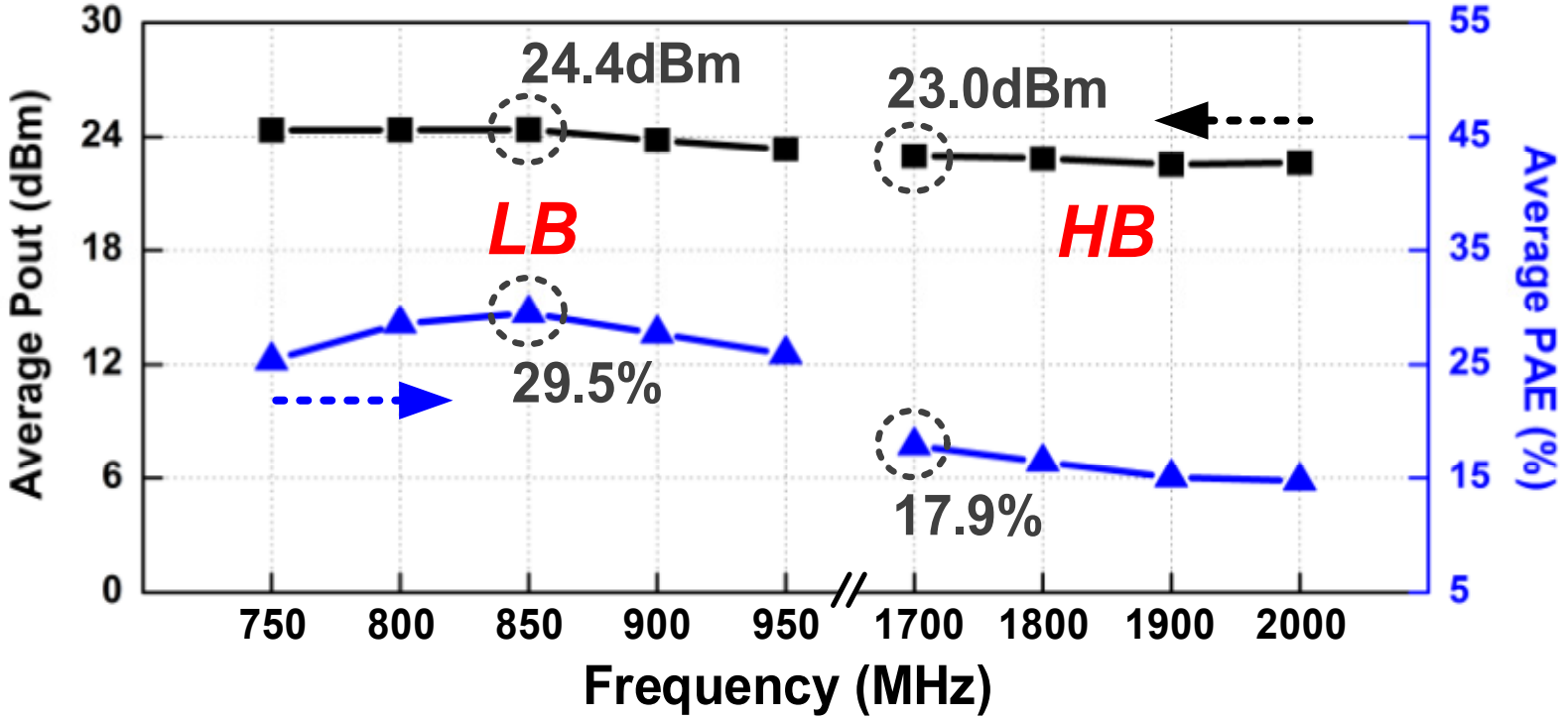
Measured NB-IoT Modulation (1)

- Memoryless DPD look-up tables for linearization
- 12-subcarrier 180kHz QPSK NB-IoT signal:
  - EVM=-21.6dB, $PAPR_{clipping}$=4.5dB
  - LB @850MHz: 24.4dBm average Pout, 29.5% average PAE
  - HB @1.7GHz: 23.0dBm average Pout, 17.9% average PAE



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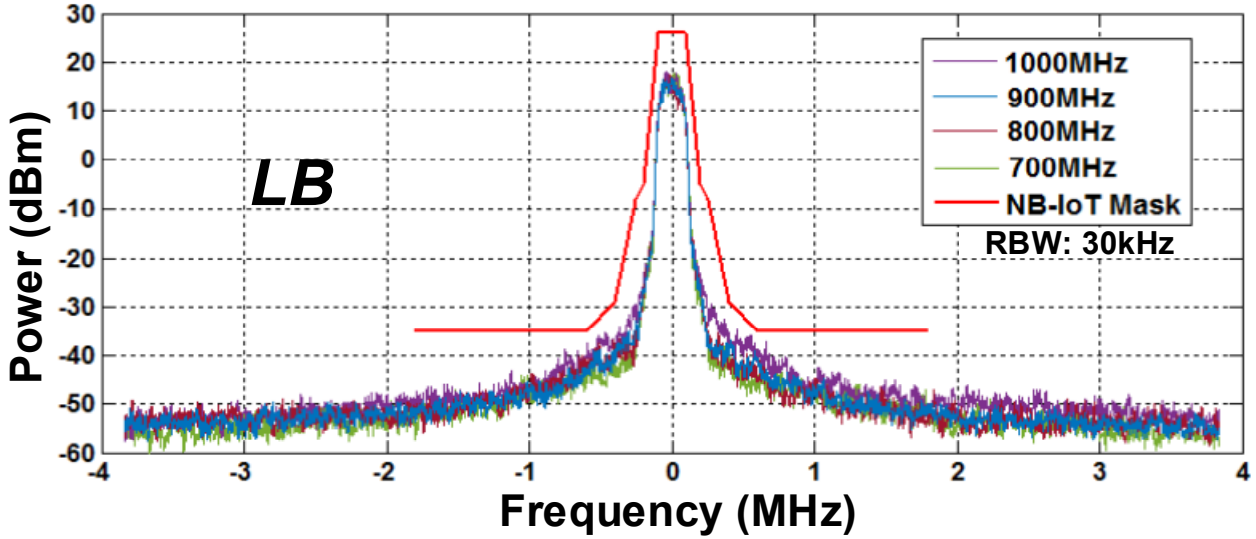
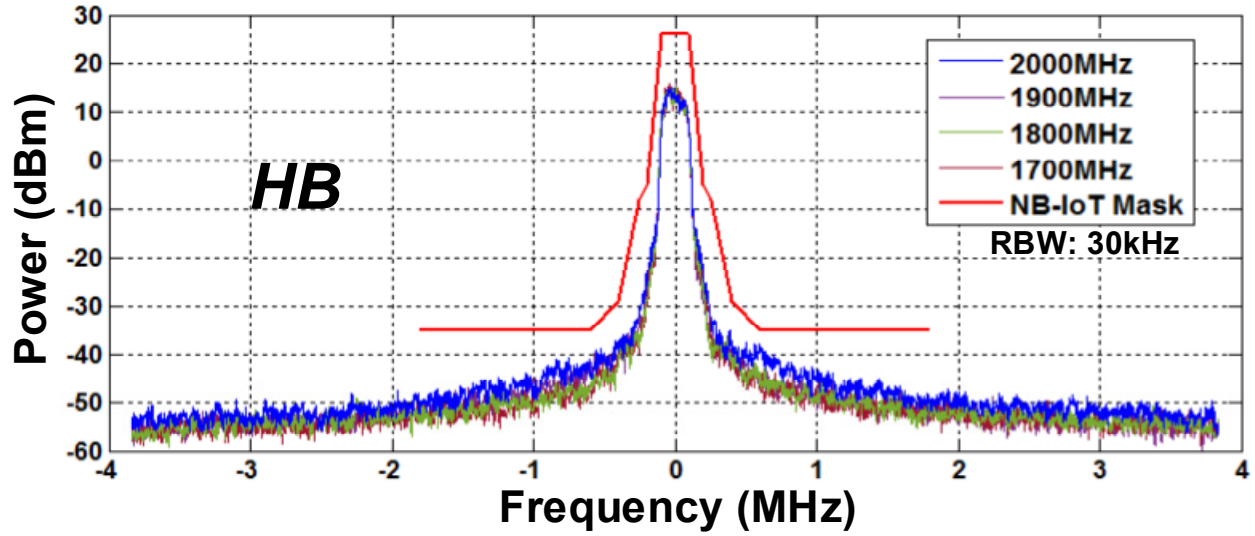
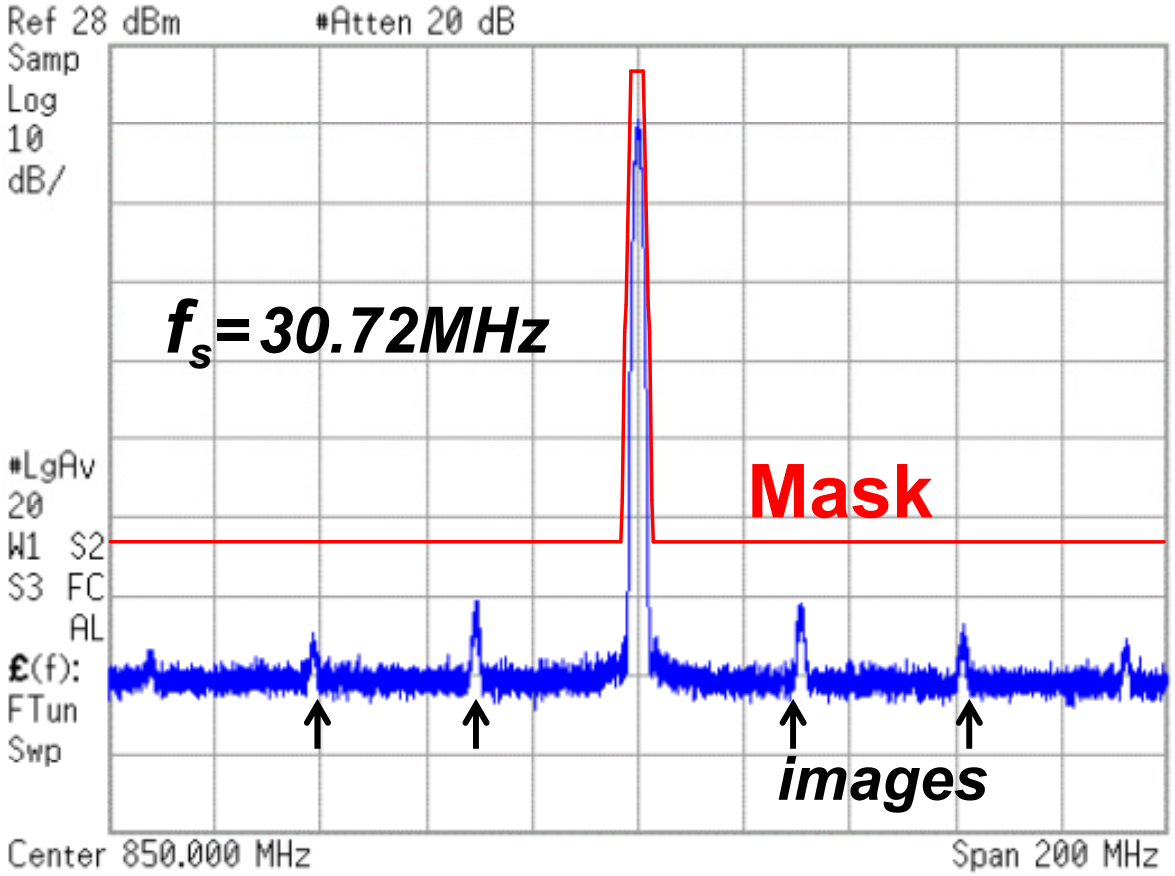
Measured NB-IoT Modulation (2)

- **PA close-in spectrum:**





- **PA far-out spectrum:**



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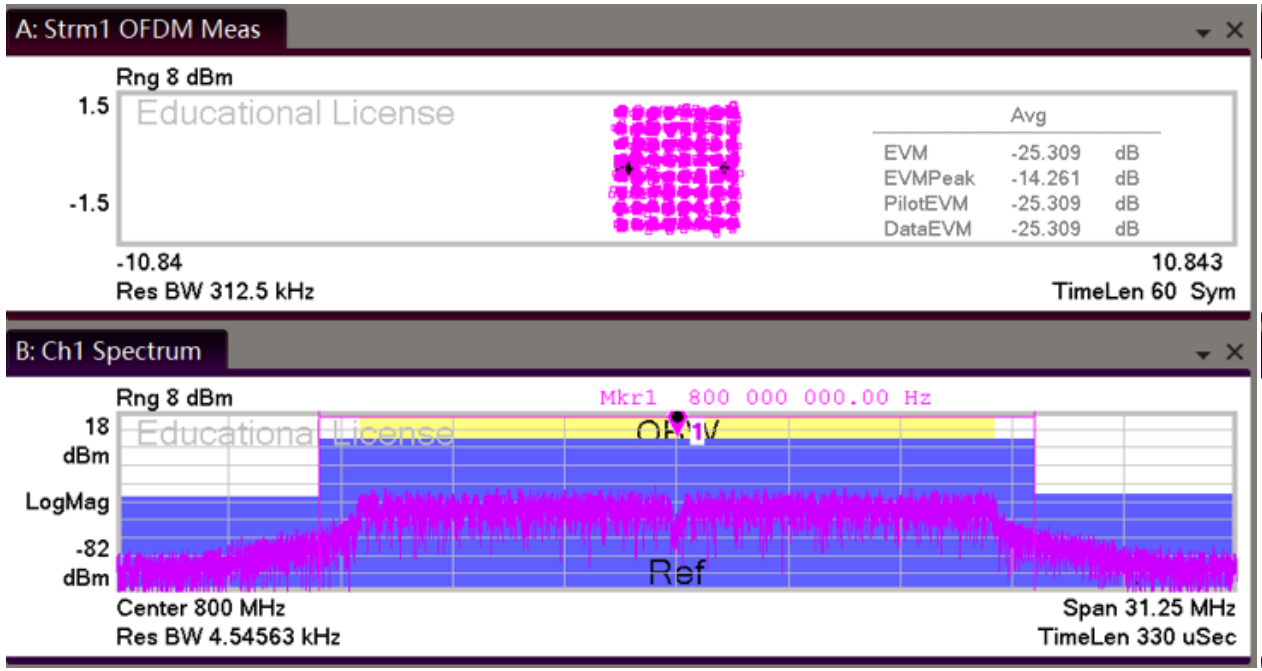
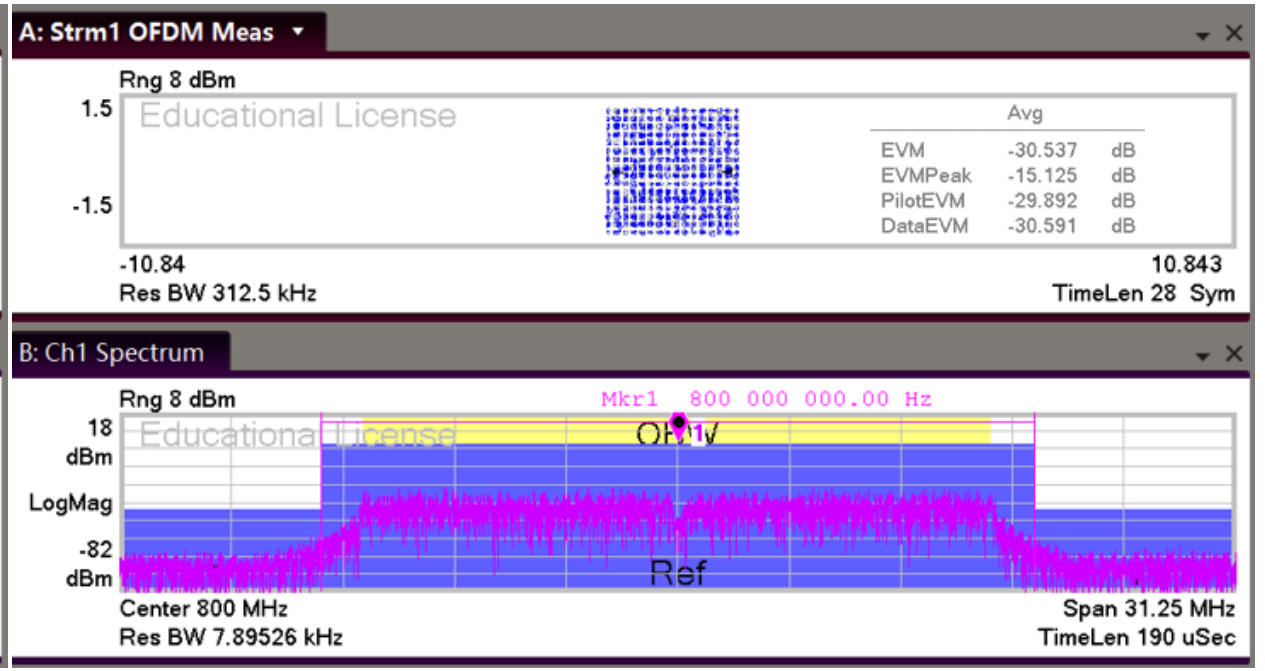
Measured Wideband Modulation





20MHz 64QAM WLAN:

- Pout=22.9dBm
- PAE=26.1%
- EVM=-25.3dB

20MHz 256QAM WLAN:

- Pout=20.8dBm
- PAE=22.7%
- EVM=-30.5dB

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Comparison with Prior Works

	This work		Z. Song† TCAS-I'17	J. Moreira ISSCC'15	J. Park* JSSC'16	S. Hu* JSSC'15	V. Vorapipat* ISSCC'17
Freq. (GHz)	**0.85/1.7**		0.891	0.95/1.95	2.6/4.5	3.82	3.5
On-chip Balun	**Yes (1 TF)**		No (Off-chip MN)	Yes (2 TF)	Yes (1 TF)	Yes (2 TF)	Yes (2 TF)
Peak Pout (dBm)	**28.9/27.0**		23.2	32	28.1/26.0	27.3	25.3
Peak PAE (%)	**36.8/25.4**		44.5	-	35/21.2	32.5 (DE)	30.4
6dB PBO PAE (%)	**29.9/16.8**		-	-	-	22 (DE)	25.3
Modulation	**180kHz NB-IoT**	**20MHz 64/256 QAM WLAN@LB**	3.75kHz NB-IoT	HSPA	8MS/s 256QAM	500kS/s 16QAM	10MHz 256QAM
Pavg (dBm)	**24.4/23.0**	**22.9/20.8**	18.87	>26/>26	20.37/18.53	21.8	19.0
PAE (%)	**29.5/17.9**	**26.1/22.7**	33.4	23.7/23.8	16.26/13.42	22.1 (DE)	24.0
EVM (dB)	**-21.6**	**-25.3/-30.5**	-28.2	-26.6/-23.2	-36.3/-34.6	-25.0	-35.0
Area (mm^2)	**1.11**		1.75	3	2.25	2.09	1.2
Technology	**55nm**		180nm	65nm	65nm	65nm	45nm SOI

† Results from the second prototype. * Results measured with GSG probe.

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Conclusions

- A new digital Doherty PA architecture is presented.
- A PCT power combiner is introduced for dual-band coverage, high output power, back-off efficiency enhancement and ultra-compact implementation.
- The PA achieves:
  - 28.9dBm peak Pout, 36.8% peak PAE, 29.9% PAE @6dB PBO
  - Best average PAE with on-chip matching and smallest footprint at sub-GHz
  - Well-fitting low-cost NB-IoT applications!

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A Continuous-Mode Harmonically Tuned 19-to-29.5GHz Ultra-Linear PA Supporting 18Gb/s at 18.4% Modulation PAE and 43.5% Peak PAE

Tso-Wei Li, Min-Yu Huang, and Hua Wang
Georgia Tech Electronics and Micro-System Lab (GEMS)
Georgia Institute of Technology, USA

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Outline

- Introduction
- Harmonically tuned continuous-mode PA output network
- PA schematic and implementation
- Measurement results
- Conclusion

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Outline

- **Introduction**
- Harmonically tuned continuous-mode PA output network
- PA schematic and implementation
- Measurement results
- Conclusion

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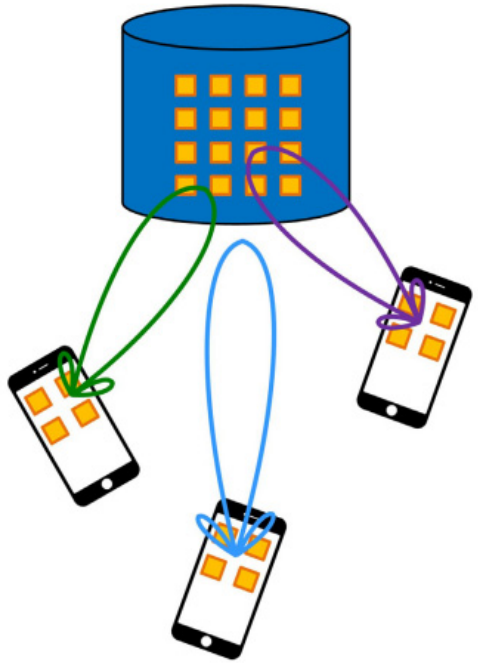
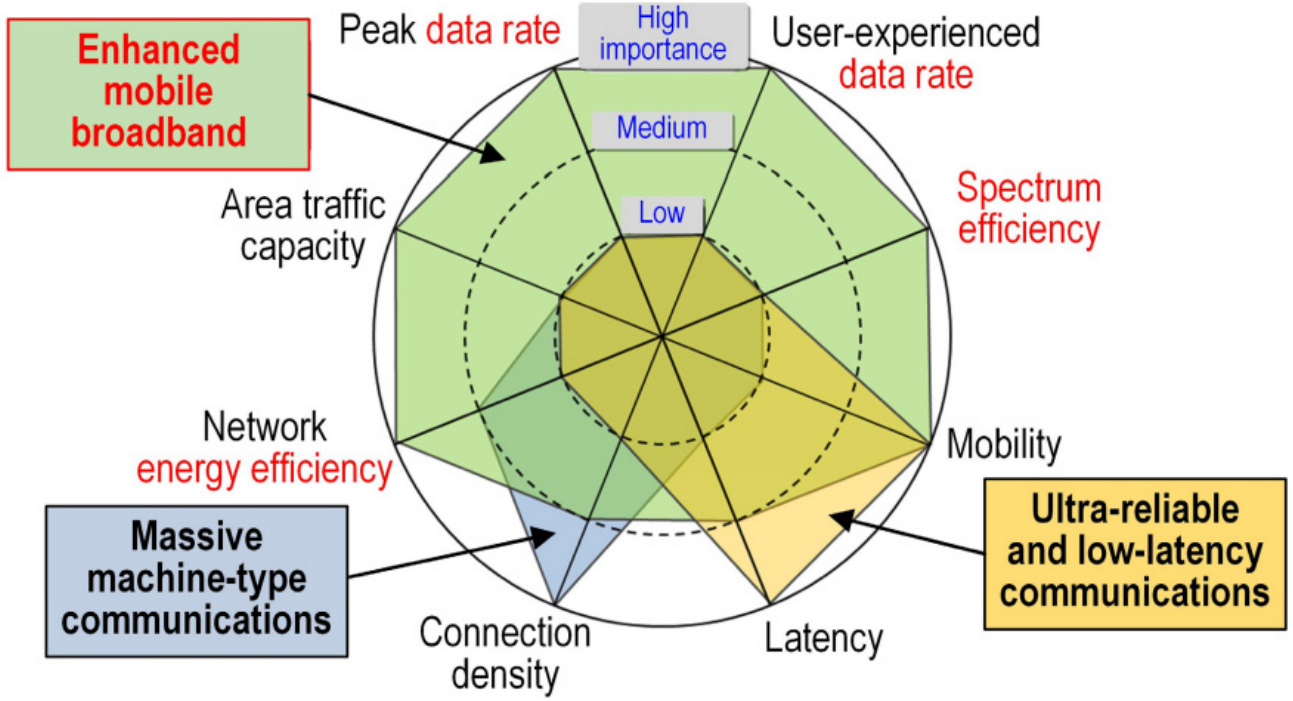
Introduction

- **The 5G mm-Wave systems support wideband spectrum-efficient modulations (e.g., 64-QAM or 256-QAM)**
  → Achieve Gb/s-link-throughput revolution





[ITU IM-2020 vision]

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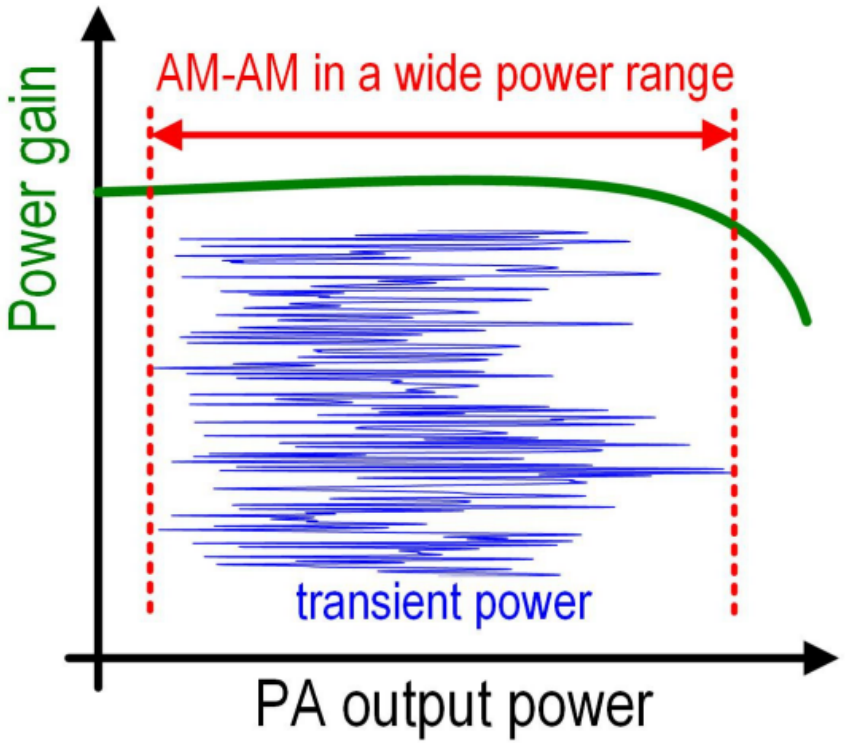
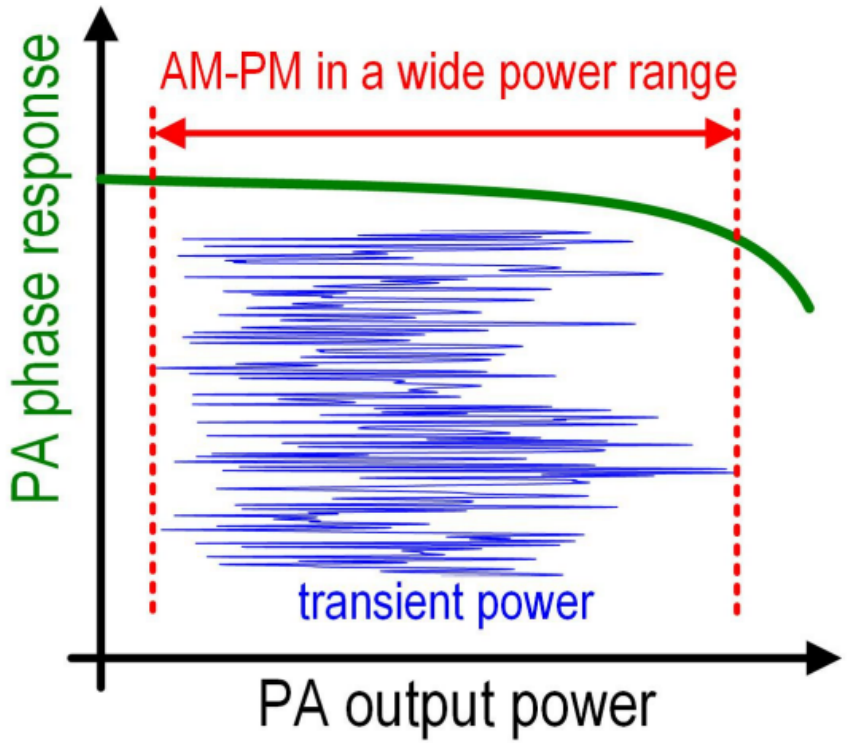
Introduction

- **Complex modulation schemes come with high-density constellations**
  → Demand stringent linearity, i.e. AM-AM and AM-PM.





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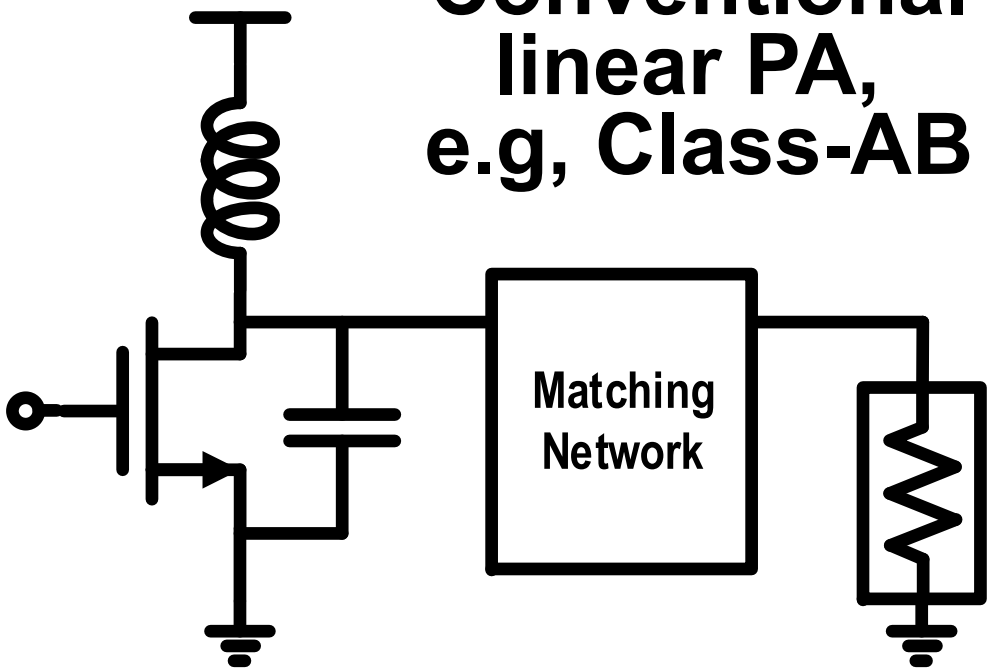
Introduction

- Practical mm-Wave PAs face a steep trade-off between the PA efficiency and linearity

Conventional linear PA, e.g, Class-AB



- Simple design
- Good linearity
- The over-simplified output network

→ efficiency is limited

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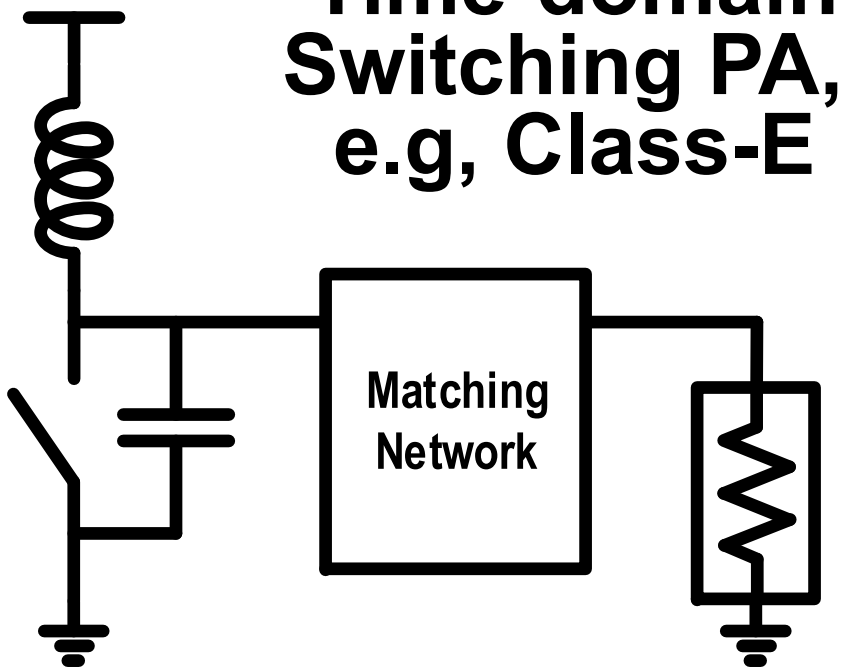
Introduction

- Practical mm-Wave PAs face a steep trade-off between the PA efficiency and linearity

Time-domain Switching PA, e.g, Class-E



- High efficiency
- Poor linearity
  → cannot support complex modulations without DPD
- DPD
  → substantial power and complexity

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Introduction

- Practical mm-Wave PAs face a steep trade-off between the PA efficiency and linearity
  - Overdriven linear PAs with harmonic terminations
  - Class-J, Class-F-like or Class-F^{-1}-like harmonic terminations
    → Boost efficiency
    → Preserve linearity

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Motivation

- The conventional overdriven linear PAs with harmonic terminations →good linearity and high efficiency
  - Area-consuming passive networks
  - Narrowband harmonic terminations

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Motivation

- **We propose a continuous-mode harmonically tuned mm-Wave PA**
  - **High efficiency**
  - **High linearity**
  - **Wideband operation**
  - **Compact size**

Good for broadband 5G massive MIMOs

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Outline

- Introduction
- **Harmonically tuned continuous-mode PA output network**
- PA schematic and implementation
- Measurement results
- Conclusion

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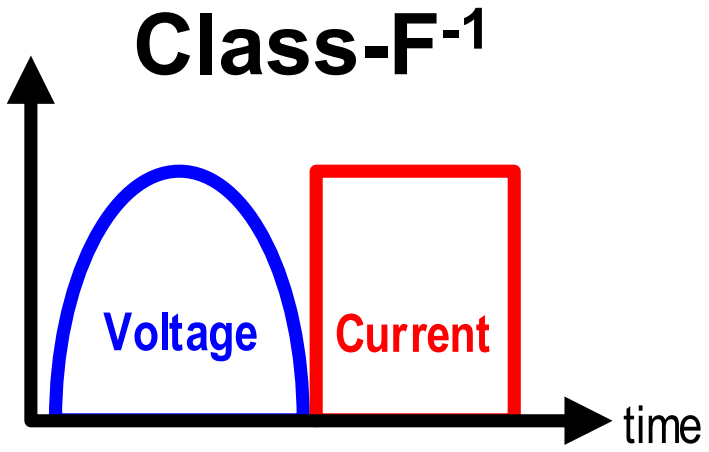
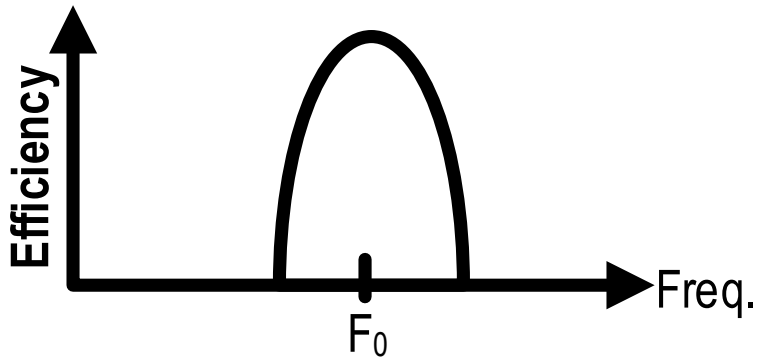
Continuous-Mode Operation

- Conventional vs. continuous-mode design



Non-overlap V-I →high efficiency
# of harmonic tuning↑ → efficiency ↑



- Needs precise load impedance at 2nd and 3rd harmonics
  - →High efficiency
  - →Narrow-band

Harmonic	ω_0	$2\omega_0$	$3\omega_0$
Impedance	R_{opt}	Open	Short

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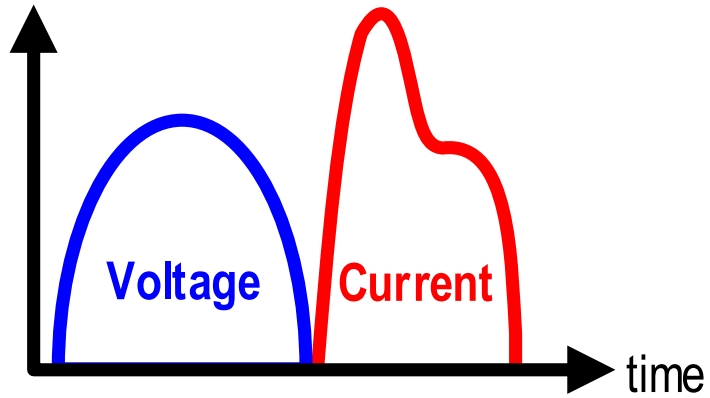
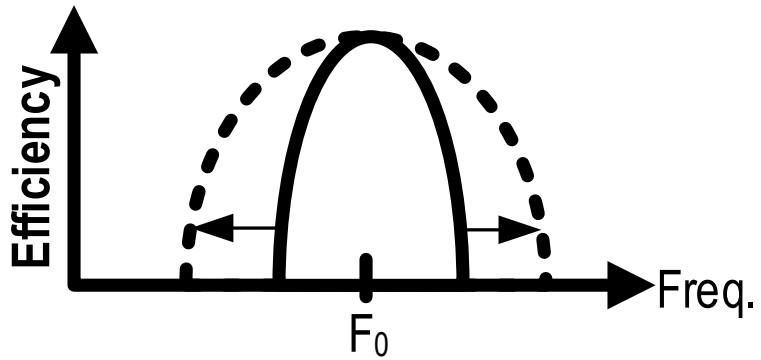
Continuous-Mode Operation

- **Conventional vs. continuous-mode design**

Continuous-mode Class-F^{-1} **[V. Carrubba et al., EuMC 2011]**



Non-overlap V-I →high efficiency



- **Additional design space for fund. and 2nd harmonic load impedance**
  →Wider bandwidth

- **Maintain high efficiency and output power**

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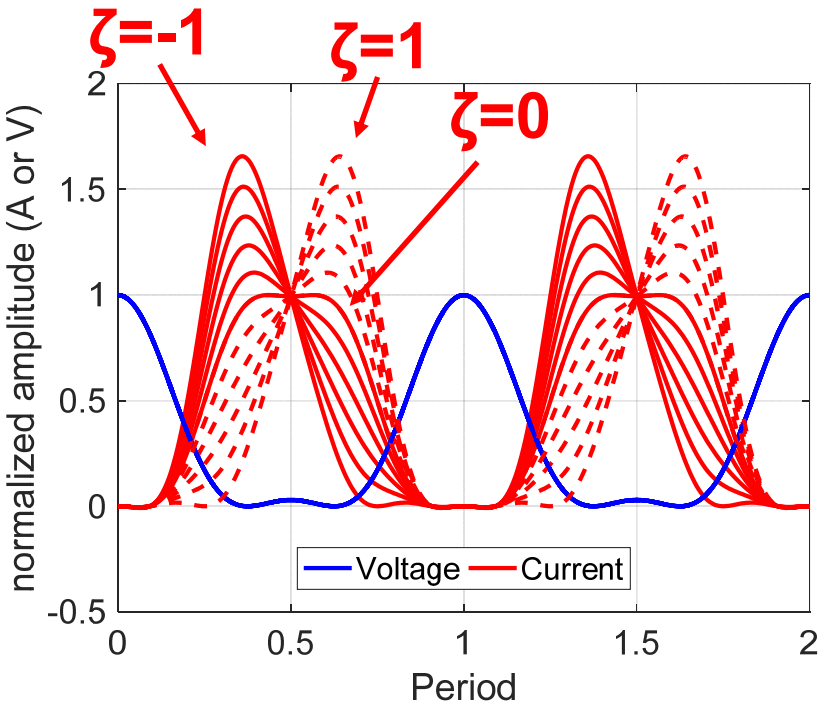
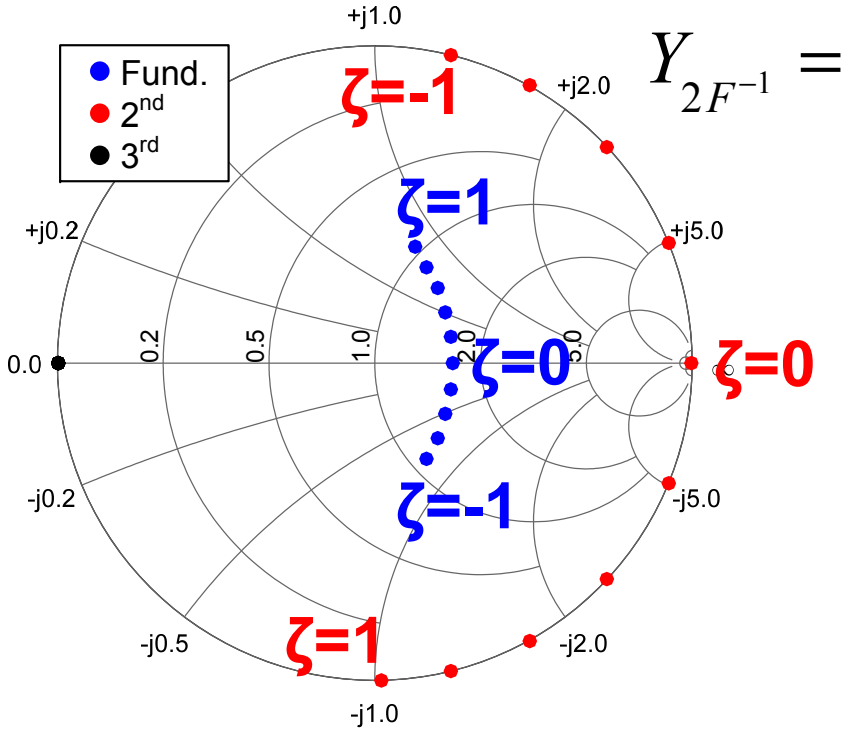
Continuous-Mode Operation

- **Continuous-mode Class-F^{-1}**

  [V. Carrubba et al., T-MTT, 2012]

$$Y_{F^{-1}} = 0.608G_{opt} + j0.523\zeta G_{opt}$$





$$Y_{2F^{-1}} = -j0.98\zeta G_{opt}$$

$$Y_{3F^{-1}} = \infty$$

$$i_{IF}(\theta) = \left(0.37 - 0.43\cos\theta + 0.06\cos 3\theta\right)\left(1 - \zeta\sin\theta\right) \Rightarrow (-1 \le \zeta \le 1)$$

$$V_{IF}(\theta) = 1 + \sqrt{2}\cos\theta + (1/2)\cos 2\theta$$

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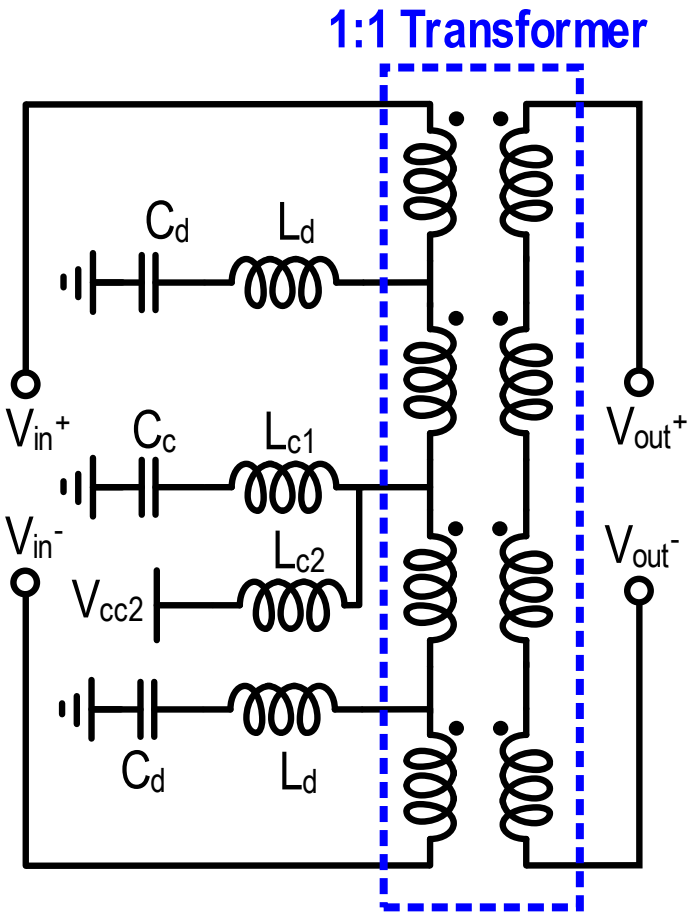
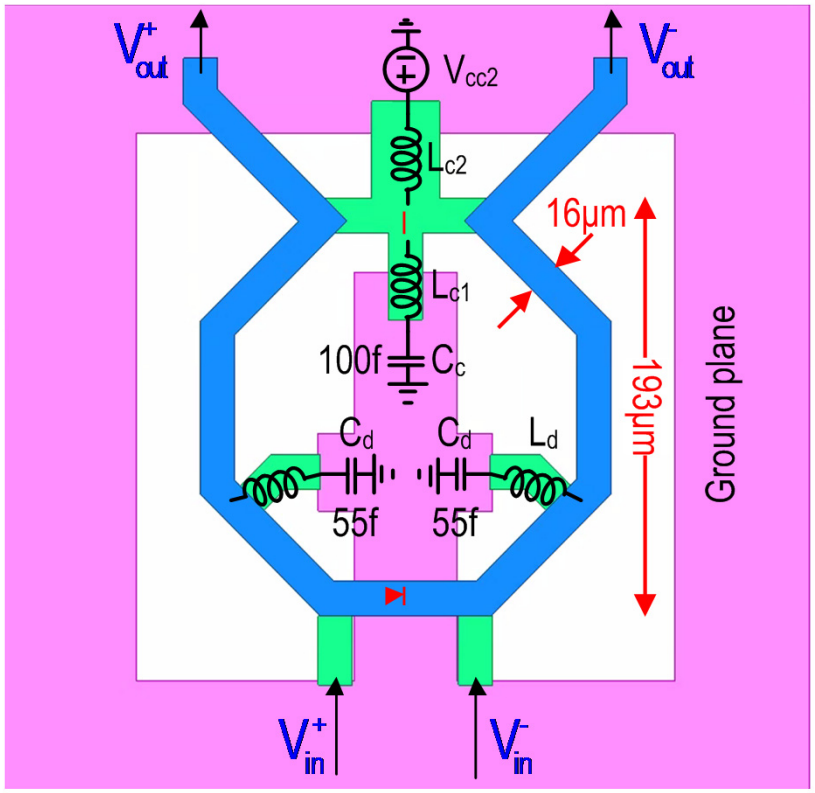
Continuous-Mode PA Output Network





- **1:1 transformer**
- 3 harmonic tuning capacitors ($2\times C_d$ & C_c)
- 2 symmetrically branches ($2\times L_d$)
- 2 extended branches (L_{c1} & L_{c2})

One transformer footprint →Ultra-compact size

No need for any additional tunable elements or switches

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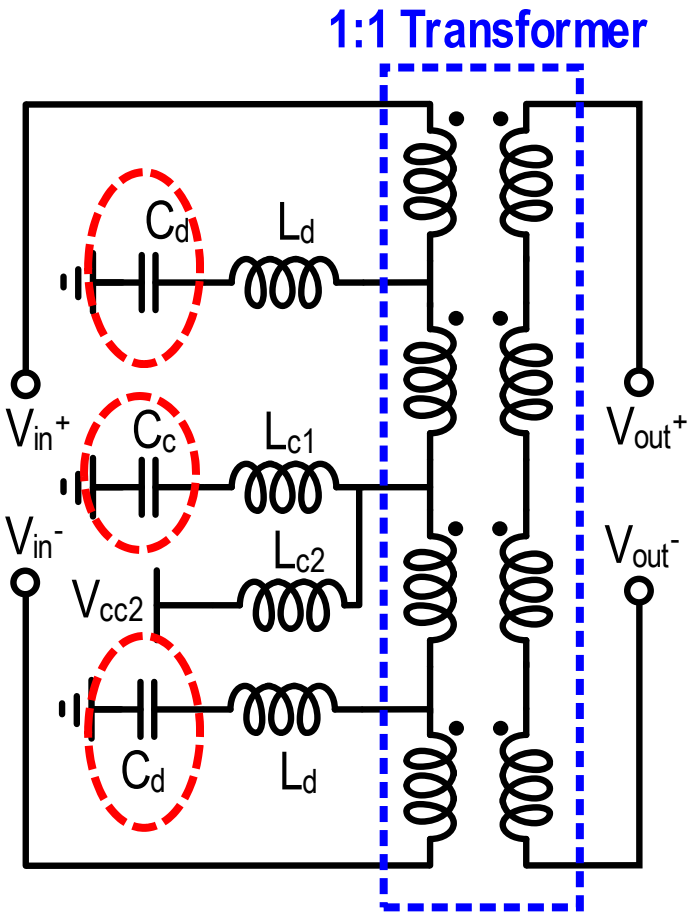
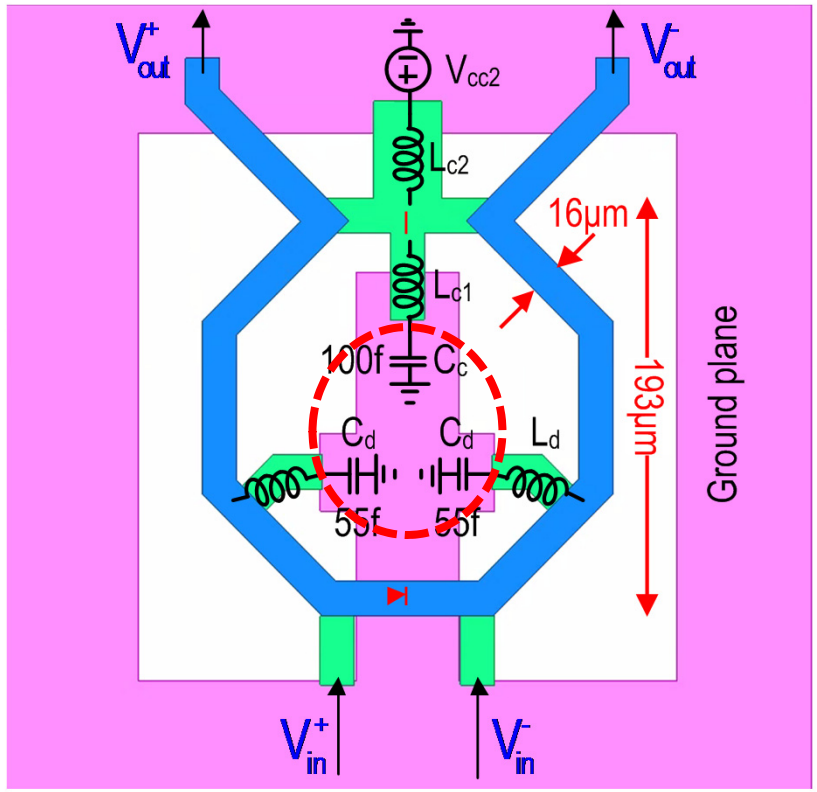
Continuous-Mode PA Output Network





- 1:1 transformer
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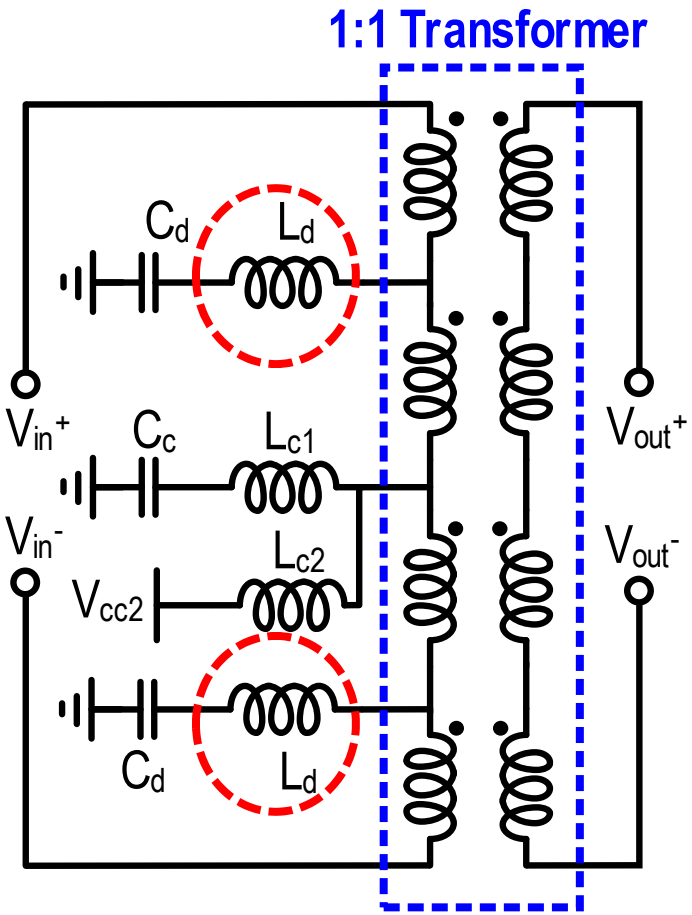
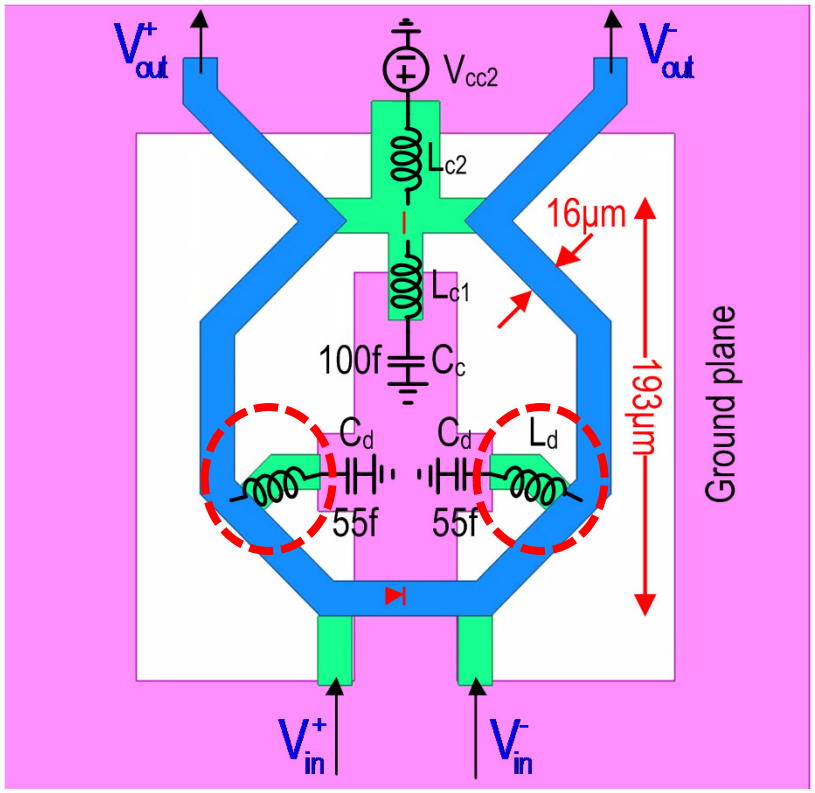
Continuous-Mode PA Output Network





- 1:1 transformer
- 3 harmonic tuning capacitors ($2\times C_d$ & C_c)
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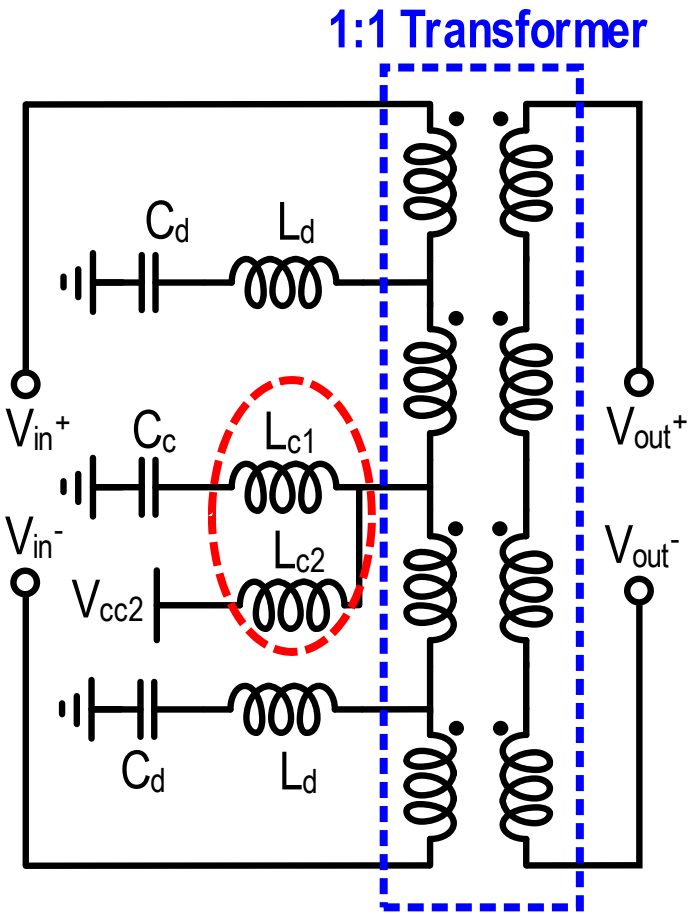
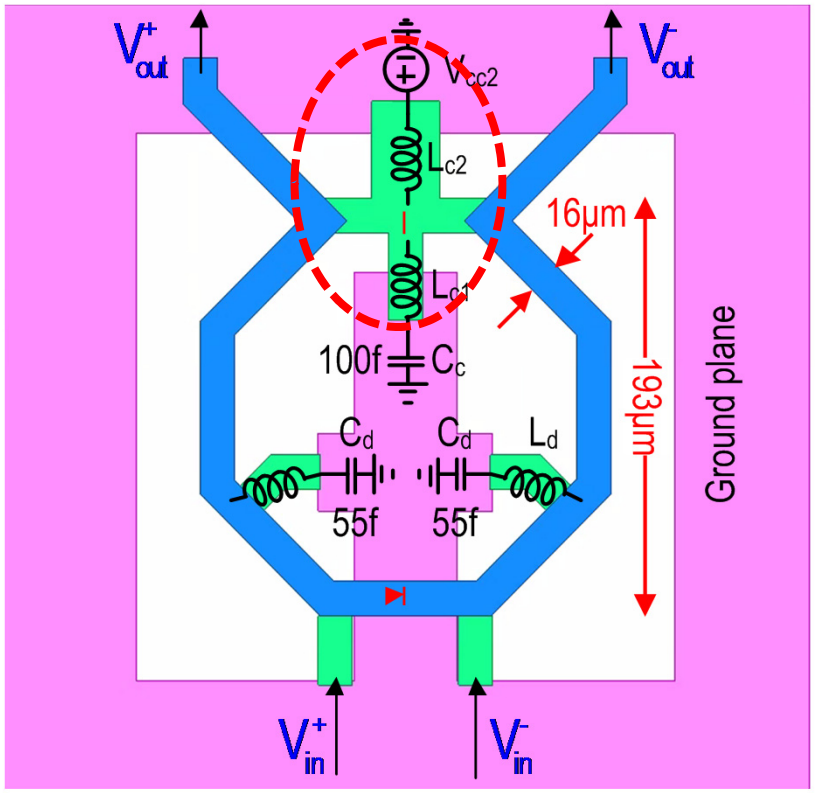
Continuous-Mode PA Output Network





- 1:1 transformer
- 3 harmonic tuning capacitors ($2\times C_d$ & C_c)
- 2 symmetrically branches ($2\times L_d$)
- 2 extended branches (L_{c1} & L_{c2})

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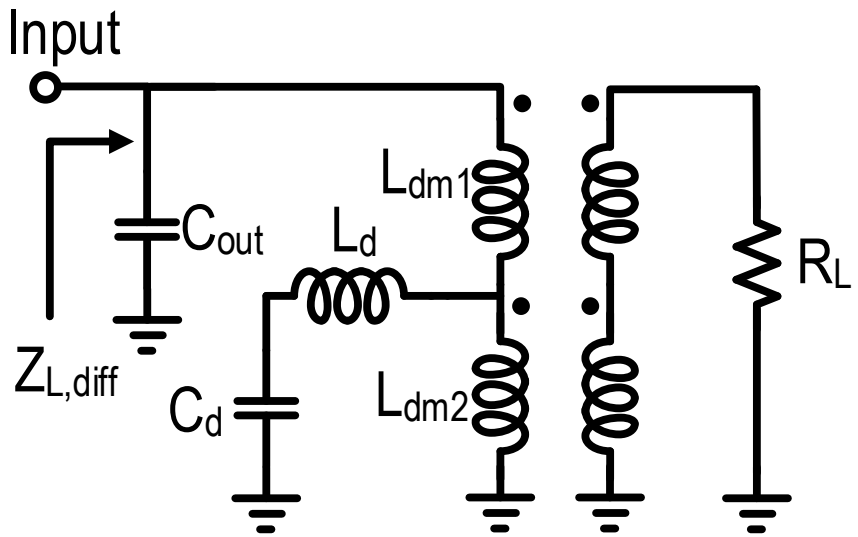
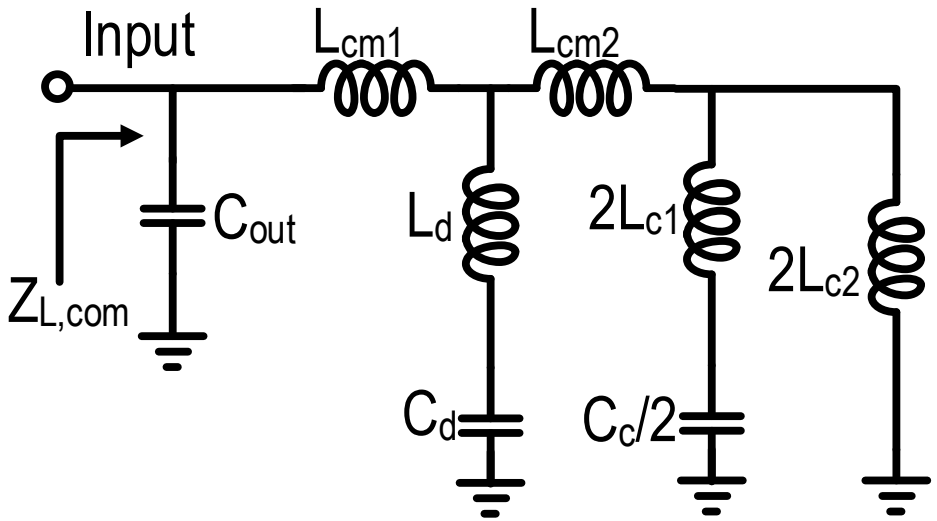
Simplified Schematic Model

- **The output network can be simplified into differential-/common-mode respectively**

Differential-mode Half Circuit



Common-mode Half Circuit



Output leads are absorbed into transformer secondary coil

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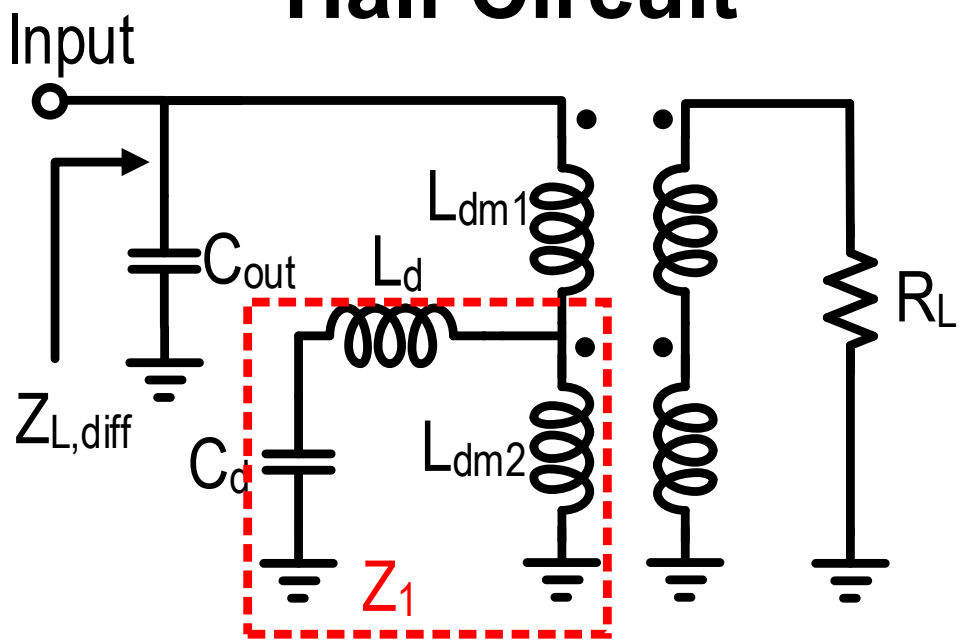
Simplified Differential-Mode Model

Differential-mode Half Circuit



- L_{dm1}/L_{dm2}: differential-mode half-circuit inductances of transformer
- C_d-L_d-L_{dm2} forms a multi-resonance tank Z_1

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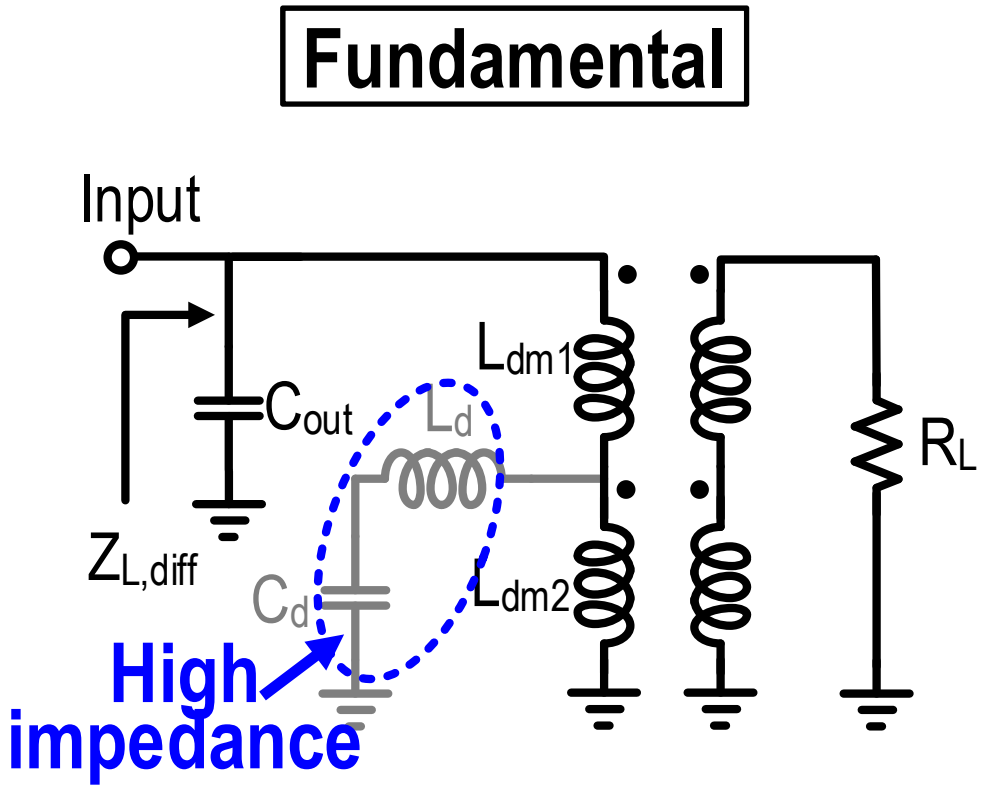
Load Impedance Trajectory

- **Differential-mode operation**



- **C_d-L_d behaves as a small cap. → a high impedance**
- **The transformer provides the desired fund. impedance**

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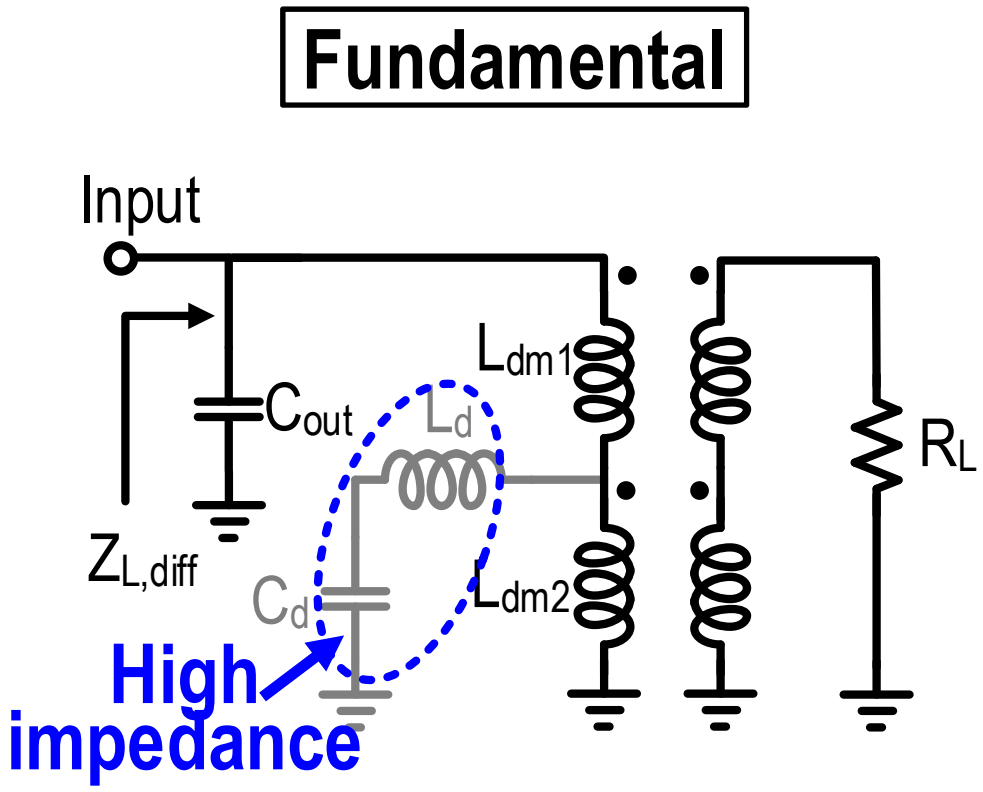
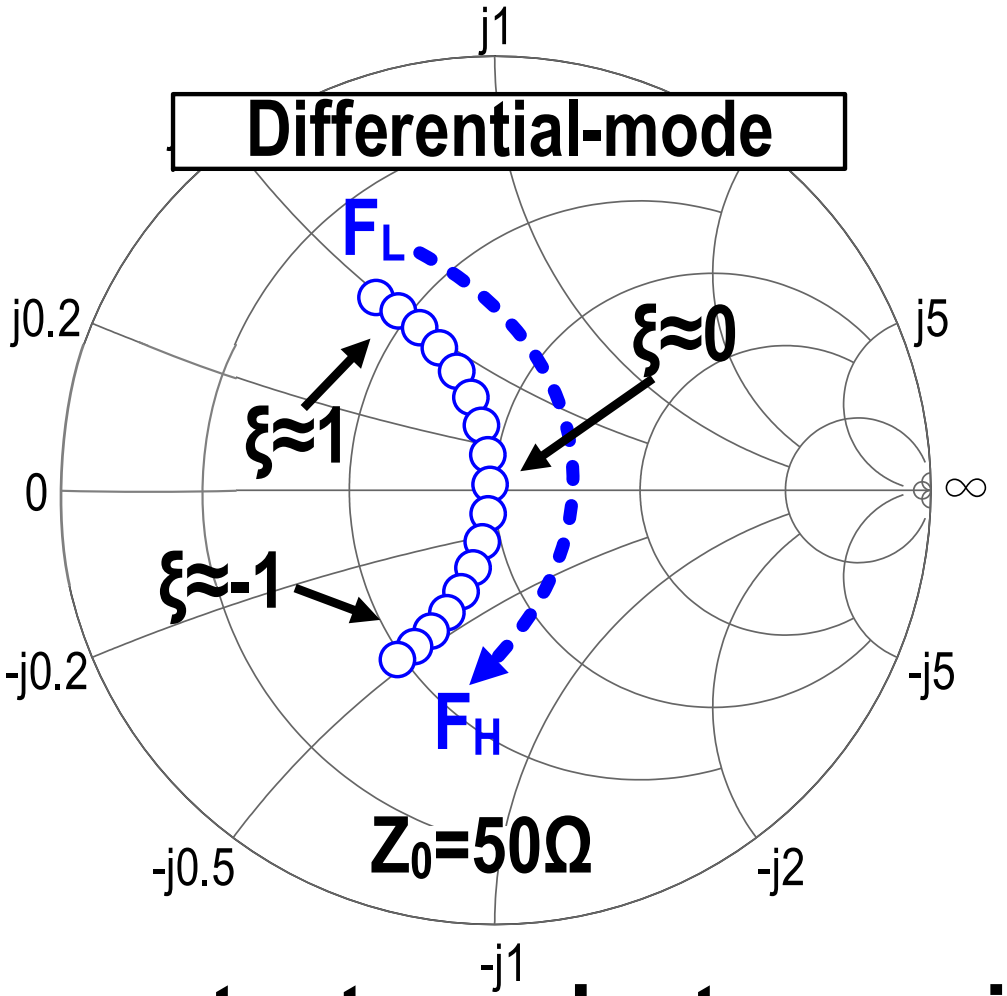
Load Impedance Trajectory

- **Differential-mode operation**





Fund. load impedance follows constant conductance circle

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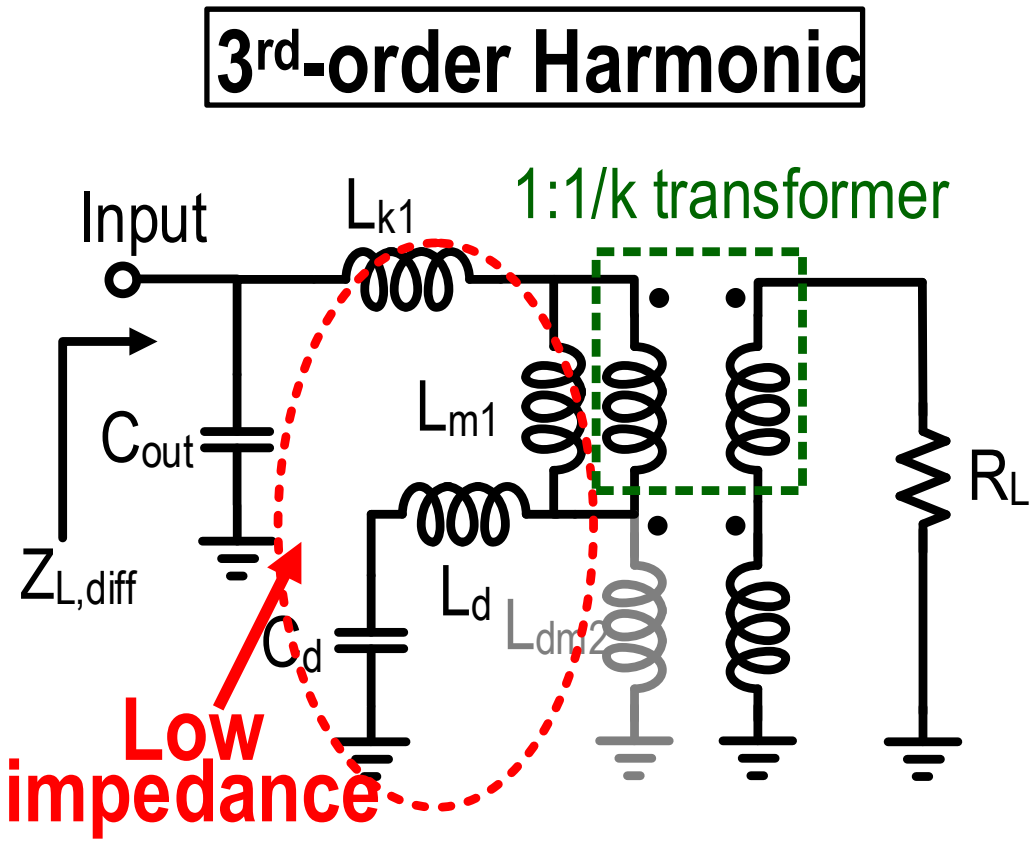
Load Impedance Trajectory

- **Differential-mode operation**



- **C_d-L_d is slightly below their series resonance → shorts out L_{dm2}**
- **C_d-L_d-L_{m1}-L_{k1} produces a desired low impedance**
- **L_{m1} and L_{k1} are magnetizing and leakage inductances of the transformer**

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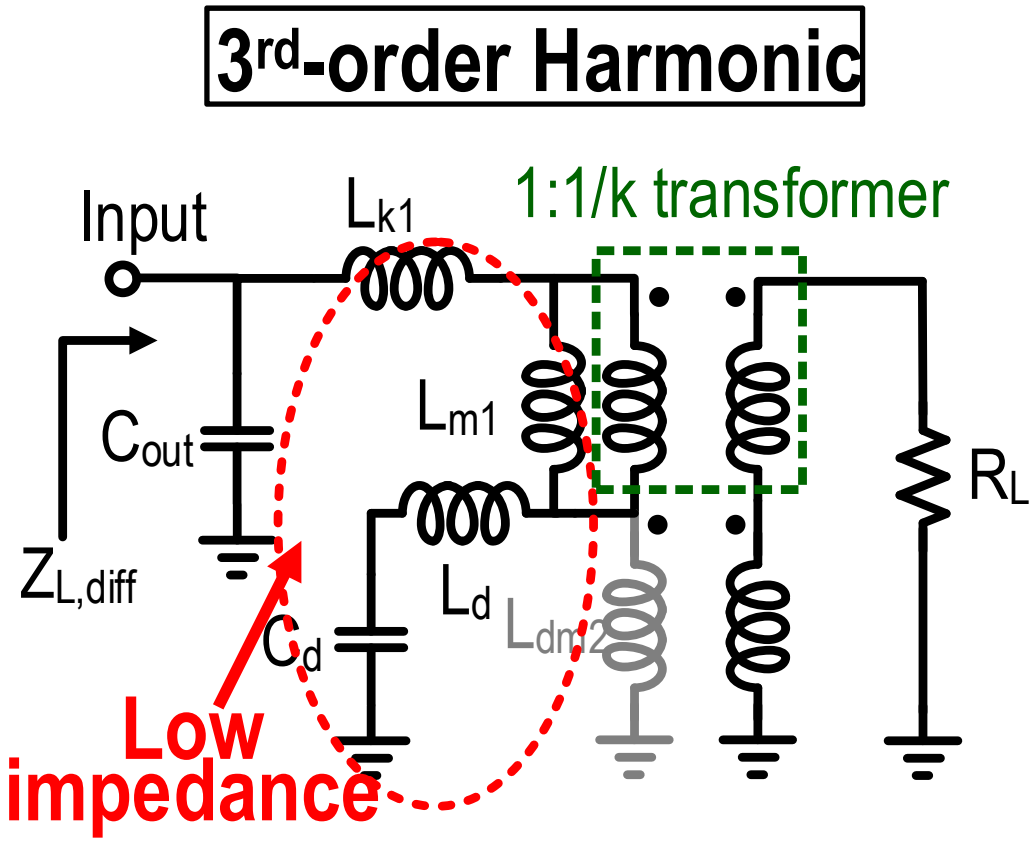
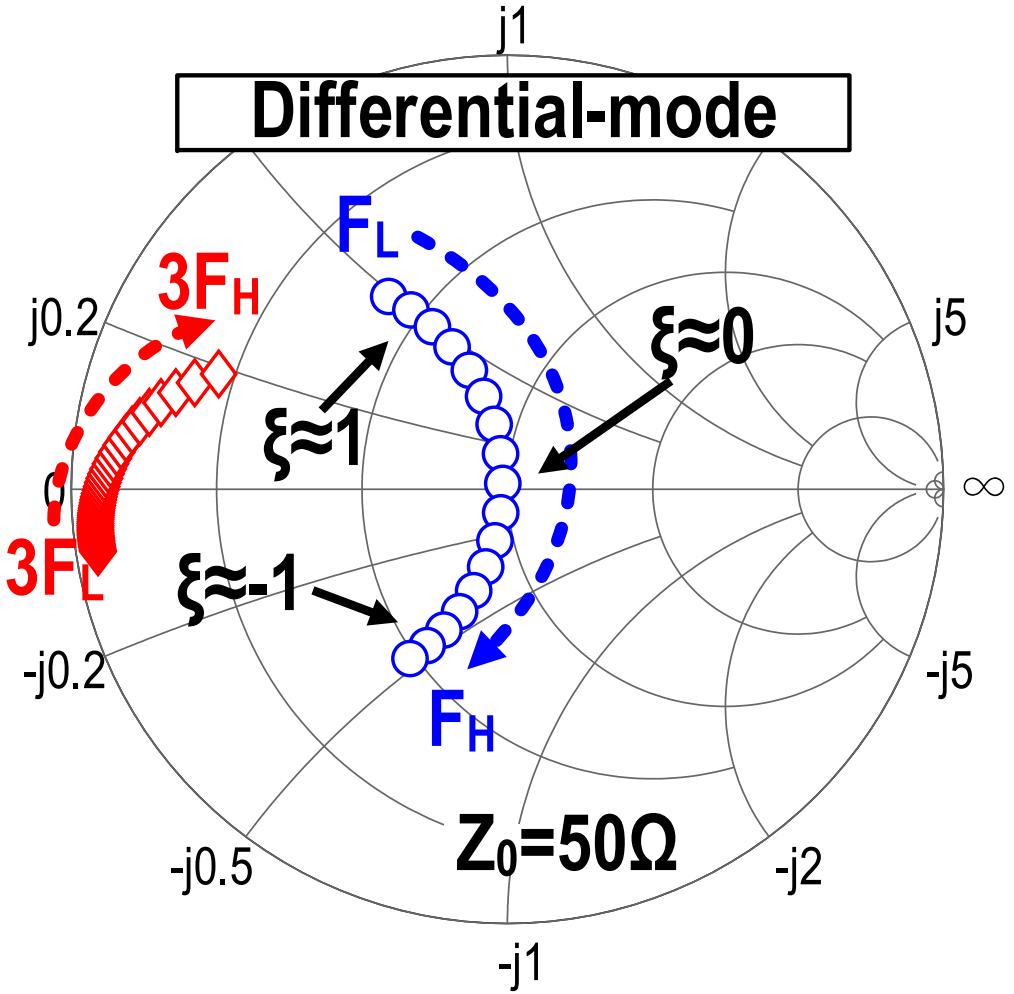
Load Impedance Trajectory

- **Differential-mode operation**





3rd harmonic load impedance is kept low

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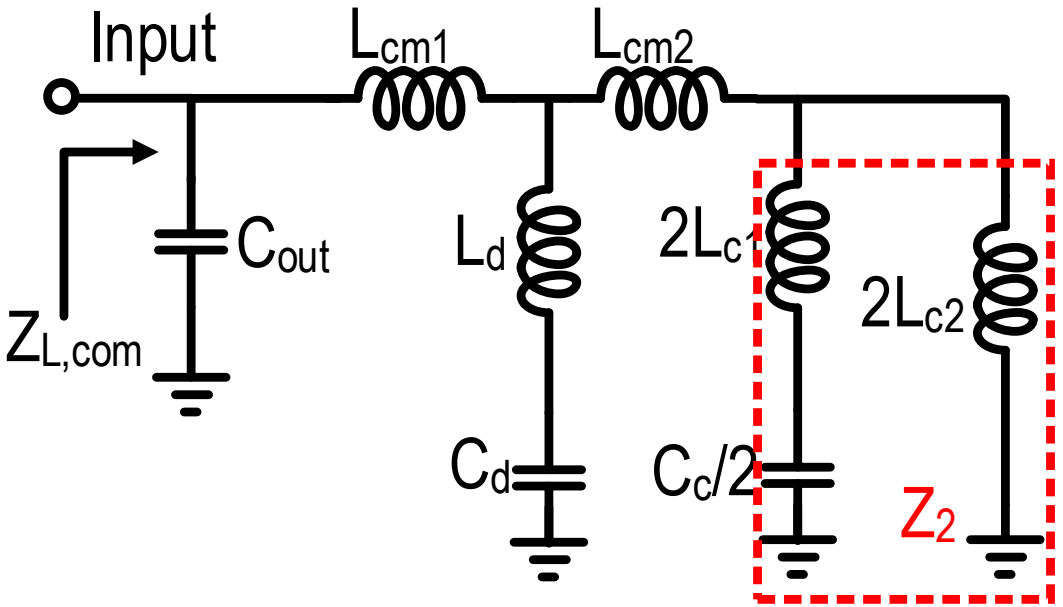
Simplified Common-Mode Model

Common-mode Half Circuit



- L_{cm1}/L_{cm2}: common-mode half-circuit inductances of transformer
- C_c, L_{c1} and L_{c2} do not affect differential-mode
- $C_c/2$-$2L_{c1}$-$2L_{c2}$ forms a multi-resonance tank Z_2

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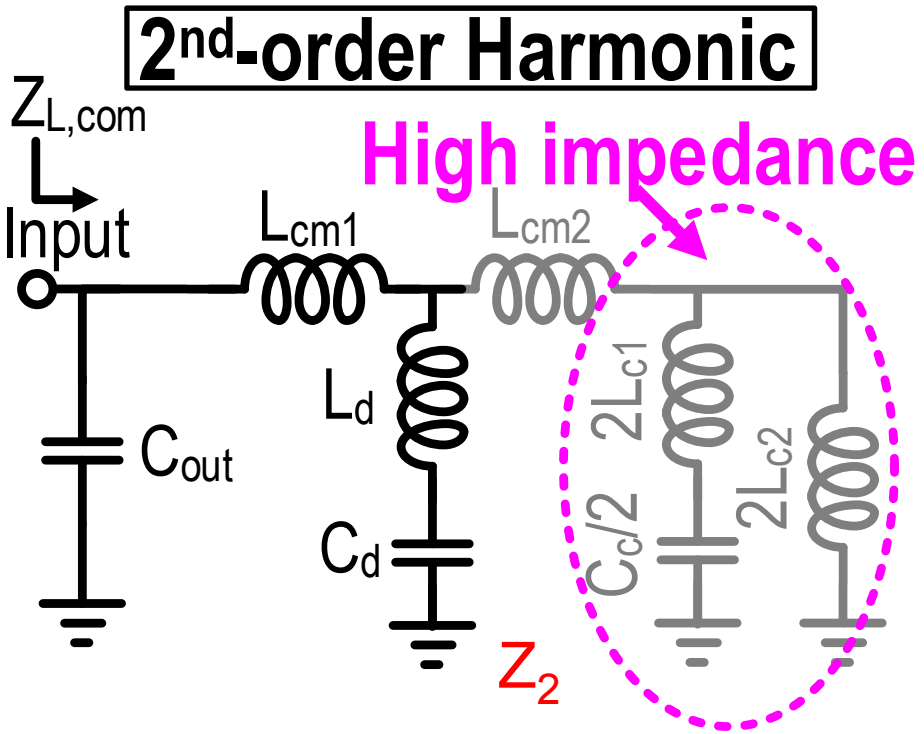
Load Impedance Trajectory

- **Common-mode operation**



- **Z_2 provides a high impedance**
- **C_d-L_d still behaves as a capacitor**

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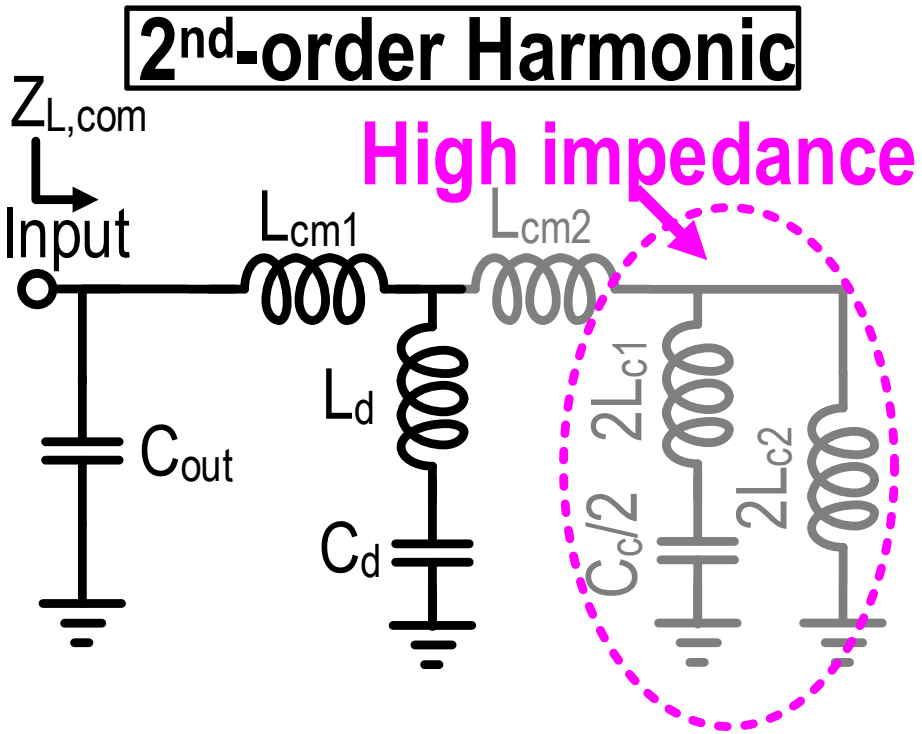
Load Impedance Trajectory

- **Common-mode operation**



The 2nd harmonic impedance is dominated by C_{out}, L_{cm1} and the effective capacitance of C_d-L_d

→desired continuous-mode 2nd harmonic impedance

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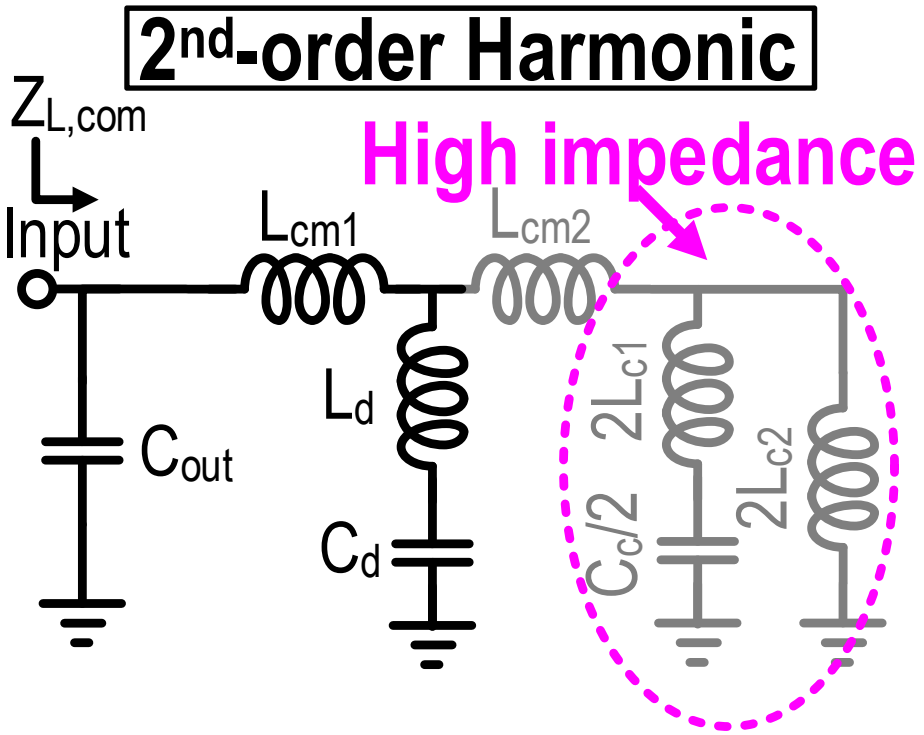
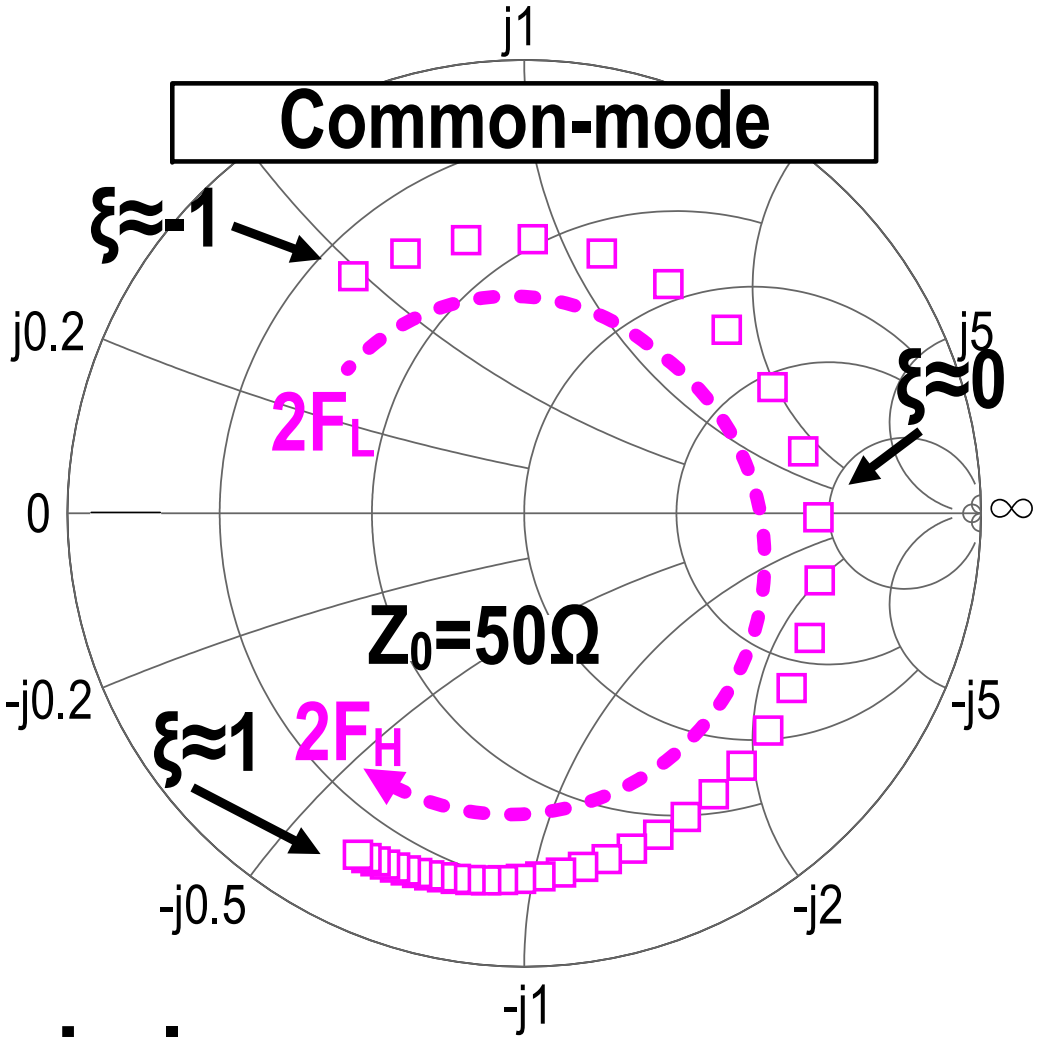
Load Impedance Trajectory

- **Common-mode operation**





2nd harmonic load impedance follows constant conductance circle

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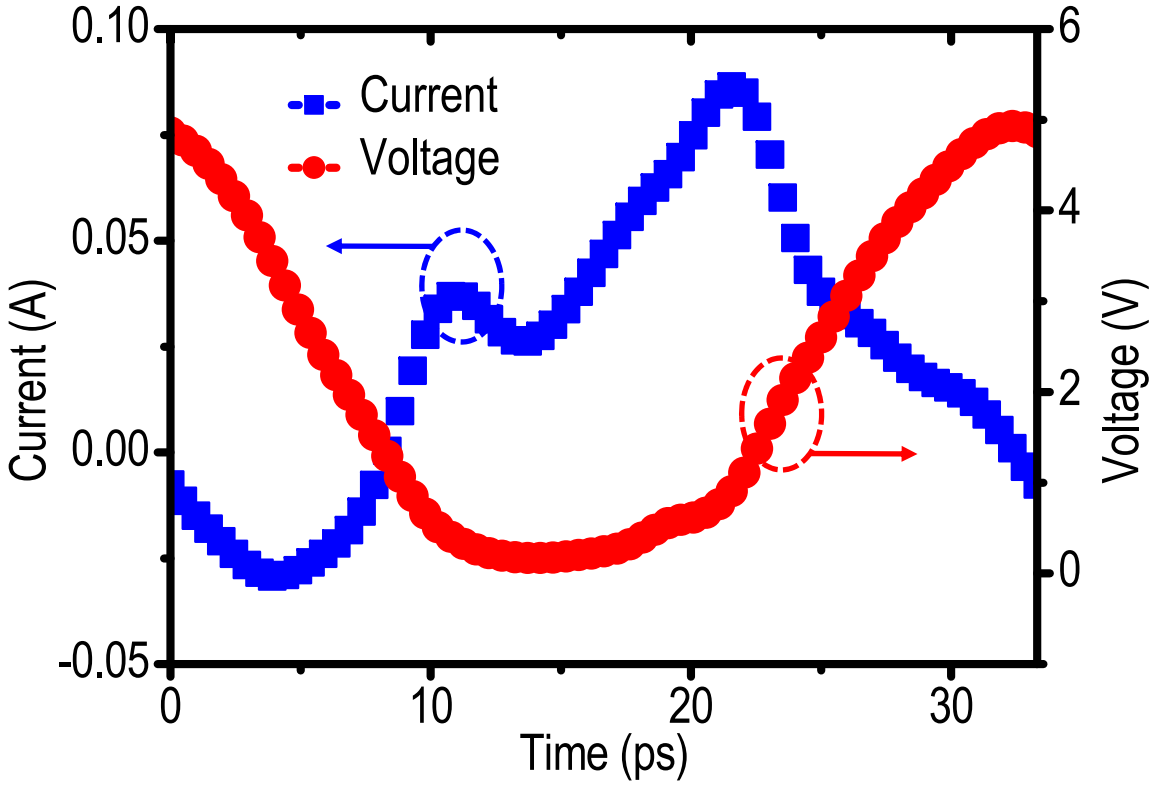
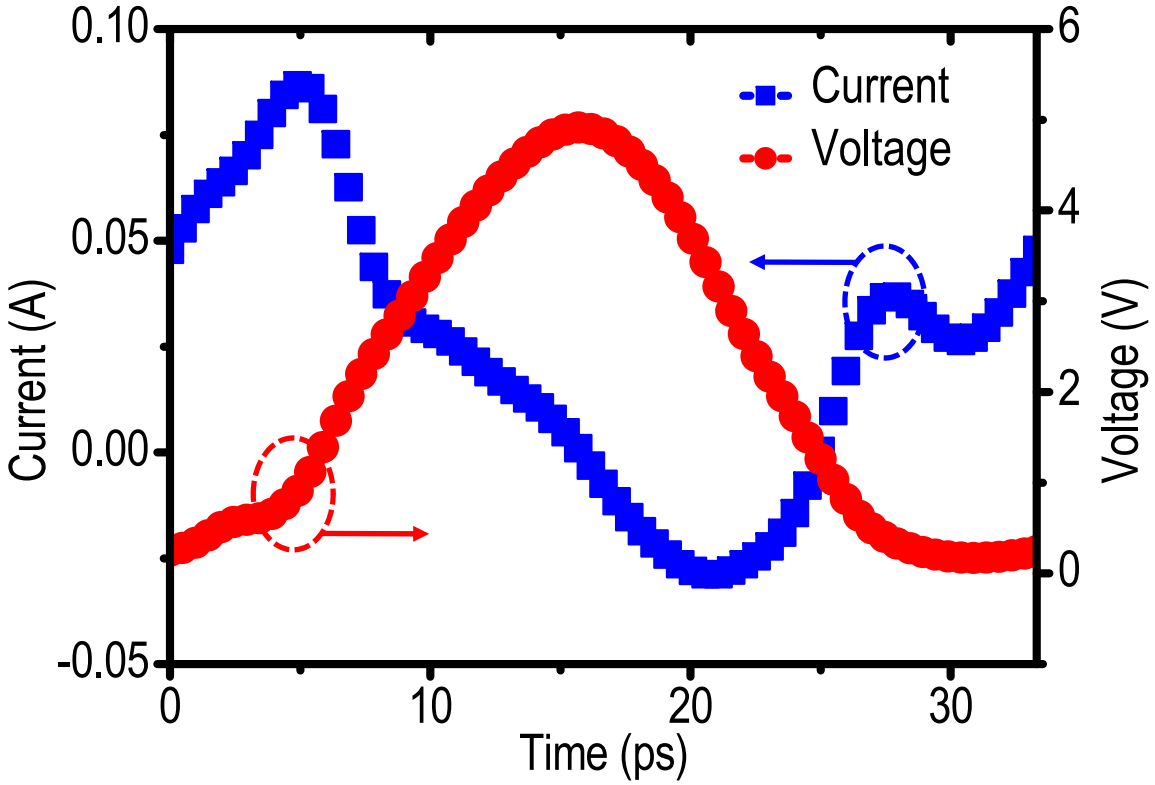
Simulated Voltage/Current Waveform

Differential+



Differential-



Frequency=28.5GHz and P_{out}=16dBm

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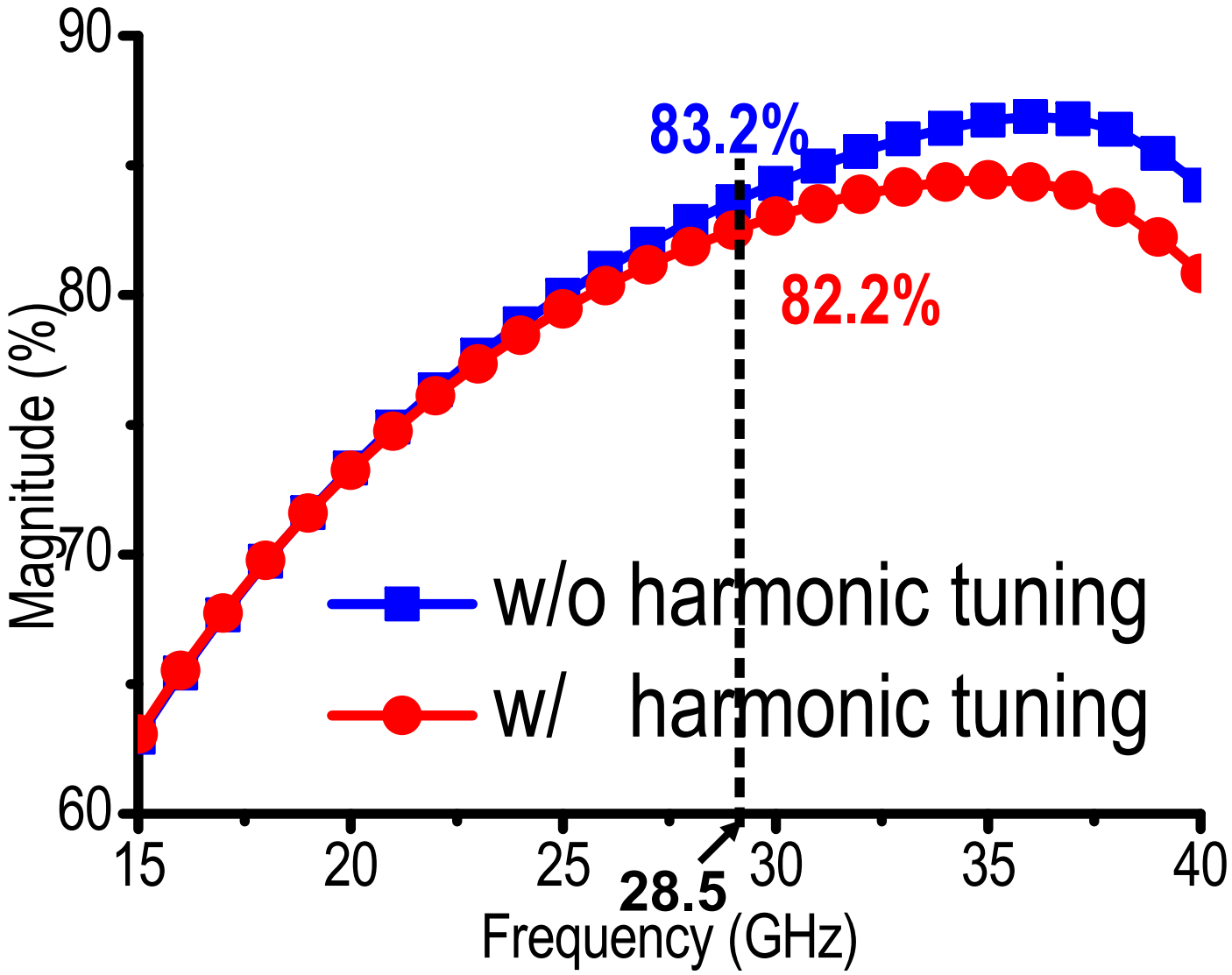
Simulated Passive Efficiency



- **Harmonic-tuning branches and cap do not significantly degrade the passive efficiency**

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Outline

- Introduction
- Harmonically tuned continuous-mode PA output network
- **PA schematic and implementation**
- Measurement results
- Conclusion

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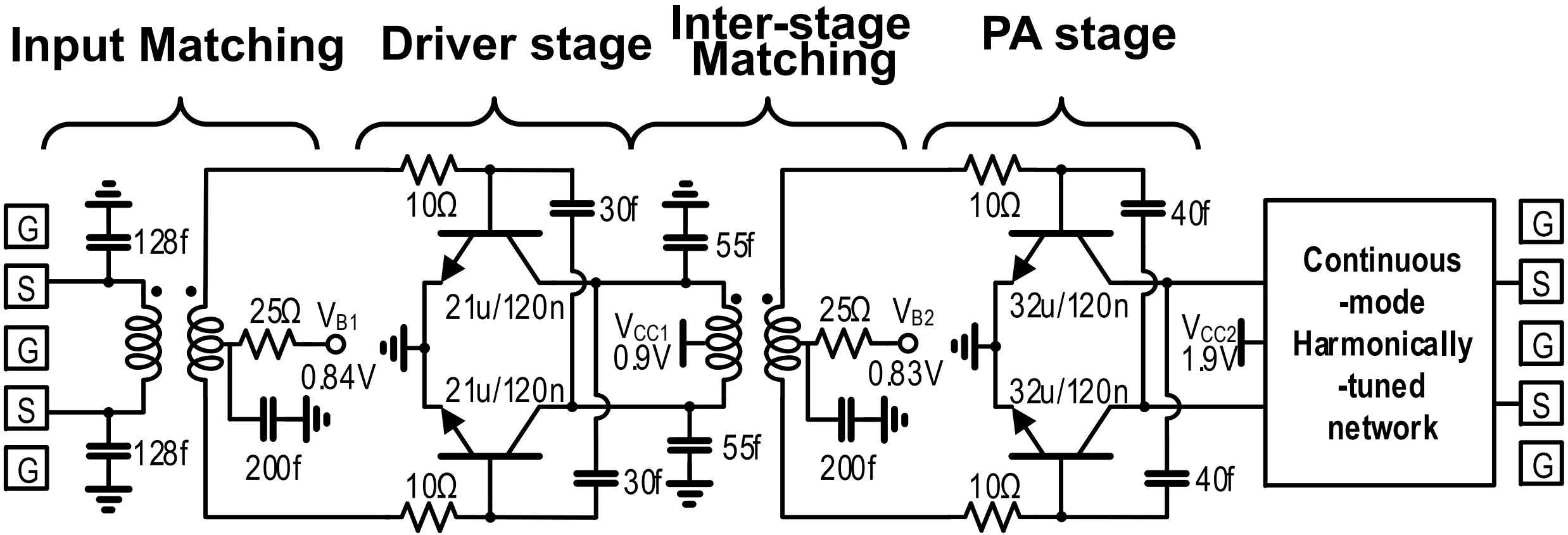
PA Schematic



Differential 2-stage PA, R_L=100ohm (Diff.)

V_{CC1}=0.9V and V_{CC2}=1.9V

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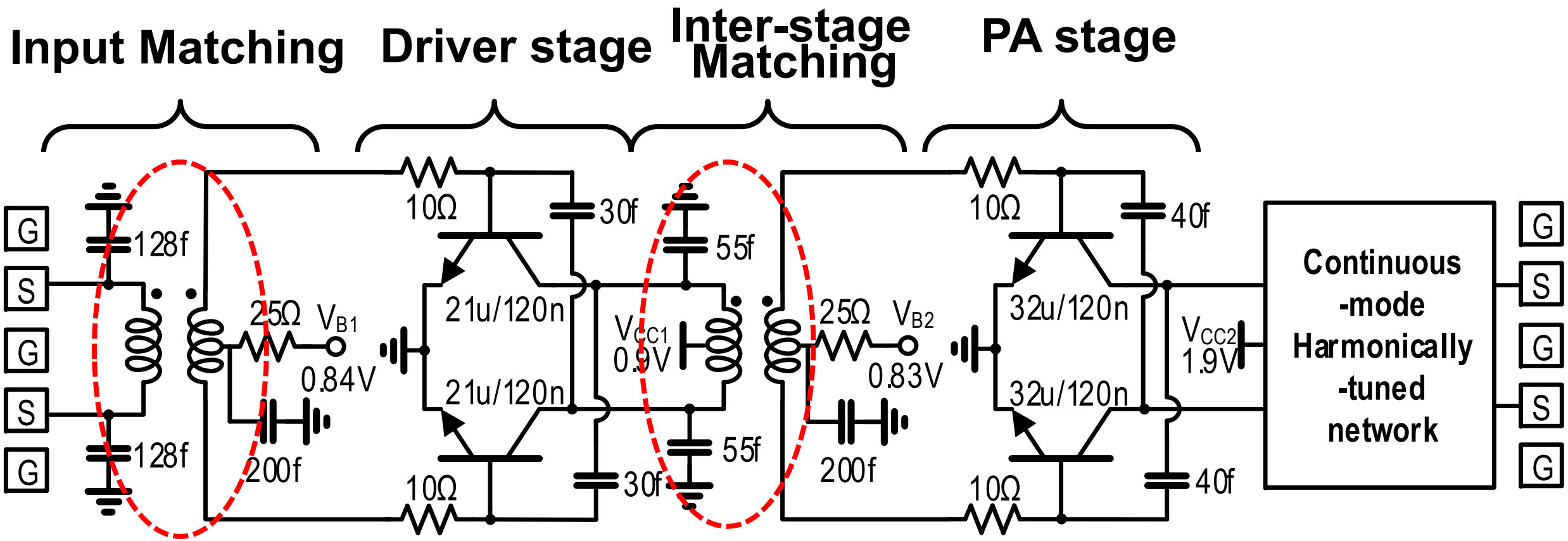
PA Schematic



1:1 transformer and two parallel capacitors for input/inter-stage matching

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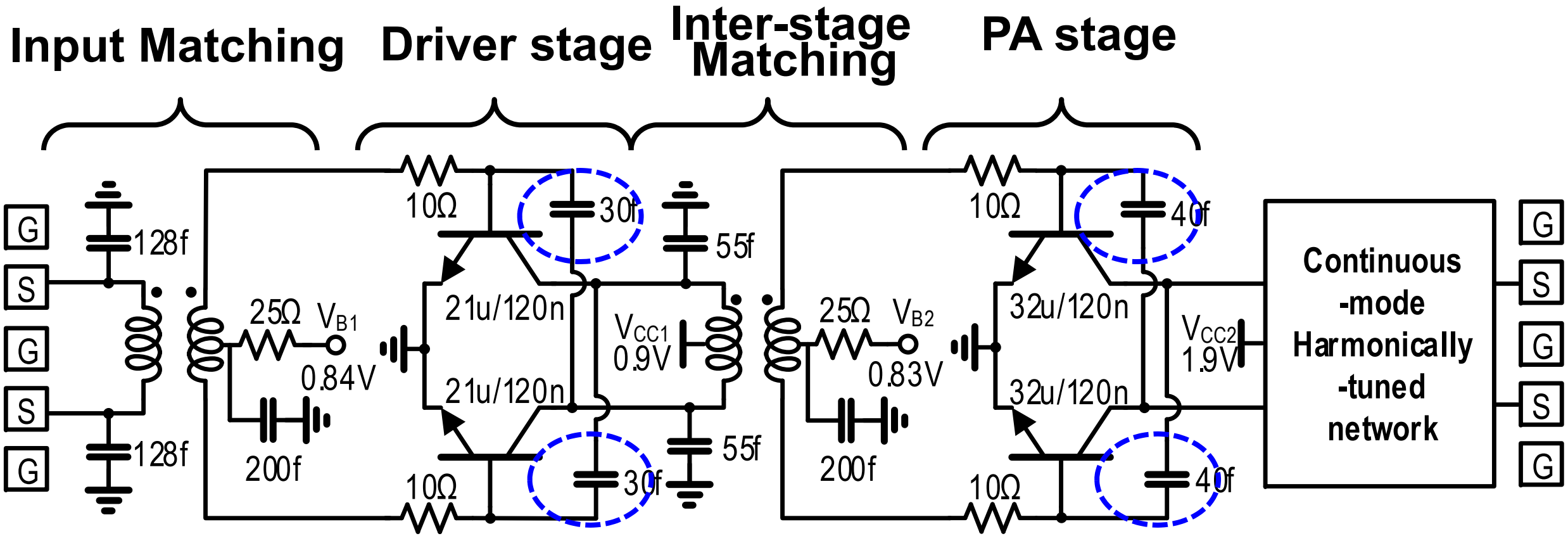
PA Schematic



Neutralization cap. improve power gain, reverse isolation, and stability

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Outline

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- Conclusion

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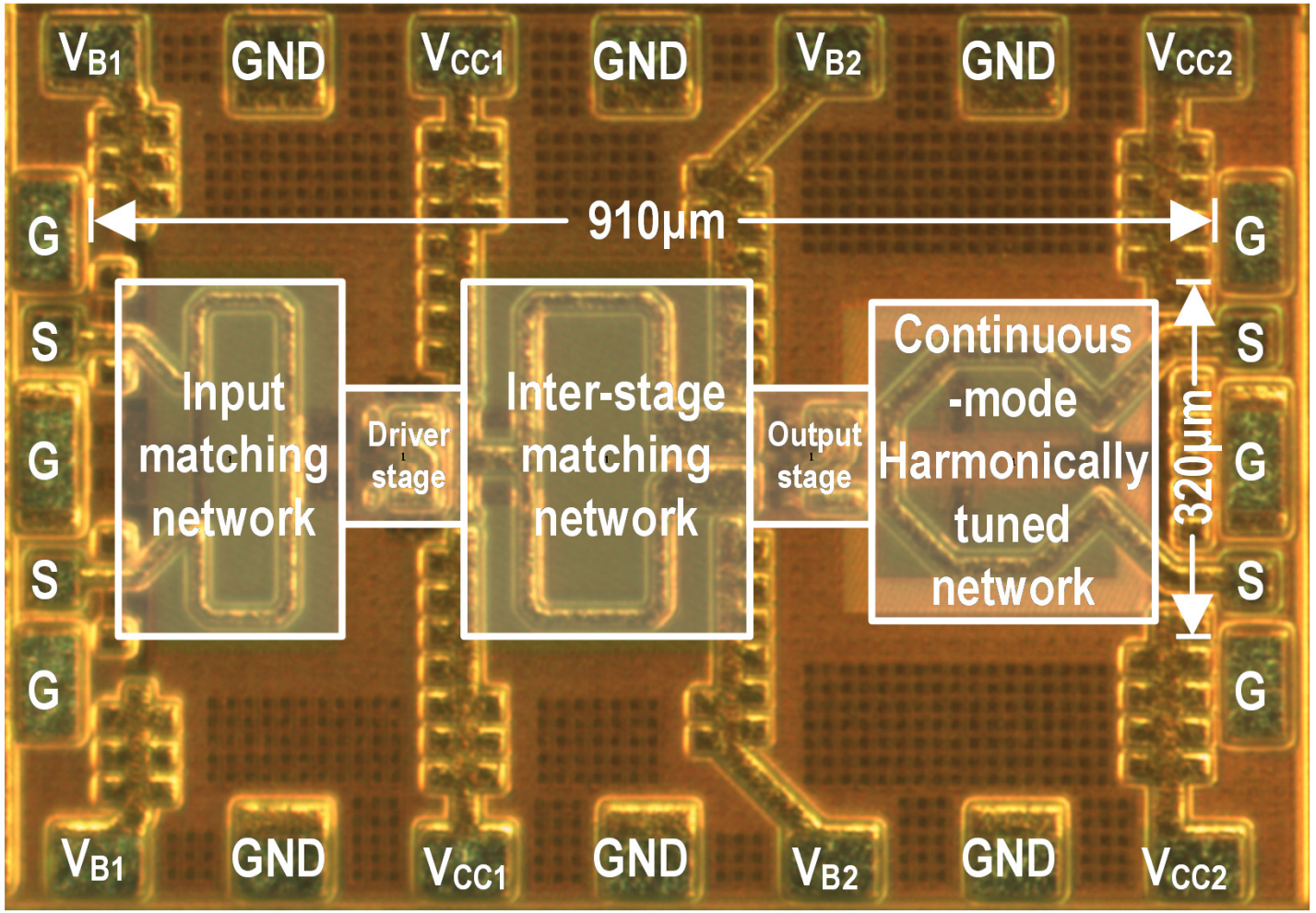
PA Die Micrograph



- 0.13μm SiGe BiCMOS
- The core size: 0.29mm^2
- Direct probing

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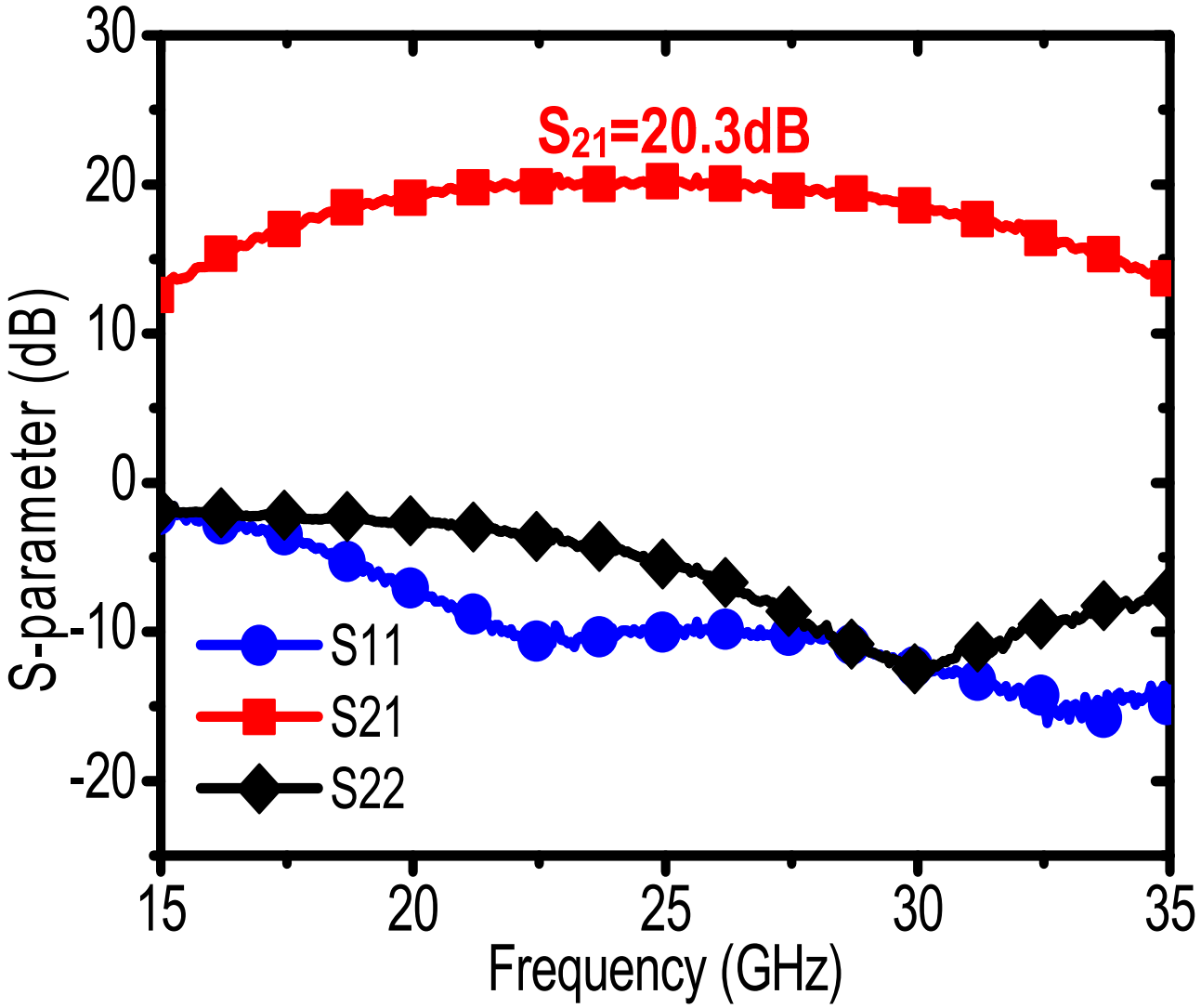
Small-Signal S-Parameter Measurement



- S_{21}=20.3dB@24.5GHz
- BW_{3dB}=20.2~28.9GHz (35.4%)
- BW_{S11}=21.5~39GHz (57.9%)

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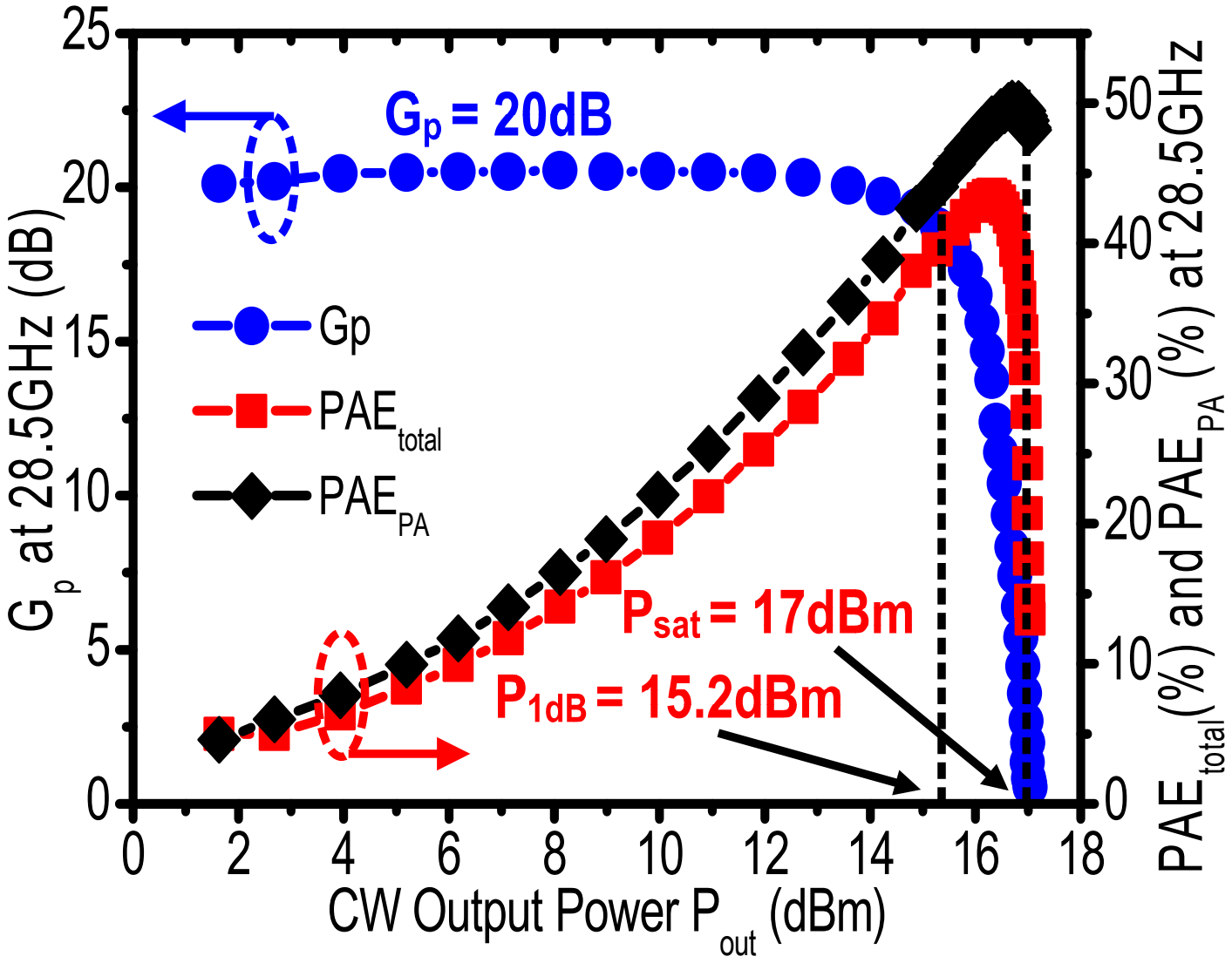
Large-Signal CW Measurement



- 28.5GHz
- Gain: G_p=20dB
- P_{sat}=17dBm
- OP_{1dB}=15.2dBm
- PAE_{total}=43.5%
- PAE_{PA}=50%
- P_{dc_PA}@PAE_{PA} =78.7mW

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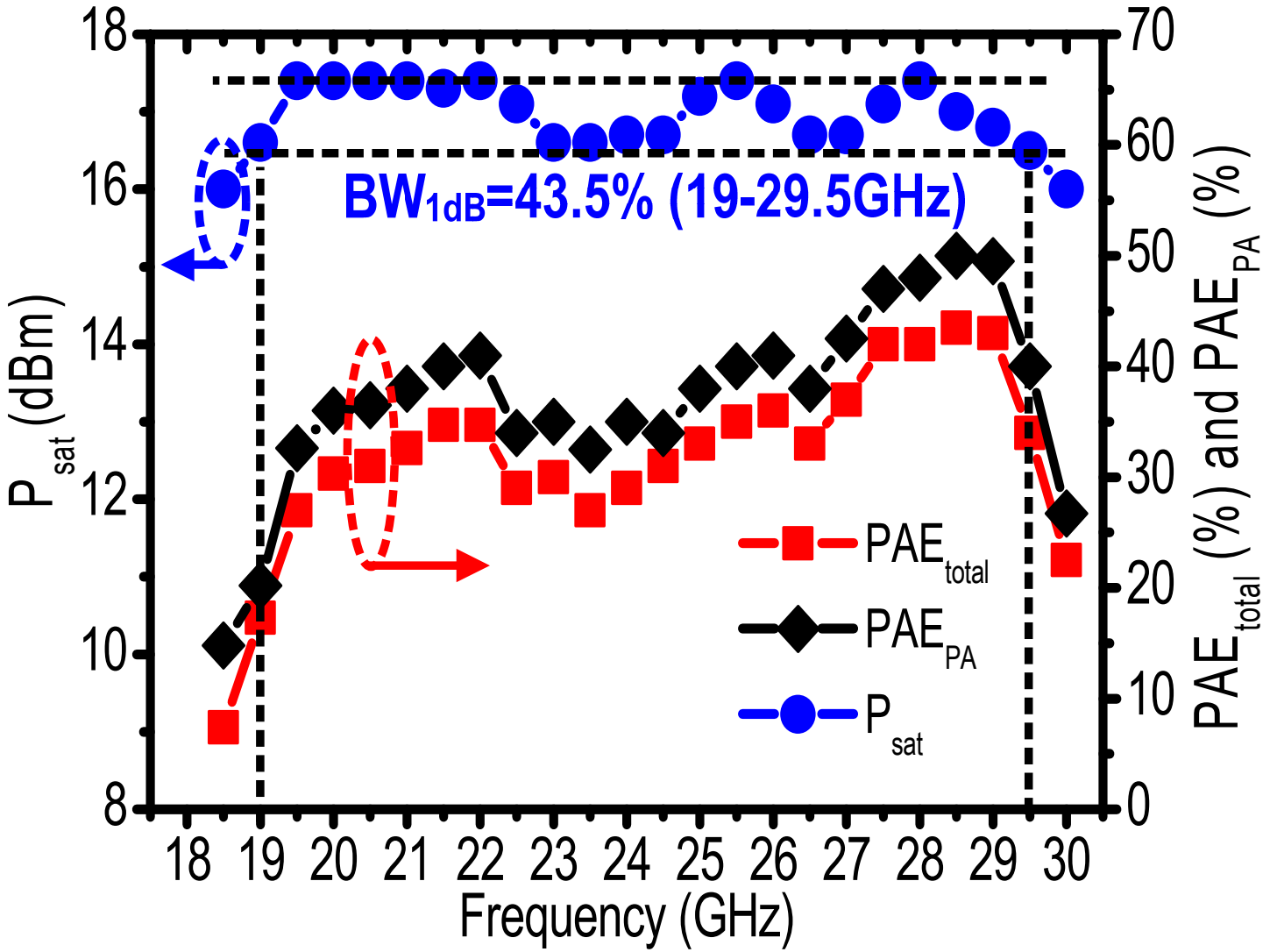
Large-Signal Peformance vs. Frequency



P_{sat} 1dB BW

=19~29.5GHz(43.3%)

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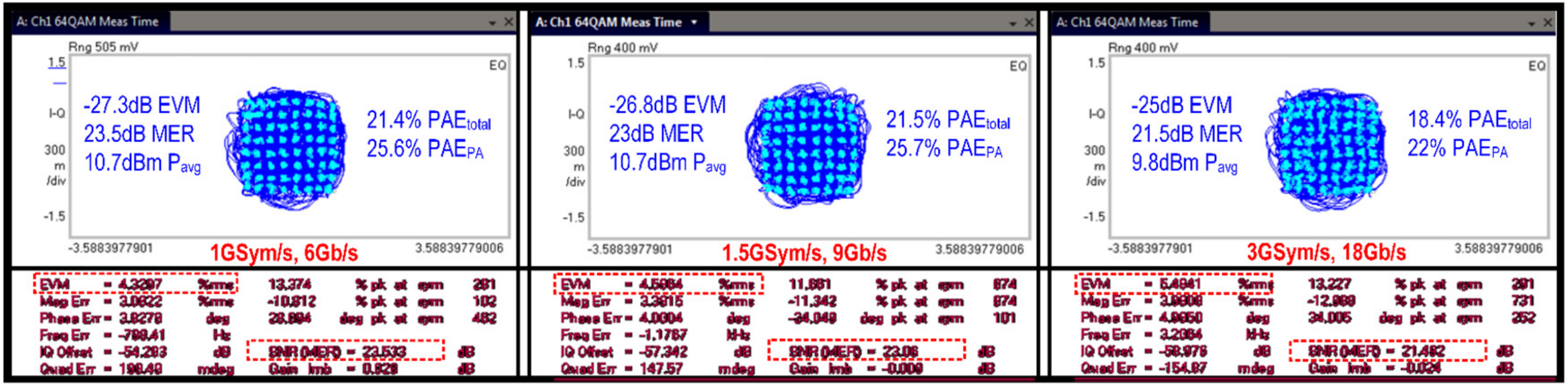
64-QAM Modulation Measurement

Carrier frequency=28.5GHz



EVM are below -25dB for measured symbol rates

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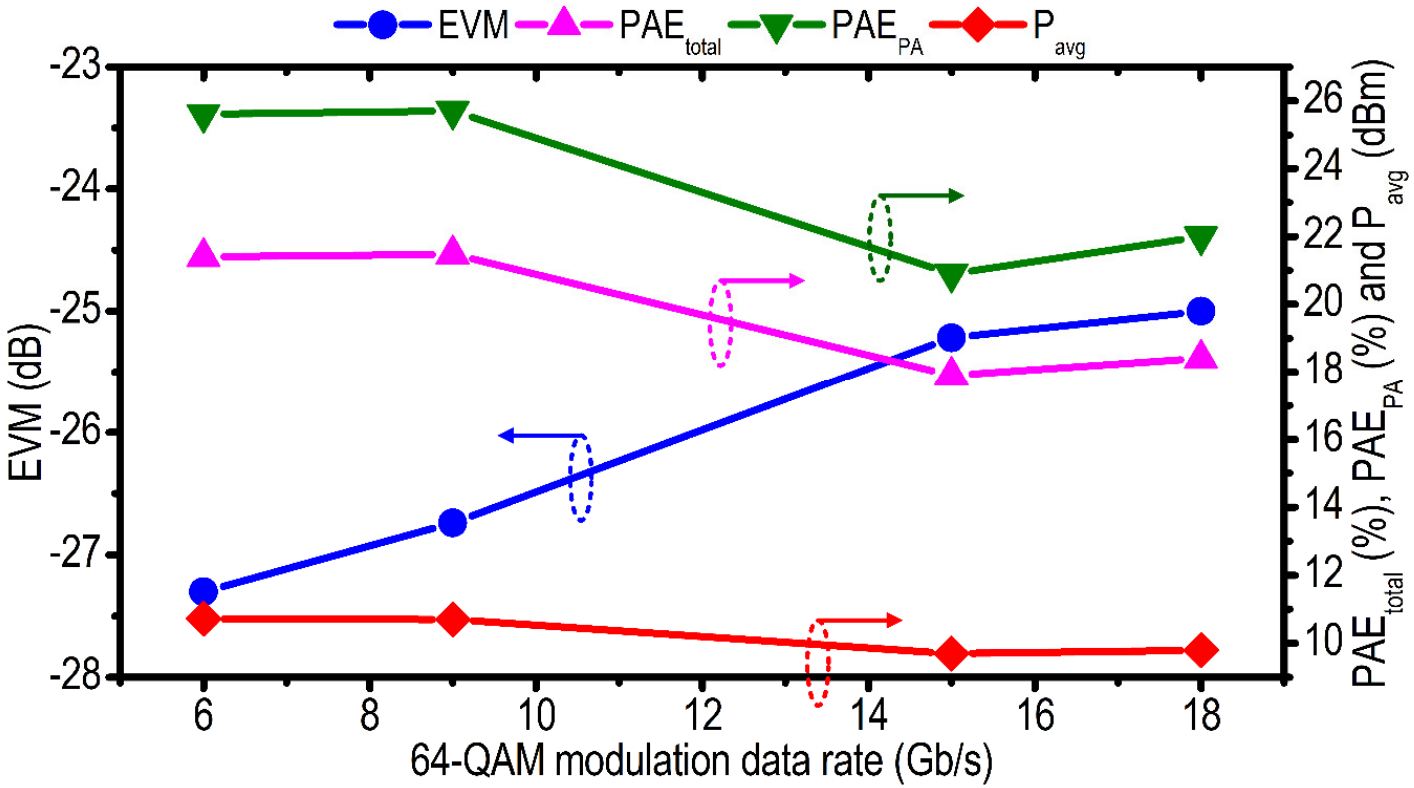
64-QAM Modulation Measurement



Data rate (Gb/s)	EVM (dB)	P_{out}@EVM (dBm)	PAE_{total}@EVM(%)
6	-27.6	10.7	21.4
9	-26.8	10.7	21.5
18	-25	9.8	18.4

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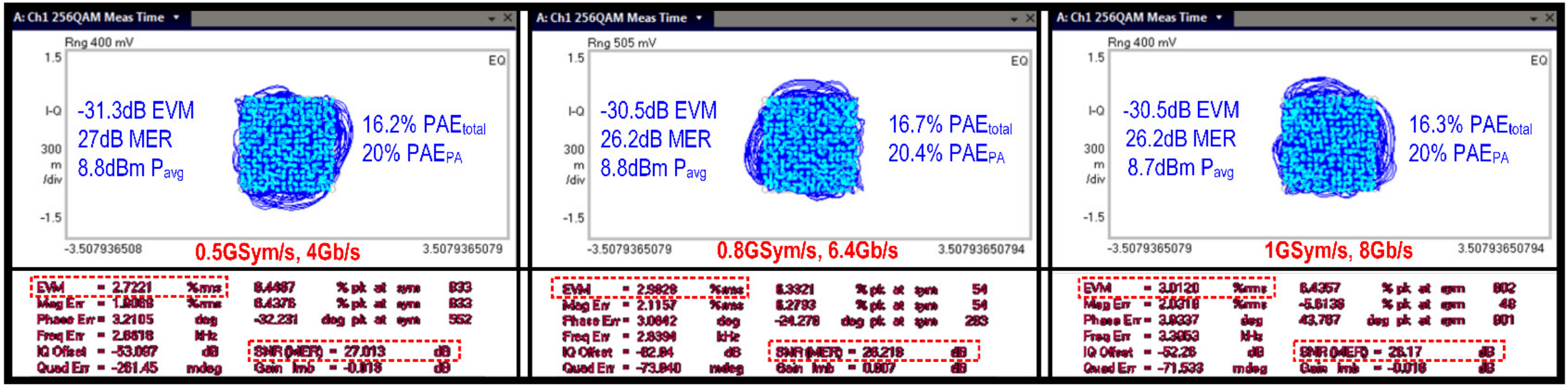
256-QAM Modulation Measurement

Carrier frequency=28.5GHz



EVM are below -30dB for measured symbol rates

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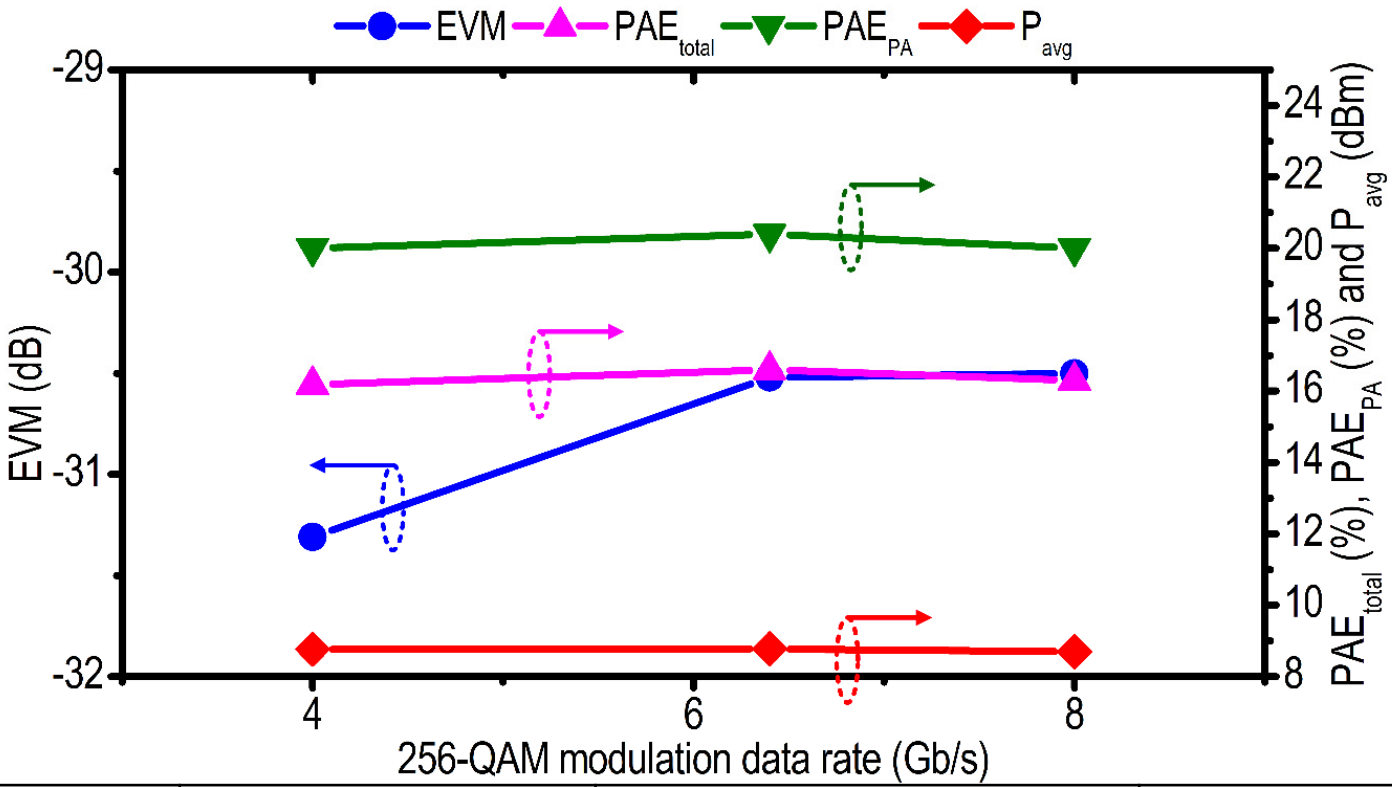
256-QAM Modulation Measurement



Data rate (Gb/s)	EVM (dB)	P_{out}@EVM (dBm)	PAE_{total}@EVM(%)
4	-31.3	8.8	16.2
6.4	-30.5	8.8	16.7
8	-30.5	8.7	16.3

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Comparison Table

	This work	S. Ali RFIC 17	A. Sarkar T-MTT 17	S. Shakib ISSCC 17	S. Hu ISSCC 17	B. Park T-MTT16	P. Indirayanti RFIC 17	M. Vigilante RFIC 17
Technology	**130nm SiGe**	65nm CMOS	130nm SiGe	40nm CMOS	130nm SiGe	28nm CMOS	28nm CMOS	28nm CMOS
PA supply (V)	**1.9**	1.1	3.6	1.1	1.5	2.2	1	0.9
P_{out} 1dB Frequency (GHz)	**19-29.5**	26-34	27-29	27-30#	28-42	26.5-29#	28-33#	25-48#
P_{out} 1dB Bandwidth	**43.3%**	26.7%	7.1%	10.5%#	40%	10.7%#	22.2%#	63%#
Gain (dB)	**20**	10	15.5	22.4	18.2	13.6	22	20.8
P_{sat} (dBm)	**17**	14.8	18.8	15.1	16.8	19.8	19.8	16.6
P_{1dB} (dBm)	**15.2**	13.2	15.9	13.7	15.1	18.6	16	13.4
PAE_{total} (%)* (2-stage PA)	**43.5**	-	-	33.7	22.6	-	21	24.2
PAE_{PA} (%)** (1-stage PA)	**50**	46.4	35.3	-	-	43.3	-	-
$PAE_{total}@P_{1dB}$ (%)	**39.2**	-	-	31.1	21.6	-	12.8	12.6
$PAE_{PA}@P_{1dB}$ (%)	**43**	39#	31.5	-	-	41.4	-	-

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Comparison Table

	This work						S. Ali RFIC 17	A. Sarkar T-MTT 17	S. Shakib ISSCC 17	S. Hu ISSCC 17	B. Park T-MTT16	P. Indirayanti RFIC 17	M. Vigilante RFIC 17
Modulation scheme	**64-QAM**			**256-QAM**			-	16-QAM OFDM	64-QAM OFDM	64-QAM	64-QAM WLAN	64-QAM	64-QAM
Data rate (Gb/s)	**6**	**9**	**18**	**4**	**6.4**	**8**	-	3.2	4.8	6	0.48	15	6
EVM (dB)	**-27.6**	**-26.8**	**-25**	**-31.3**	**-30.5**	**-30.5**	-	-22	-25	-26.6	-27.5	-25	-25
P_{out}@EVM (dBm)	**10.7**	**10.7**	**9.8**	**8.8**	**8.8**	**8.7**	-	-	6.7	7.2	10.97	11.7	5.9
PAE_{total}@EVM (%)	**21.4**	**21.5**	**18.4**	**16.2**	**16.7**	**16.3**	-	-	11	7.5[#]	17.3	5.75	2.3
PA core size (mm^2)	**0.29**						0.12	0.27	0.23	1.76	0.28	0.59	0.16
Topology	**Differential 2-stage Continuous-mode Harmonically-tuned**						Single-ended 1-stage Continuous-mode Class-F	Single-ended 1-stage Cascode Continuous-mode Class-AB	Single-ended 3-stage Class-AB	Single-ended 2-stage Doherty	Single-ended 1-stage 2-stacked Harmonically-tuned Class-AB	Single-ended 2-stage Doherty	Single-ended 2-stage Class-AB with Output Power Combiner

*PAE_{total} includes the DC power consumption of both driver and PA stage, **PAE_{PA} includes the DC power consumption of the output PA stage only, and
[#]Graphically estimated from reported figures

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Outline

- Introduction
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Conclusion

- A Continuous-mode harmonically tuned ultra-linear wideband PA is implemented in 0.13μm SiGe.
- Continuous-mode operation achieves high efficiency and wide bandwidth.
- First demonstration:
  - $P_{average}$=9.8dBm/PAE_{mod}=18.4% at 18Gb/s 64-QAM
  - $P_{average}$=8.7dBm/PAE_{mod}=16.3% at 8Gb/s 256-QAM

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Acknowledgement

- GlobalFoundries for chip fabrication.
- Members at Georgia Tech Electronics and Micro-System Lab (GEMS) for technical discussion.

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A Coupled Rotary-Traveling-Wave-Oscillator Based Subharmonic Receiver Front-end for 5G E-Band Backhaul Links in 28nm Bulk CMOS

Marco Vigilante[1,2], Prof. Patrick Reynaert[1]

[1]KU Leuven, ESAT-MICAS, Belgium
[2]Now with Qualcomm, San Diego, CA

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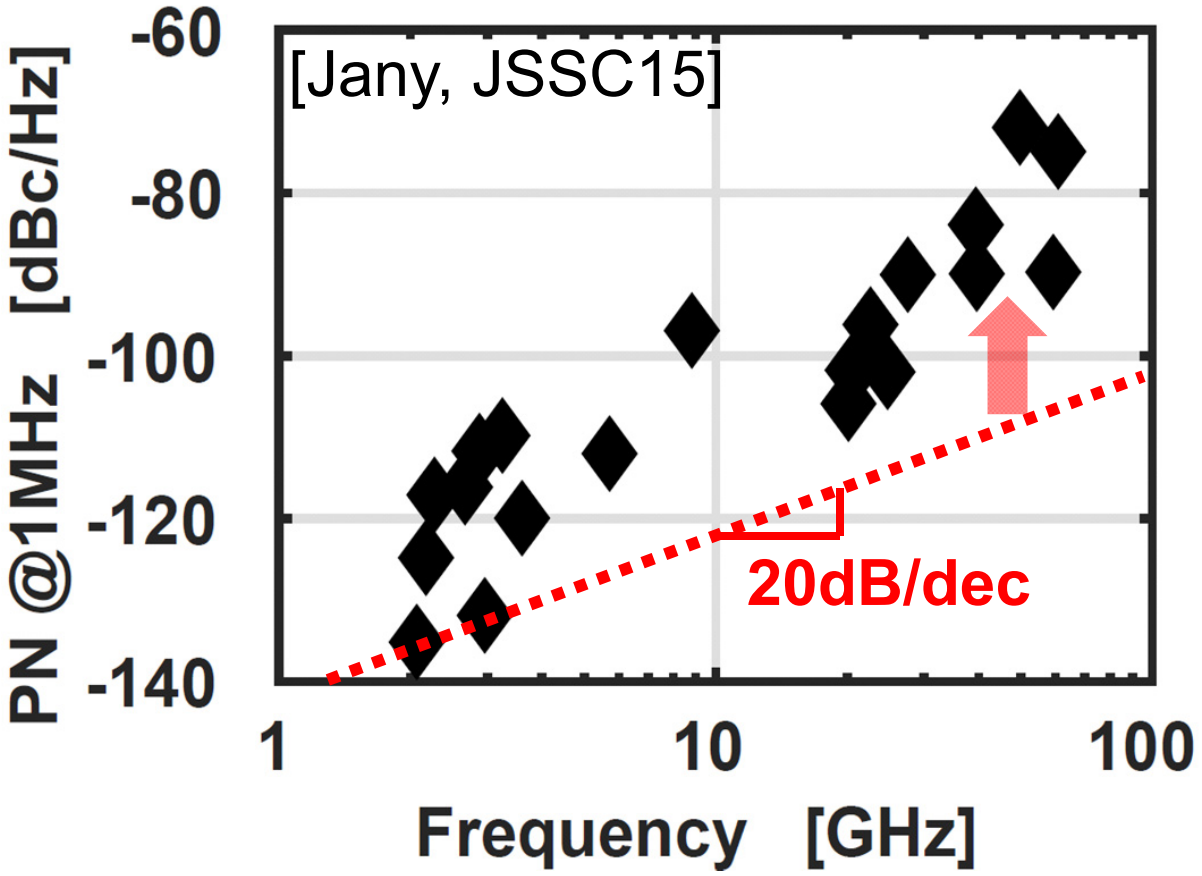
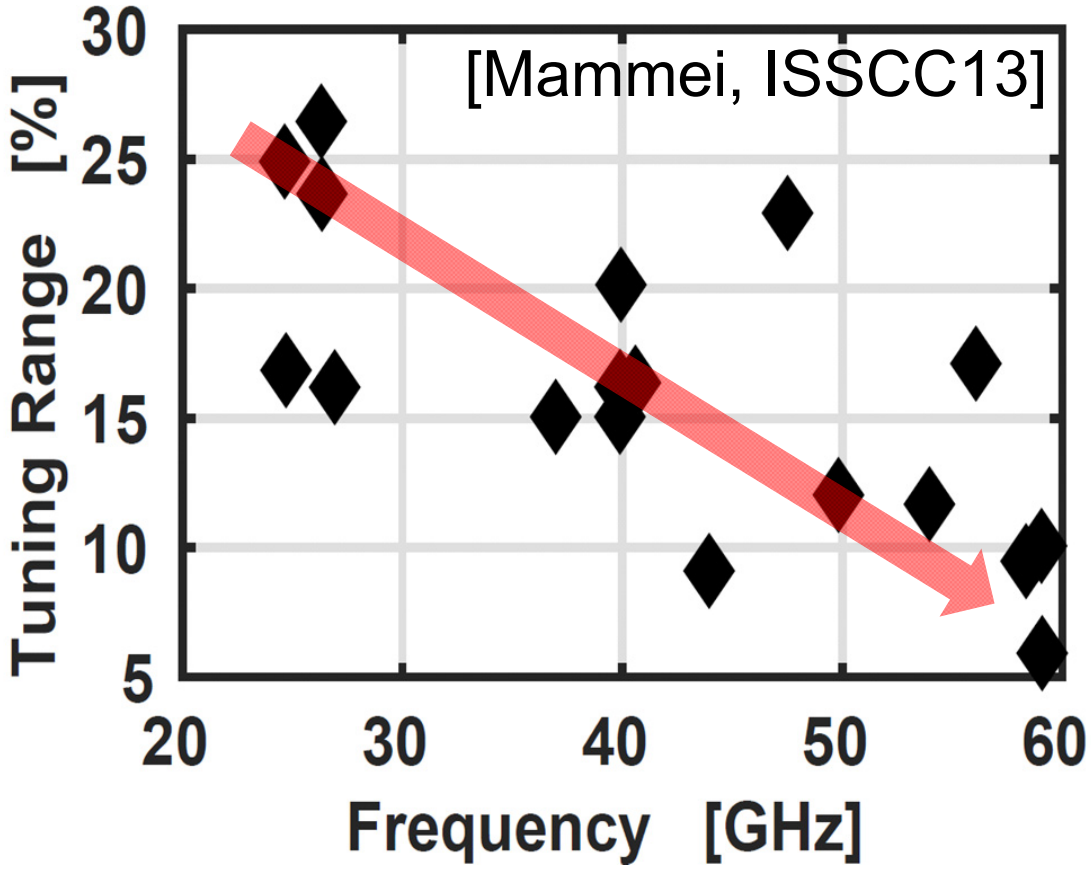
Challenges @mm-Wave





- Phase noise & tuning range drastically degrade with frequency
- Deep-scaled technologies do not help!

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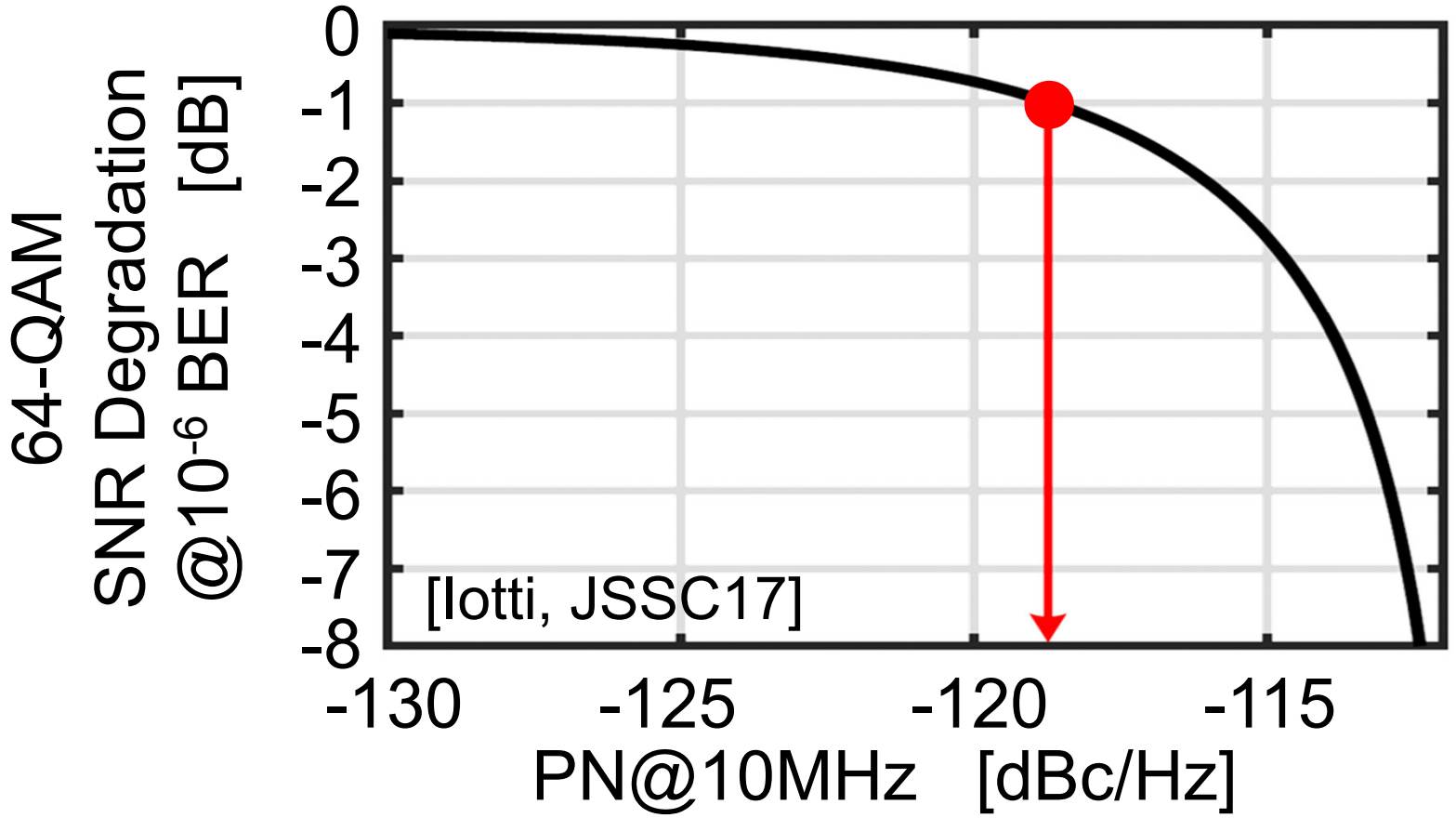
Local oscillator requirements



- $PN_{@10MHz}$=-119dBc/Hz degrades SNR <1dB
- In combination with >19% TR & I/Q phases!

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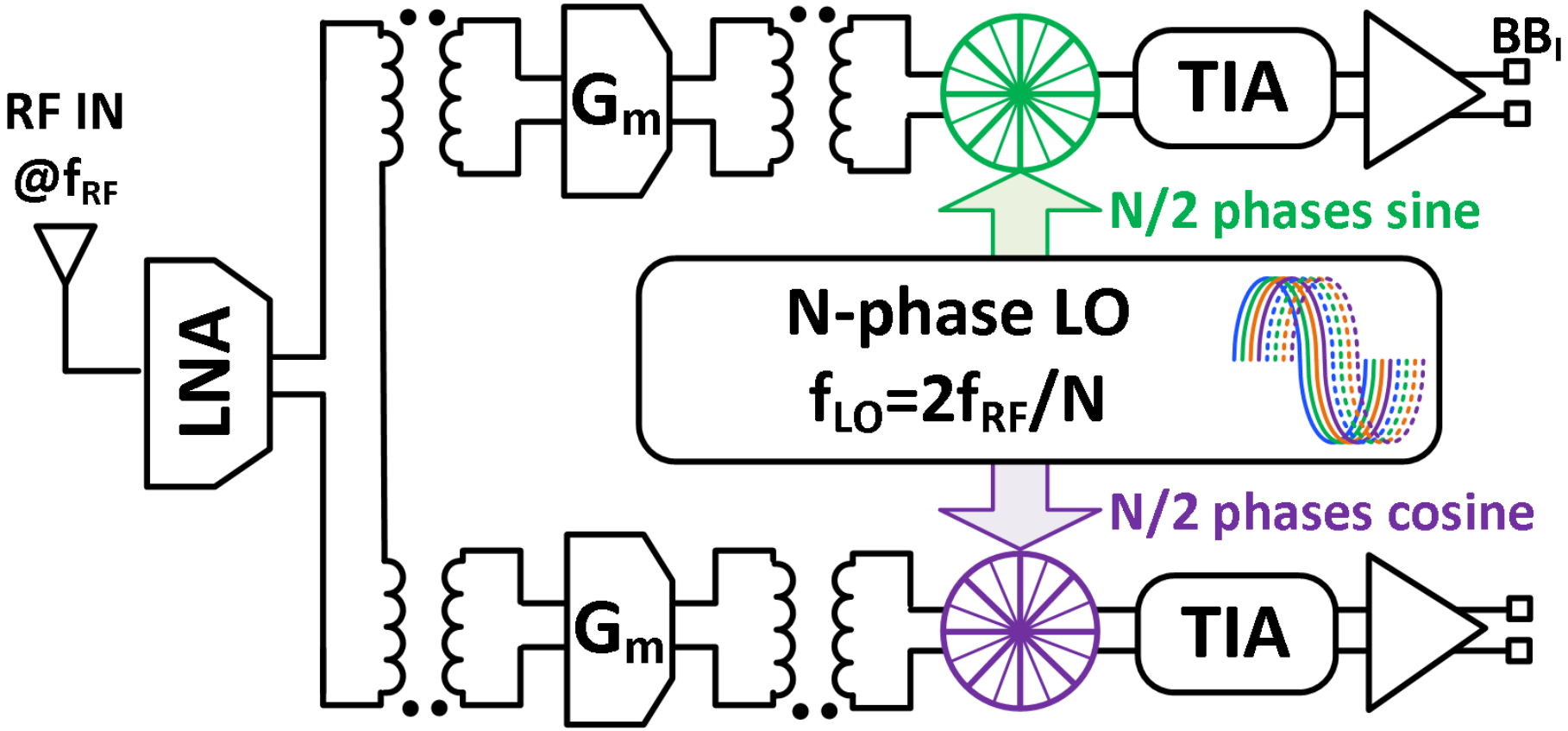
Subharmonic receiver requirements



- Target noise figure <10dB (1km link distance)
- >15GHz BW_{-3dB}
- Current mode operation for low V_{DD}

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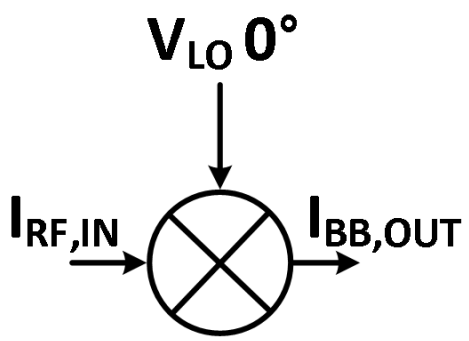
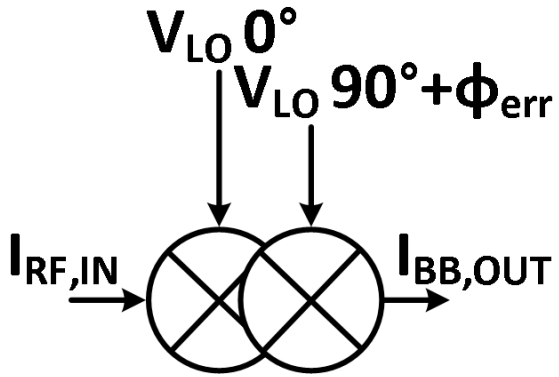
How far can we push N?

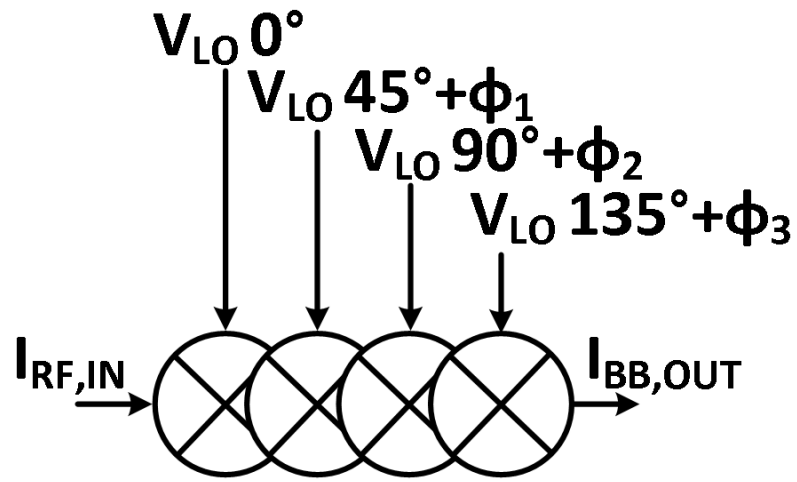
N/2=1, $f_{LO}=f_{RF}$
CG=2/π



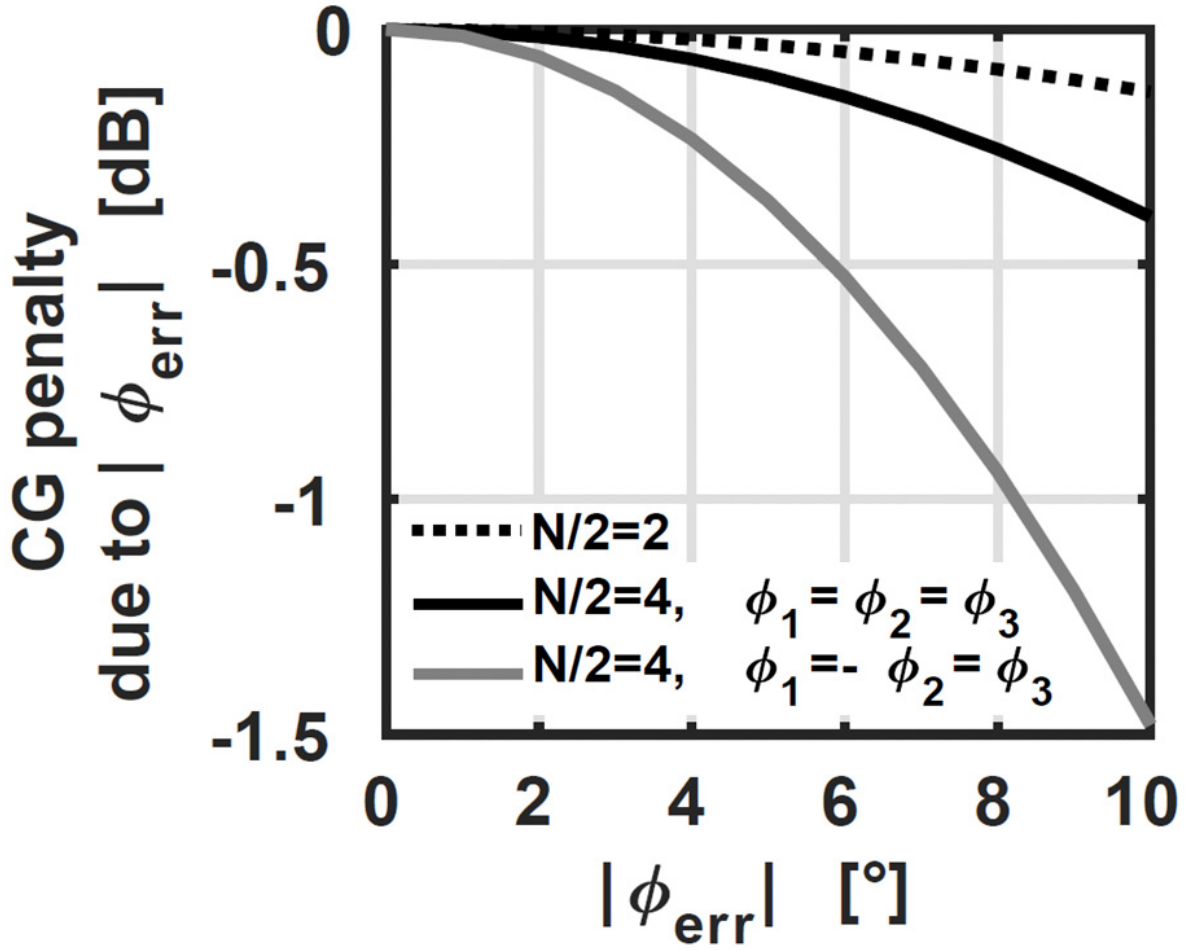
N/2=2, $f_{LO}=f_{RF}/2$
CG≈2/π·cos(ϕ_{err})



N/2=4, $f_{LO}=f_{RF}/4$



(With lossless switches)



$|\Phi_{err}|=8°$ ➔ <1dB CG degradation

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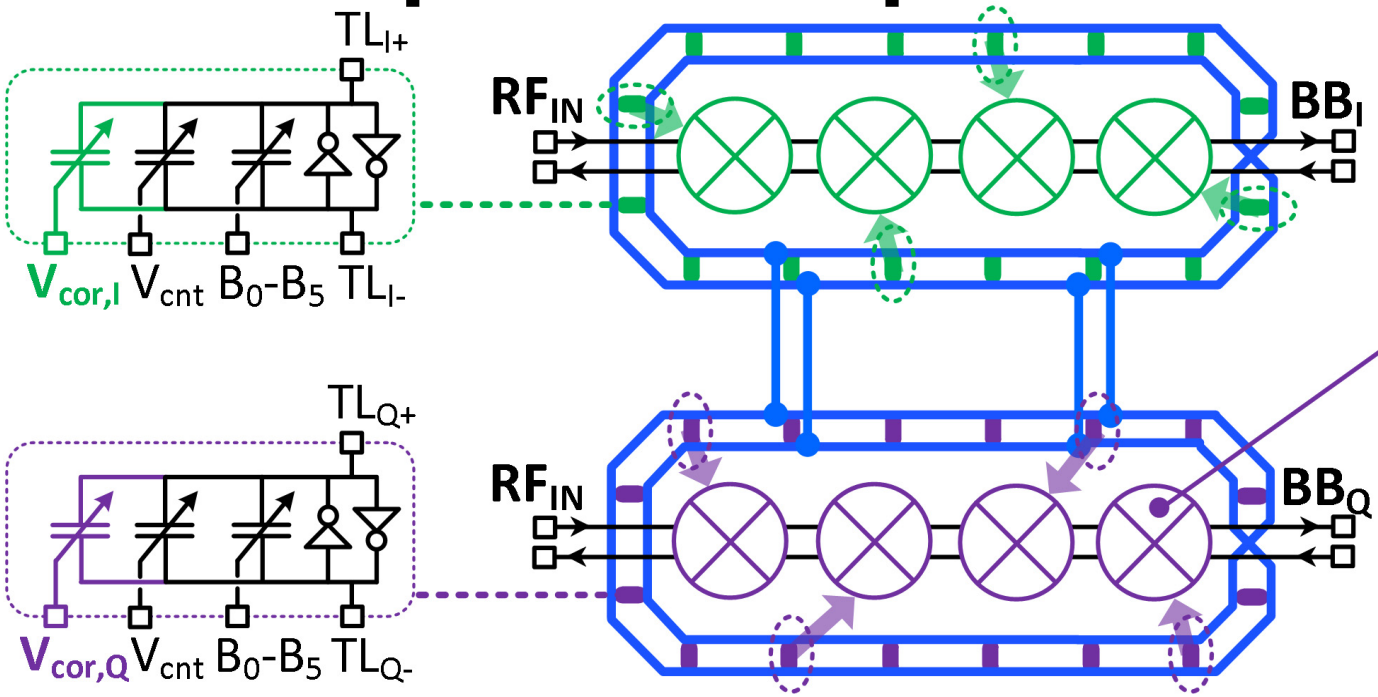
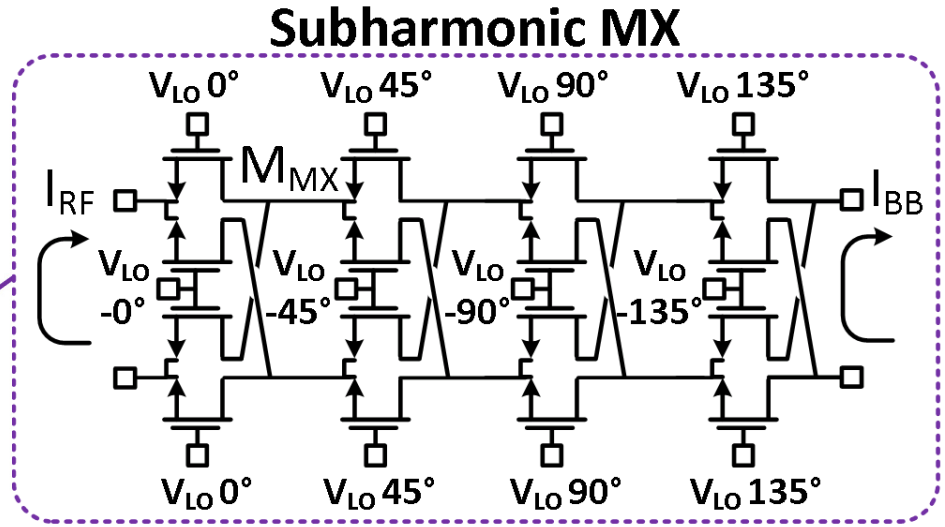
Proposed coupled-RTWO-based SHMXs





- N=8 ➔ $f_{LO}=f_{RF}/4$ (≈20GHz)
  - ✓ No image problem
  - ✓ ↓ LO feedthrough
  - ✓ No PA pulling
  - ✓ Superior PN, TR & FOM
  - ✓ No LO buffers needed!
- Coupled RTWOs
  - ✓ 3dB lower PN, same FOM
  - ✓ Pseudo square-wave
  - ✓ ↑CG SHMX, ↓4th harmonic (↓LOFT)
  - ✓ Simple I/Q correction
  - ✓ Elegant layout solution

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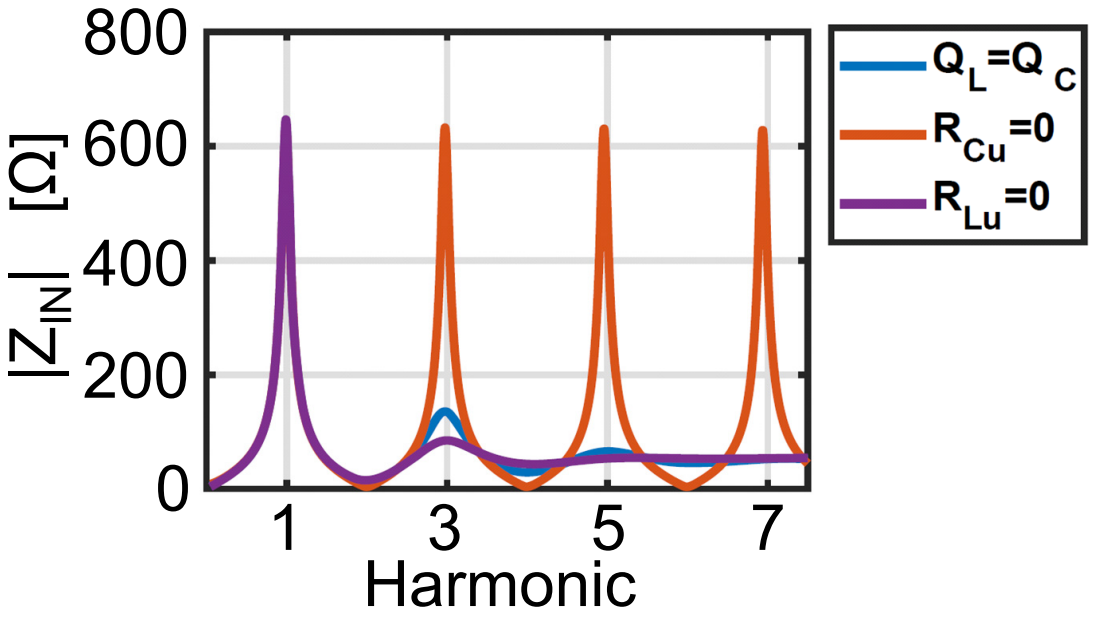
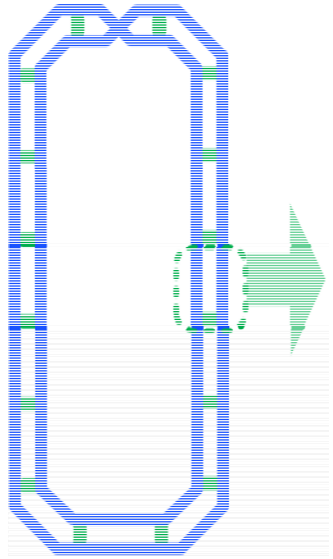
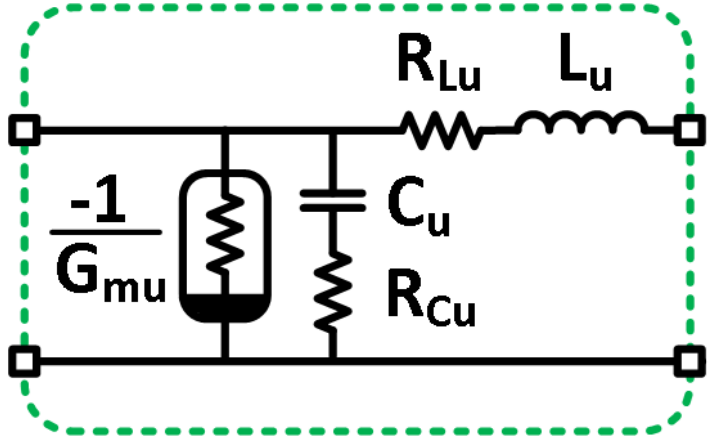
More on RTWO design







[Moroni, JSSC14]
[Garampazzi, JSSC14]

$$PN(\Delta f) \approx 10log_{10}\left[\frac{K_B T(1+\gamma)}{2Q^2 \boldsymbol{P_{RF}}}\left(\frac{f_o}{\Delta f}\right)^2\right]$$

⇐ **Increase P_{RF}**

$$\boldsymbol{P_{RF}} = \frac{(\mu_V V_{DD})^2}{\boldsymbol{R_T}} = \frac{(\mu_V V_{DD})^2 \pi}{Q\boldsymbol{Z_o}} \approx \frac{(\mu_V V_{DD})^2 \pi}{Q}\sqrt{\frac{\boldsymbol{C_u}}{\boldsymbol{L_u}}}$$

⇐ **Decrease Z_o**

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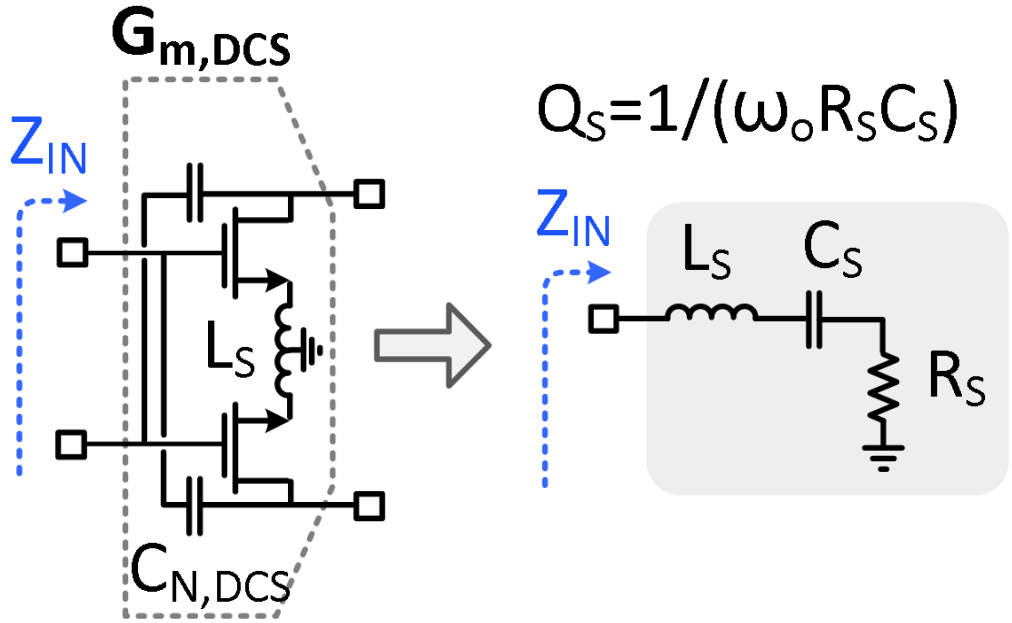
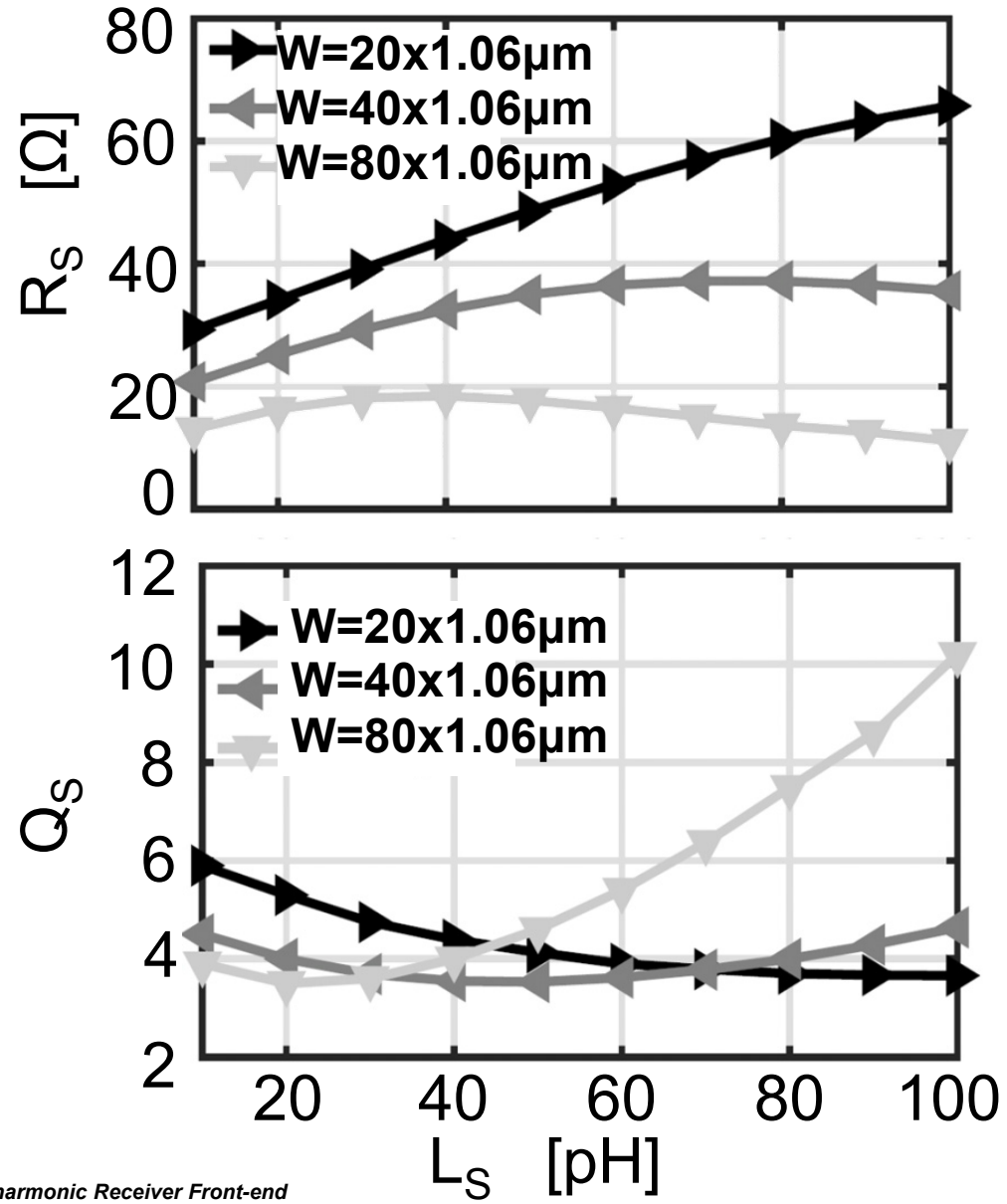
Broadband LNA design in the E-Band





- Fixed bias for maximum $f_t\, g_m/I_D$
- $Q_{S,min}$ independent from L_S and W
  - ☺ Lower L_S ➔ higher G_m
  - ☹ Larger W ➔ higher P_{DC}

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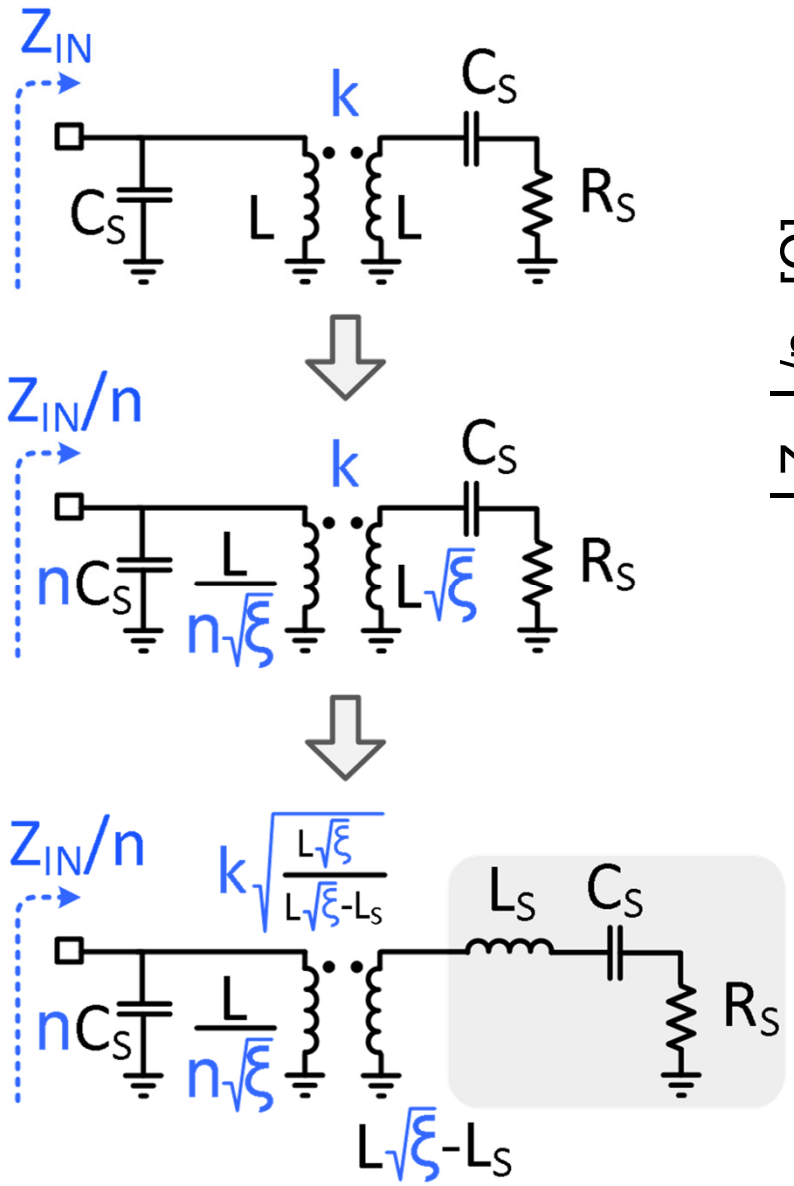
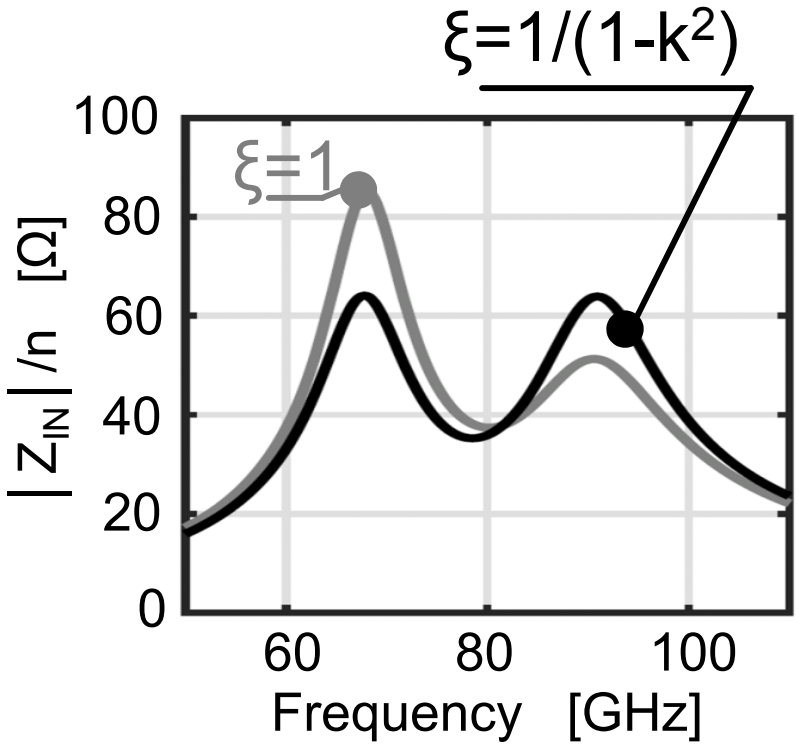
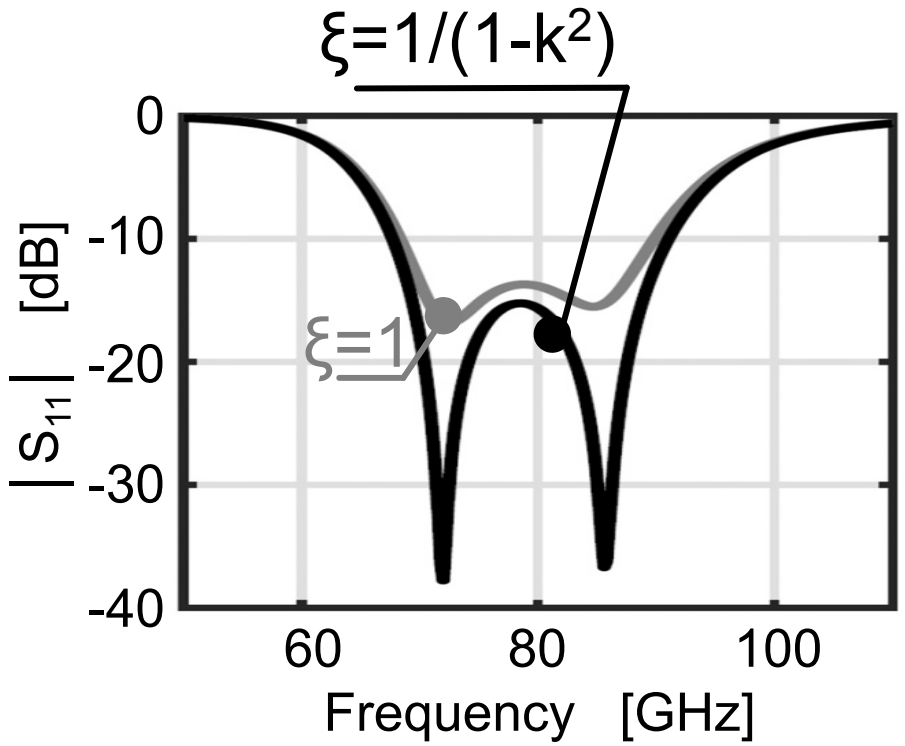
Broadband LNA design in the E-Band







$$|k| = \frac{\omega_H^2 - \omega_L^2}{\omega_H^2 + \omega_L^2}$$

$$L = \frac{1}{\omega_o^2 C_S (1 - k^2)}$$

$$n = \frac{1}{\omega_o^2 (1 - k^2) C_S^2 R_S 50\Omega}$$

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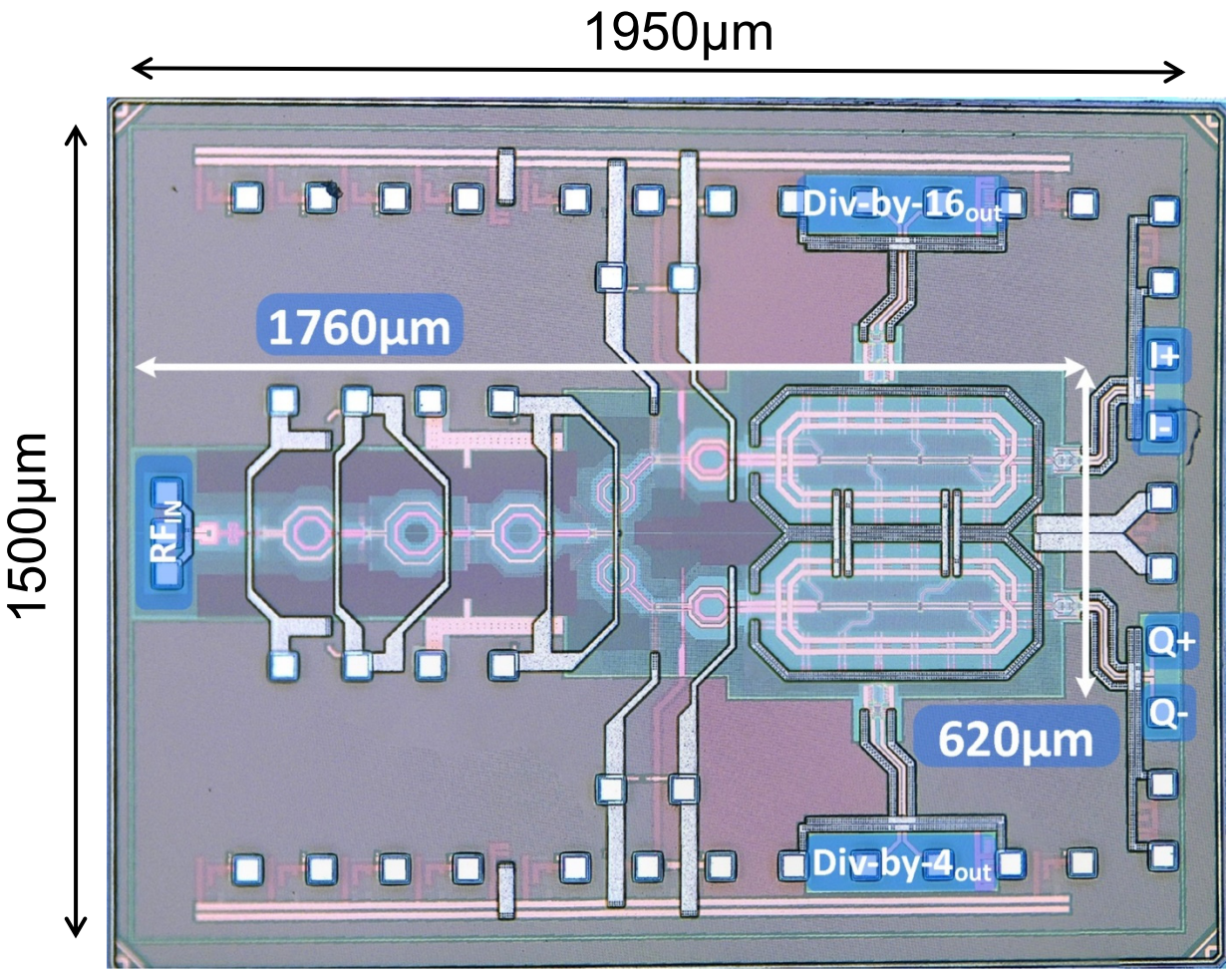
Chip Micrograph



- TSMC 28nm-bulk-CMOS
- No ultra-thick RF top metal
- Core area 1760µm x 620µm

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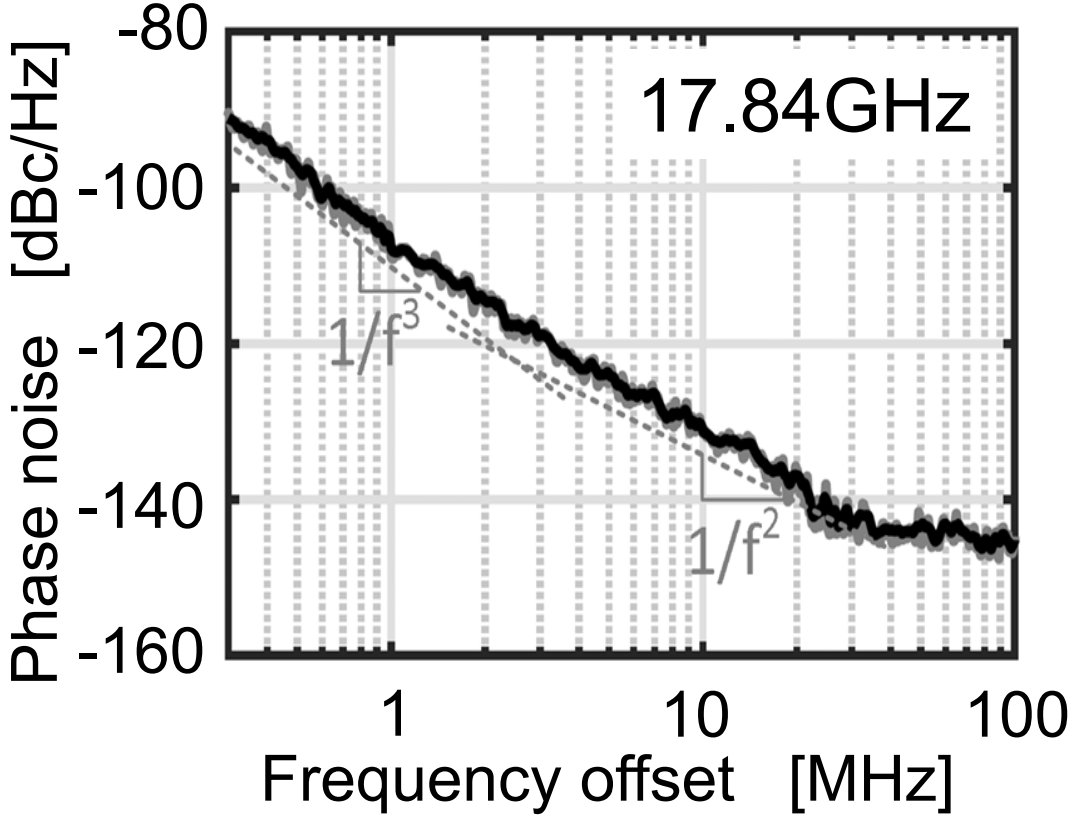
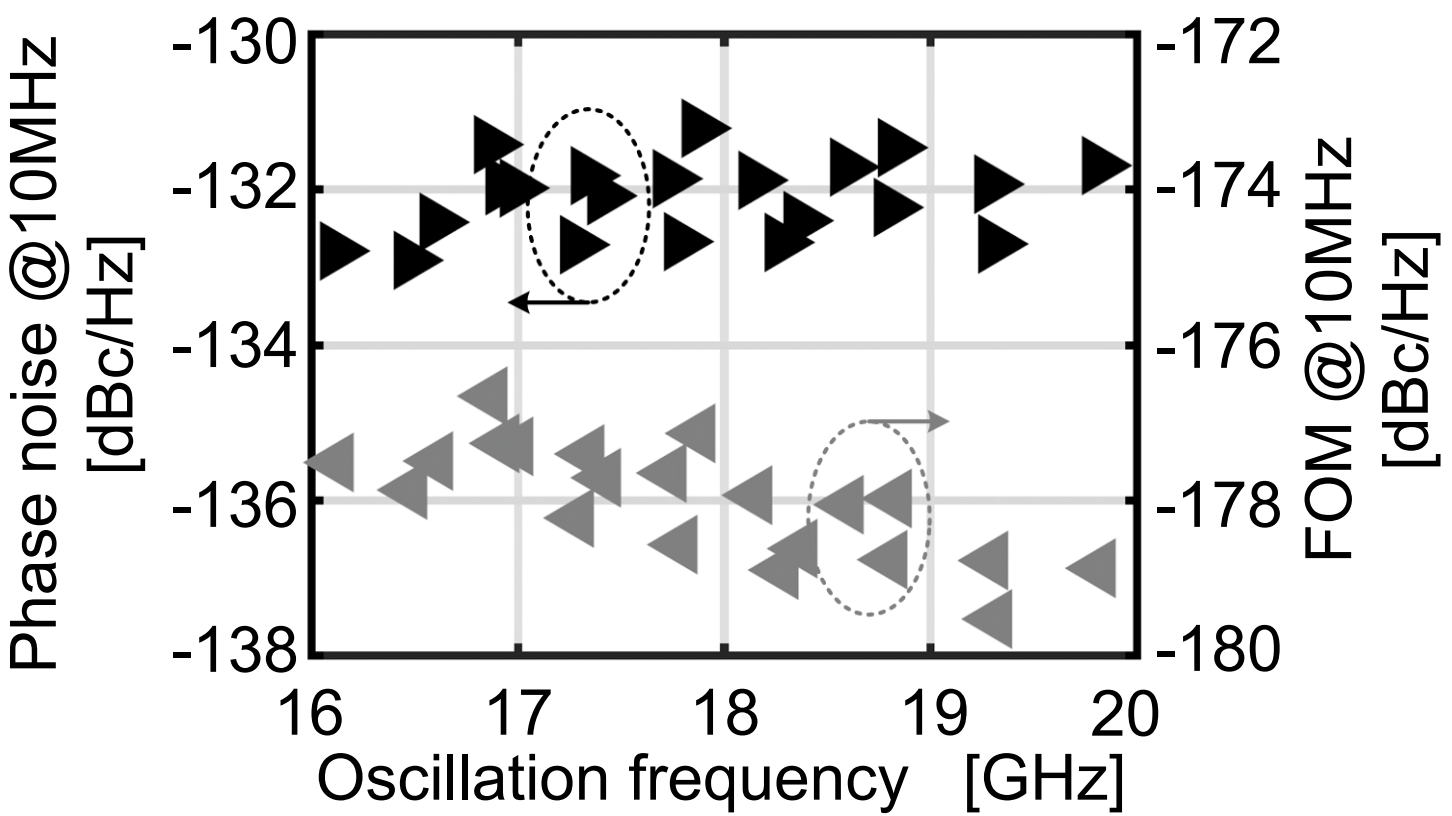
Coupled RTWOs measurements





- Benefited by the subharmonic architecture $f_{LO}=f_{RF}/4$
- 20.5% tuning range (400MHz minimum overlap)
- PN from -131.2 to -132.8dBc/Hz (1.6dB variation)
- FOM from -176.7 to -179.5dBc/Hz

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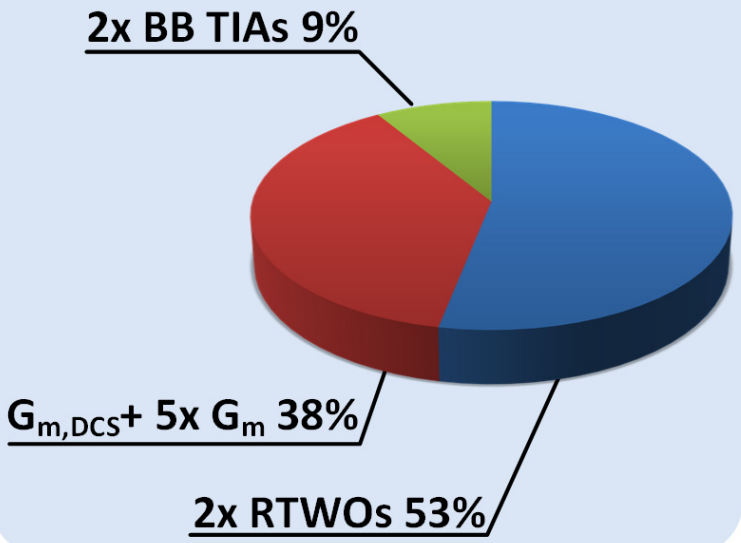
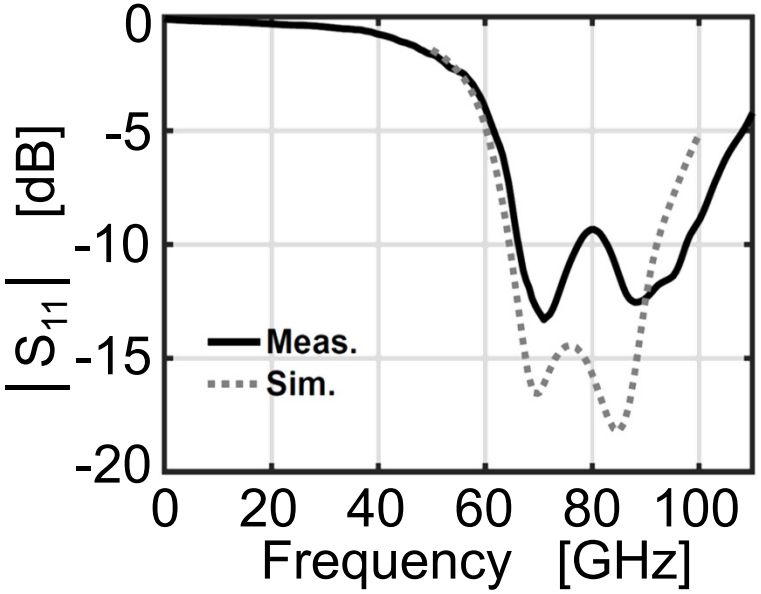
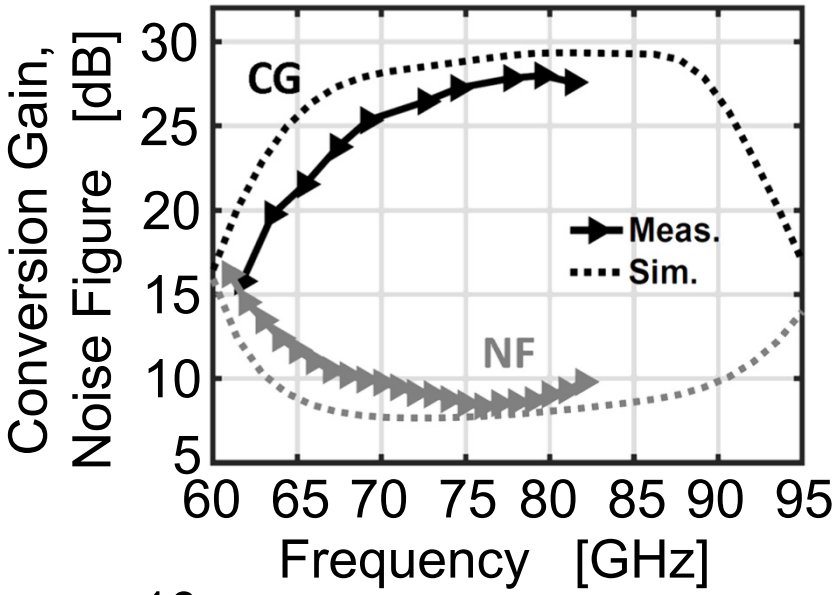
SHRX measurements

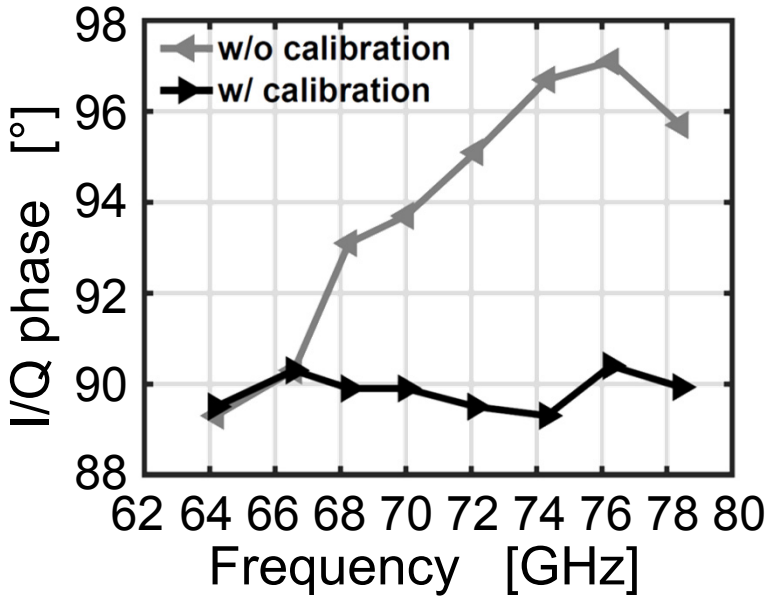
Power breakdown between the blocks @lowest frequency

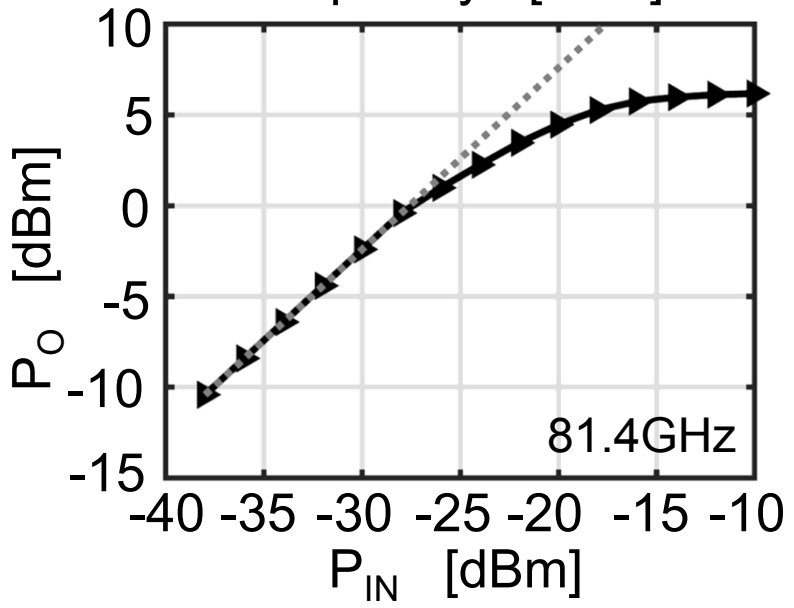


No LO buffer is needed!









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E-Band Frequency Generation State-of-the-art

Ref.	Tech.	Topology	Freq. [GHz]	TR [%]	P_{DC} [mW]	PN @10MHz [dBc/Hz]	FOM [dBc/Hz]	I/Q?
This work	**28nm CMOS**	**2 Coupled RTWOs (eq. @4f_o)**	**16.1-19.8 (64.4-79.2)**	**20.5**	**87.6-75**	**-131.2/-132.8 (-119.1/-120.7)**	**-176.7/-179.5**	**YES**
Guermandi JSSC17 [2]	28nm CMOS	VCO + SH-QILO5	78-87	11	100	-116	-174.3	YES
Vigilante TMTT16	28nm CMOS	QVCO	71.4-76.1 85.6-90.7	6.4 5.8	35.6*	-114.2/-117.7 -107/-110	-176.3/-179.4* -170.2/-173.4*	YES
Huang ISSCC15	65nm CMOS	I/Q ILFM3	70.5-85.5	19.2	47.3*	-111.7/-115.8#	-173.5/-176.3*	YES
Iotti JSSC17 [1]	55nm SiGe	4 Coupled VCOs + Quadrupler	69.6-80.9+	15	50*	-126/-128.2#	-187.2/-188.2*	NO
Fujibayashi JSSC17 [4]	0.13µm SiGe	VCO + Quadrupler + Hibrid Coupler	74-82.4	12	NA	-119/-120#	NA	YES
Levinger TMTT16 [5]	0.13µm SiGe	VCO + Quadrupler + Divide-by-2 (eq. @9/2 f_o)	15.6-19.3 (70.1-86.7)	21.2	405^	-133 (-120)	-171.5^	YES

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E-Band RX State-of-the-art comparison

Reference	**This work**	Guermandi JSSC17 [2]	Guermandi ISSCC15 [3]	Fujibayashi JSSC17 [4]	Levinger TMTT16 [5]	
Technology	**28nm CMOS**	28nm CMOS	28nm CMOS	0.13µm SiGe	0.13µm SiGe	
Architecture	**Subharmonic Direct Conversion 2 Coupled RTWOs**	Direct Conversion VCO + SH-QILO5	Direct Conversion SH-QILO5	Direct Conversion VCO + Quadrupler + Hybrid Coupler	Sliding-IF VCO + Quadrupler + Divide-by-2	
f_c [GHz]	**75.1**	82.5	79	78.5	73	83
Gain [dB]	**28**	31	35	15	70	70
RF-BW	**12.5GHz* (16.7%*)**	9GHz (10.9%)	8GHz (10.1%)	7GHz (9%)	5GHz (6.9%)	5GHz (6%)
NF [dB]	**8.3-10**	12#	6.2-7	7-8	6-7	6-7
ICP_{1dB} [dBm]	**-25**	-28	-32.5	1	-19.6+	-21.6+
RX P_{DC} [mW]	**77.3**	68	59	197.5	222	222
On-chip LO?	**YES**	YES	NO	YES	YES	
LO freq. [GHz]	**16.1-19.8**	78-87	NA	74-82.4	15.6-19.3	
LO TR [%]	**20.5**	11	NA	12	21.2	
LO P_{DC} [mW]	**87.6-75**	100	NA	NA	405^	
PN @10MHz [dBc/Hz]	**-131.2/-132.8 (-119.1/-120.7)v**	-116	NA	-119/-120**	-133 (-120)v	
LO FOM [dBc/Hz]	**-176.7/-179.5**	-174.3	NA	NA	-171.5^	

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Conclusion

- ✓ First Coupled-RTWO-Based Subharmonic Receiver for high-capacity 5G E-Band backhaul links
  - ✓ N=8 differential phases are generated by distributed oscillators
  - ✓ A simple I/Q correction circuit is proposed
  - ✓ Current mode design allows low V_{DD} operation
- ✓ SHRX implemented in 28nm CMOS
  - ✓ Record phase noise, tuning range and FOM
  - ✓ State-of-the-art RF BW_{-3dB} and noise figure
  - ✓ Excellent I/Q phase accuracy

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Acknowledgments

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Analog Devices Inc, Limerick, Ireland.

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A 12mW 70-to-100GHz Mixer-First Receiver Front-End for mm-Wave Massive-MIMO Arrays in 28nm CMOS

L. Iotti, G. LaCaille, A.M. Niknejad
University of California, Berkeley

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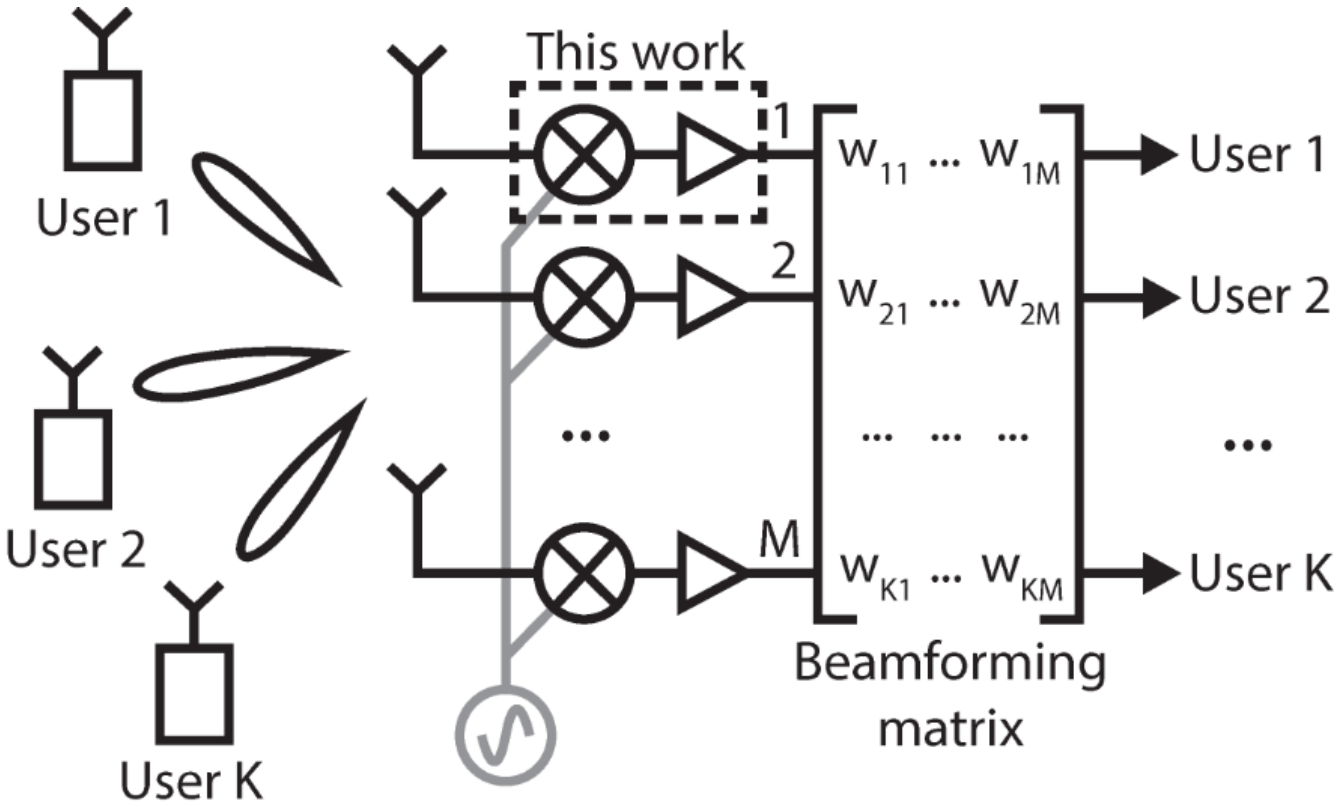
mm-Wave Massive MIMO Base Station



- **Why (Multi-User) MIMO?**
  - **Spectral efficiency enhancement through spatial multiplexing**
  - K user data streams extracted from array of M antennas
- **Why Massive (M>>K)?**
  - **Linear beamforming achieves nearly-optimal performance**
- **Why mm-wave?**
  - **Wide BW and compact array**
  - Focus on E-Band: 71-76 GHz, 81-86 GHz, 92-95 GHz

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RX Design for Massive MIMO

- **Noise figure can be relaxed**
  - $SNR_{OUT} = SNR_{ANTENNA} + [NF_{RX} - 10\log_{10}(M)]$
- **Low power and small footprint are key**
- **Good linearity is required**
  - RF/LO signal combining not practical (MxK mmW phase shifters required)
  - Antenna streams combined at baseband: **spatial filtering after front-end**
  - RX has to cope with in-band interferers

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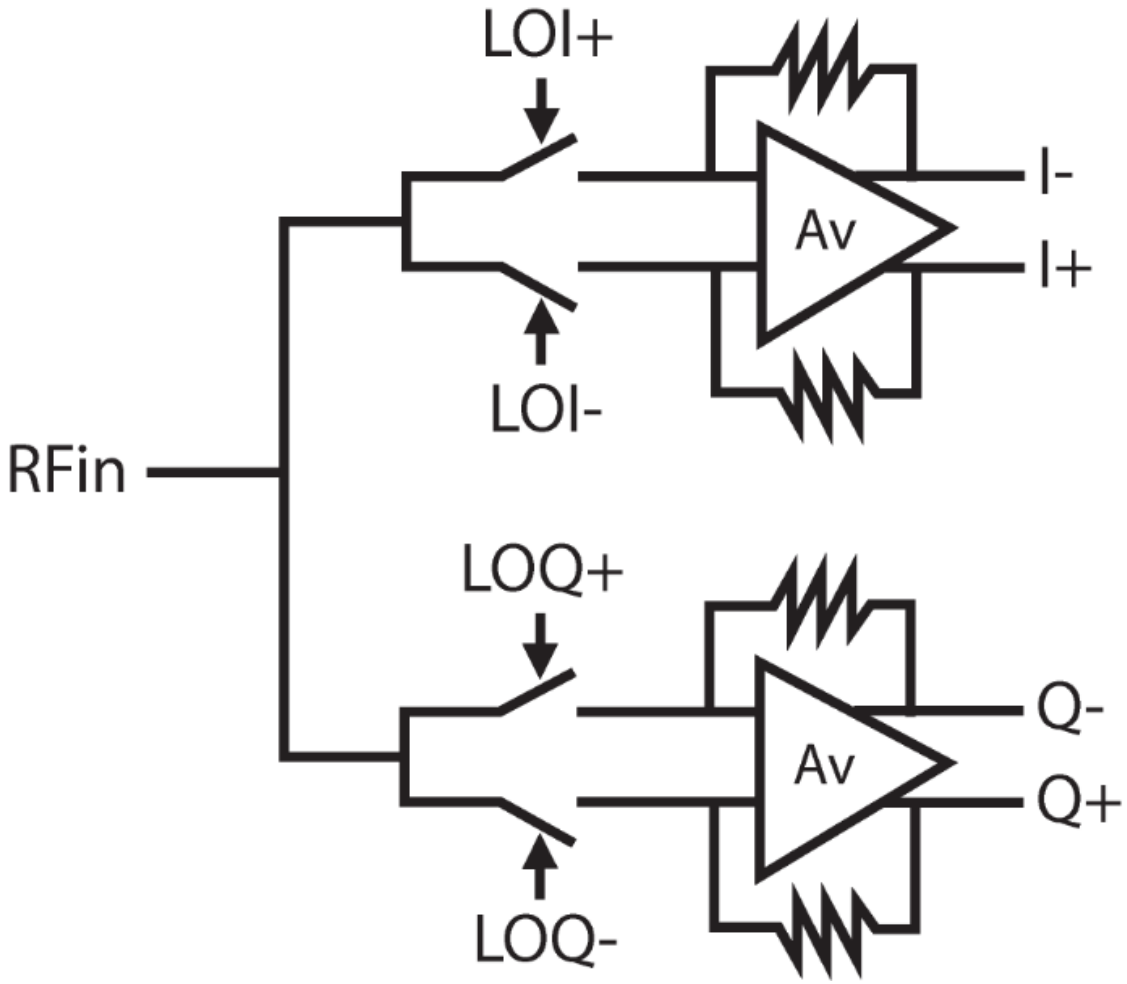
Conventional Mixer-First RX



- ✓ Minimum # of stages at mmW
- ✓ Compact, low power
- ✓ Good linearity
- ✓ Wideband

- x Ideal-switch operation requires large switches
- x High LO power

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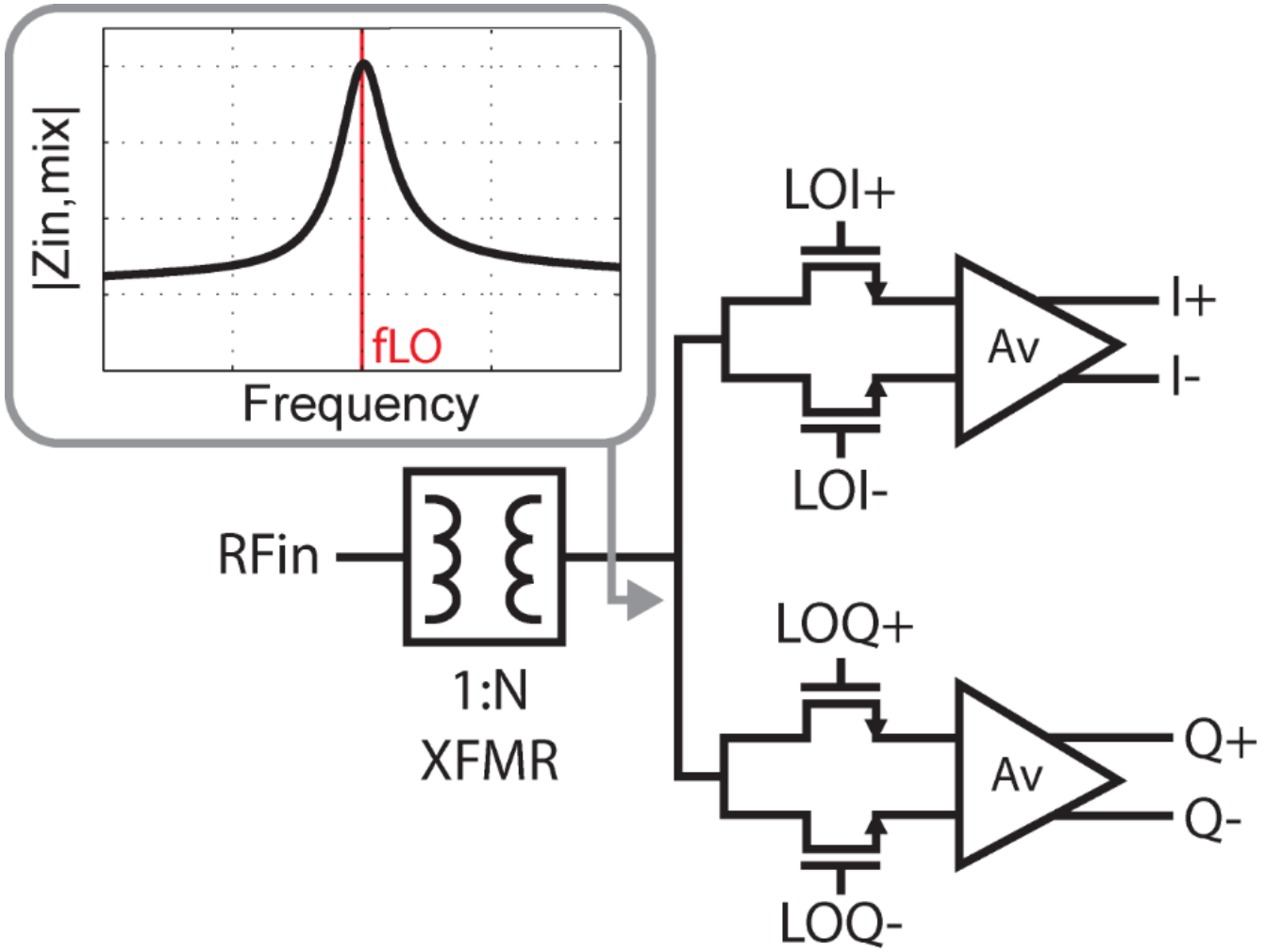
High-Zin Mixer-First RX



- **Small switches**
- **Open loop baseband amp**
- **XFMR match to antenna**

✓ Lower LO power needed

✓ XFMR passive voltage gain compensates higher mixer noise

x High-turn-ratio XFMR not feasible at mmW

x Narrowband operation

First implementation: 5GHz WLAN RX [Homayoun, JSSC 2015]

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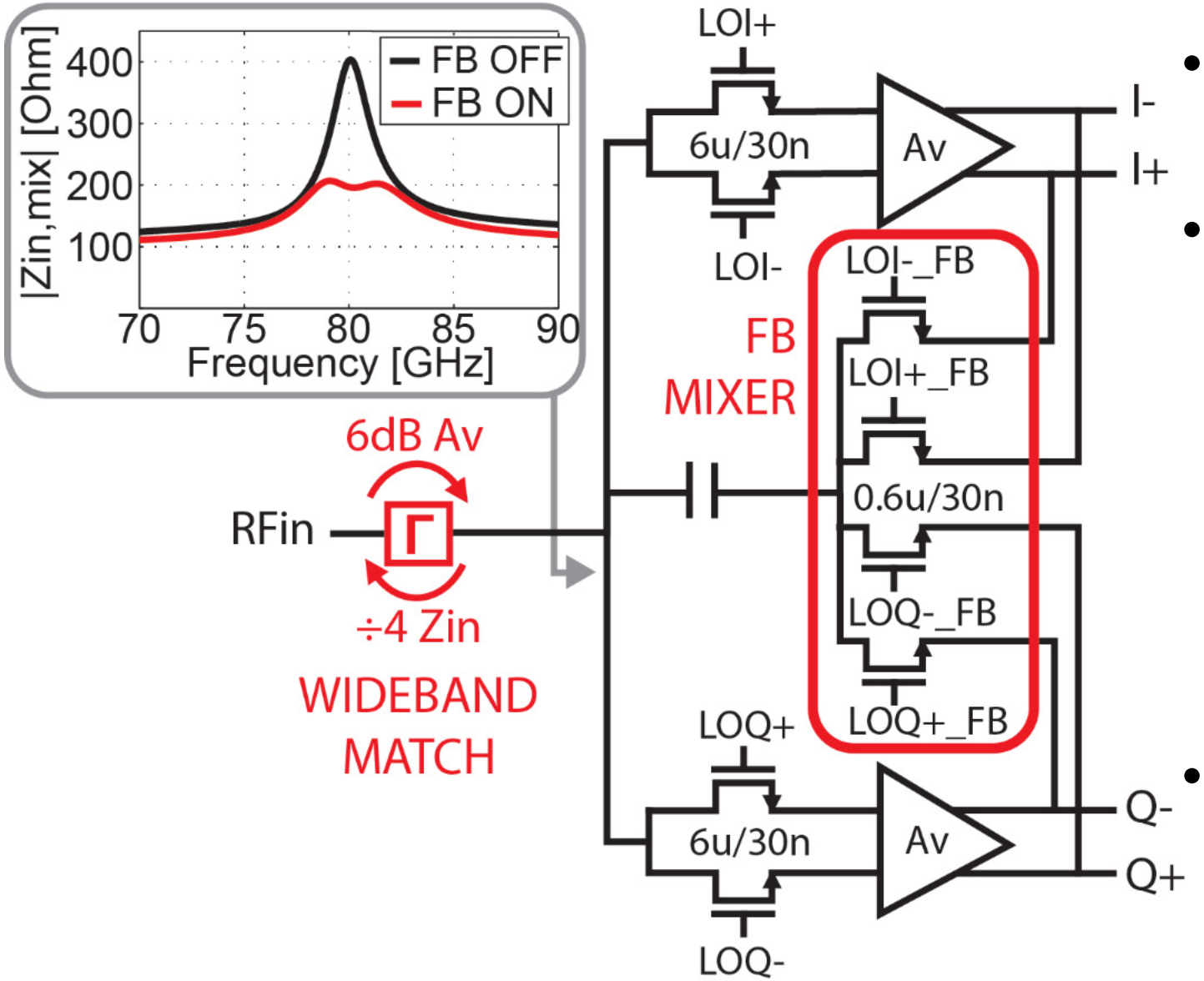
Proposed Mixer-First RX



- Small mixer switches
  - |Zmix|=400Ω
- **Frequency-translational feedback** provides 50% Zin reduction
  - BB amp is part of the loop
  - W_FBMIX = 0.1 W_MIX
  - 10% capacitance overhead
  - <1dB NF penalty
- **Wideband matching network** provides 50Ω input matching

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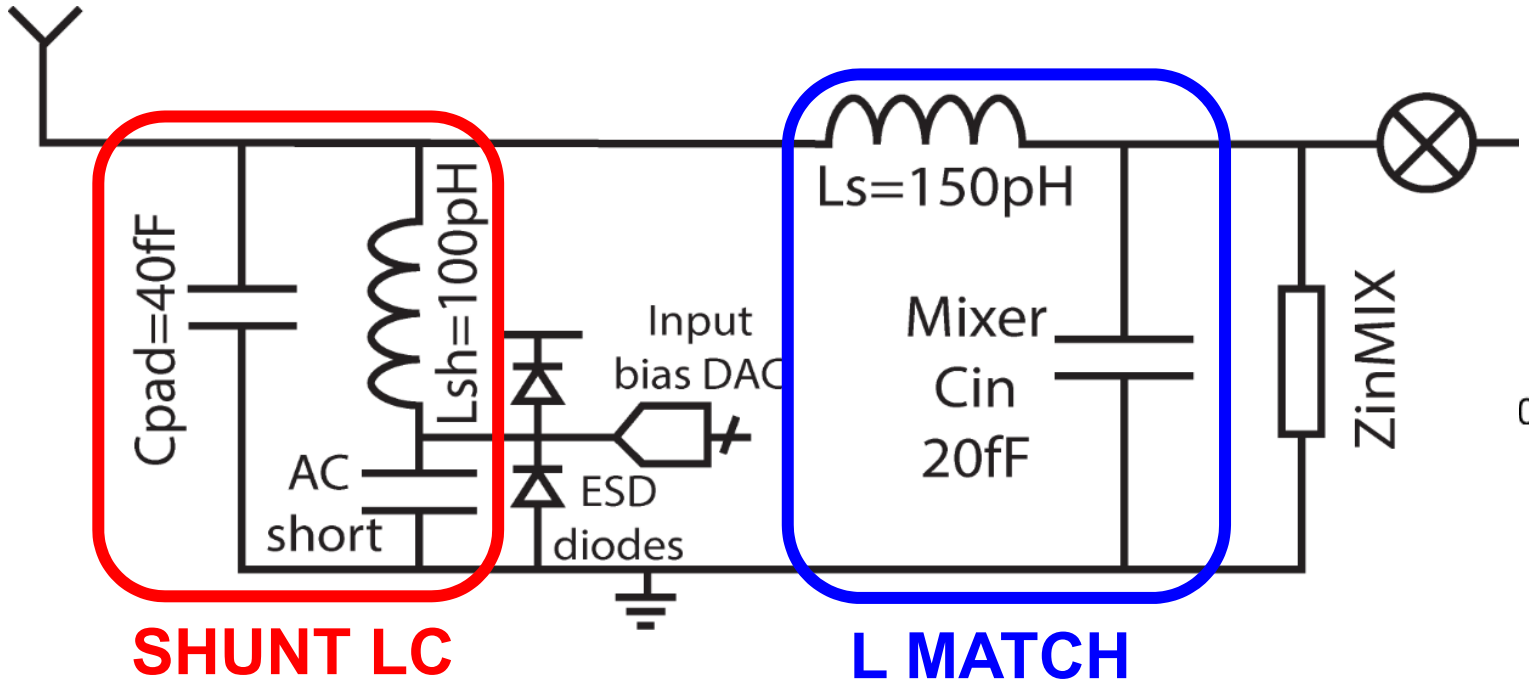
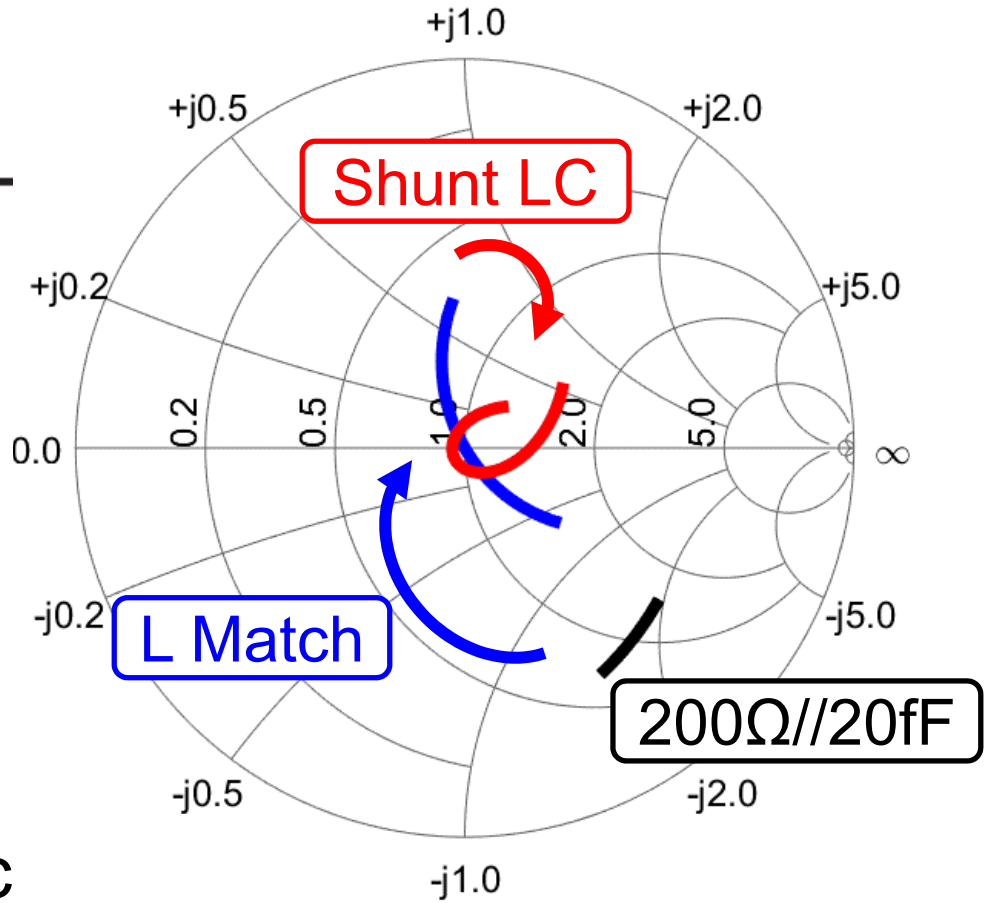
Wideband Matching Network





- **L-Match** translates impedance to 50Ω @ fc
- **Shunt LC resonator** neutralizes pad cap and provides wideband match
  - ESD protection and input bias included

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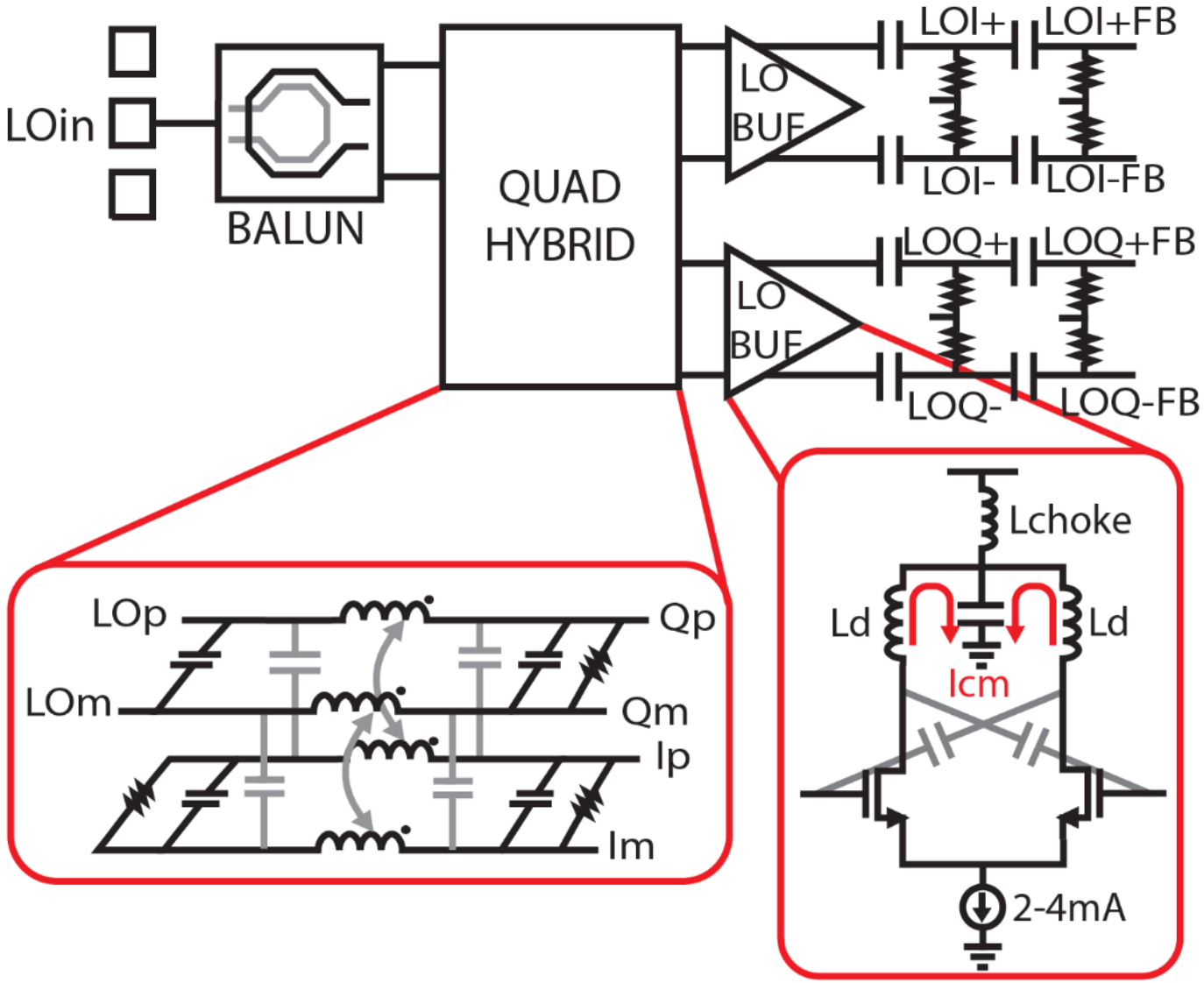
LO Generation



- **Low-power LO buffers:**
  - 7dB max gain
  - 300mV,SE,0pk out swing
  - LC series trap for CM rejection
- **Differential XFMR-coupled quad hybrid** generates I/Q LO
- LO tone generated off-chip

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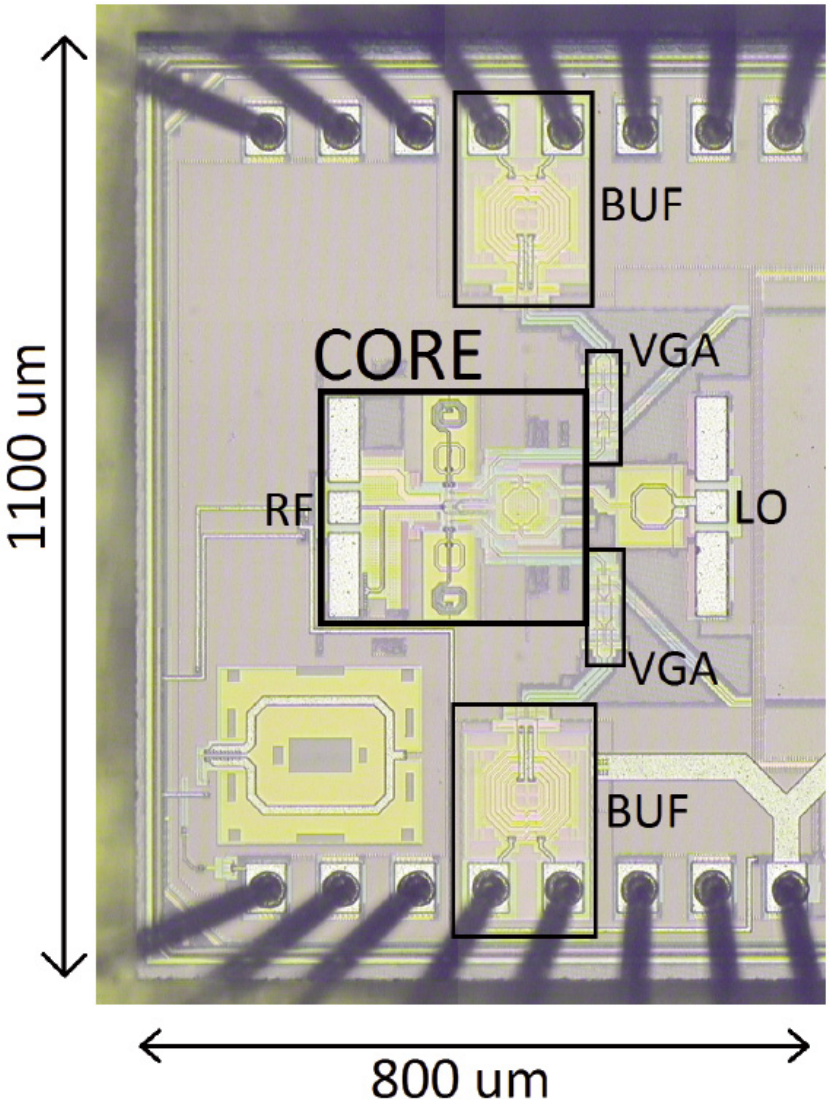
Chip Prototype



- CMOS 28nm tech (no UTM)
- 1V supply
- Core area 320um x 270um
- VGA + Out Buf for measurements

- Power consumption:
  - **2x 2 mW BB amps**
  - **2x 2-4 mW LO buffers**

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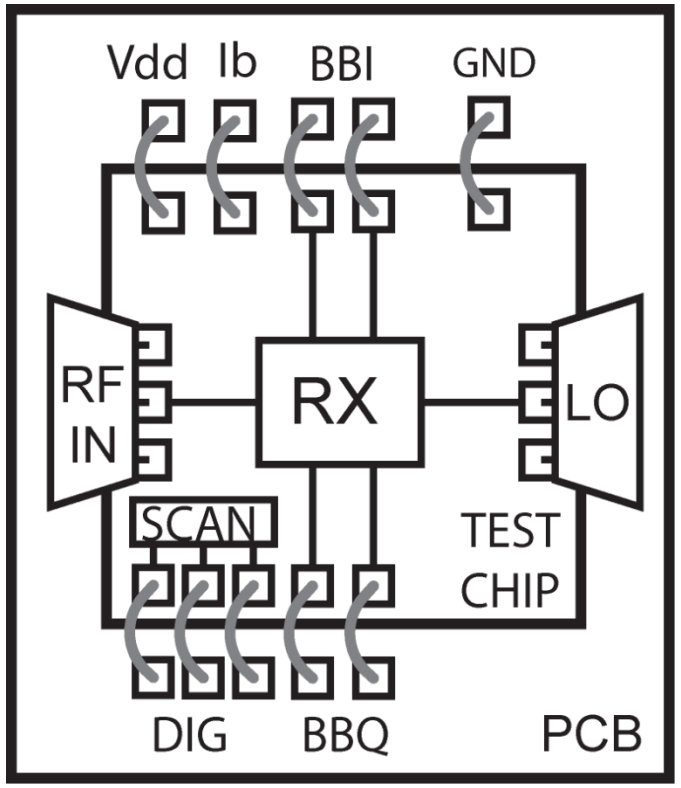
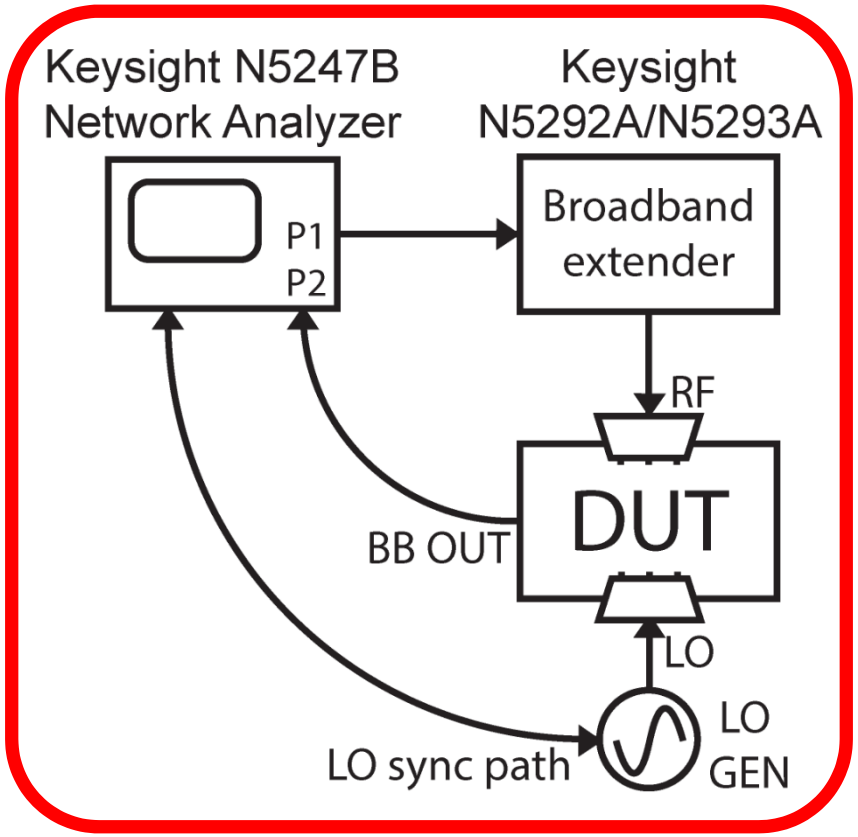
Measurement Setup

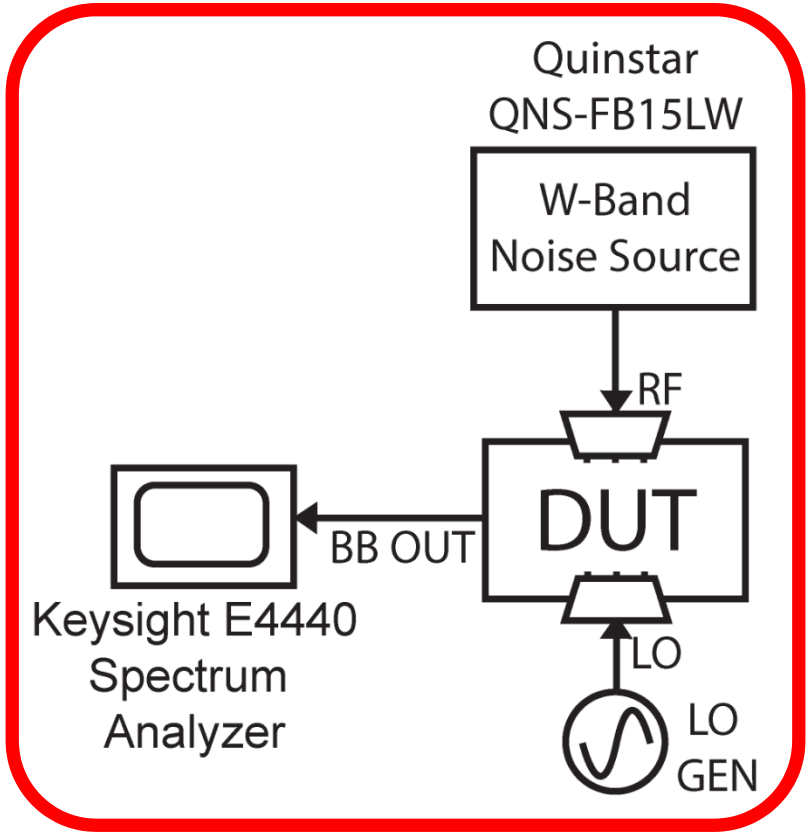
Test chip interface



S-Parameter meas setup



NF meas setup (Y factor)



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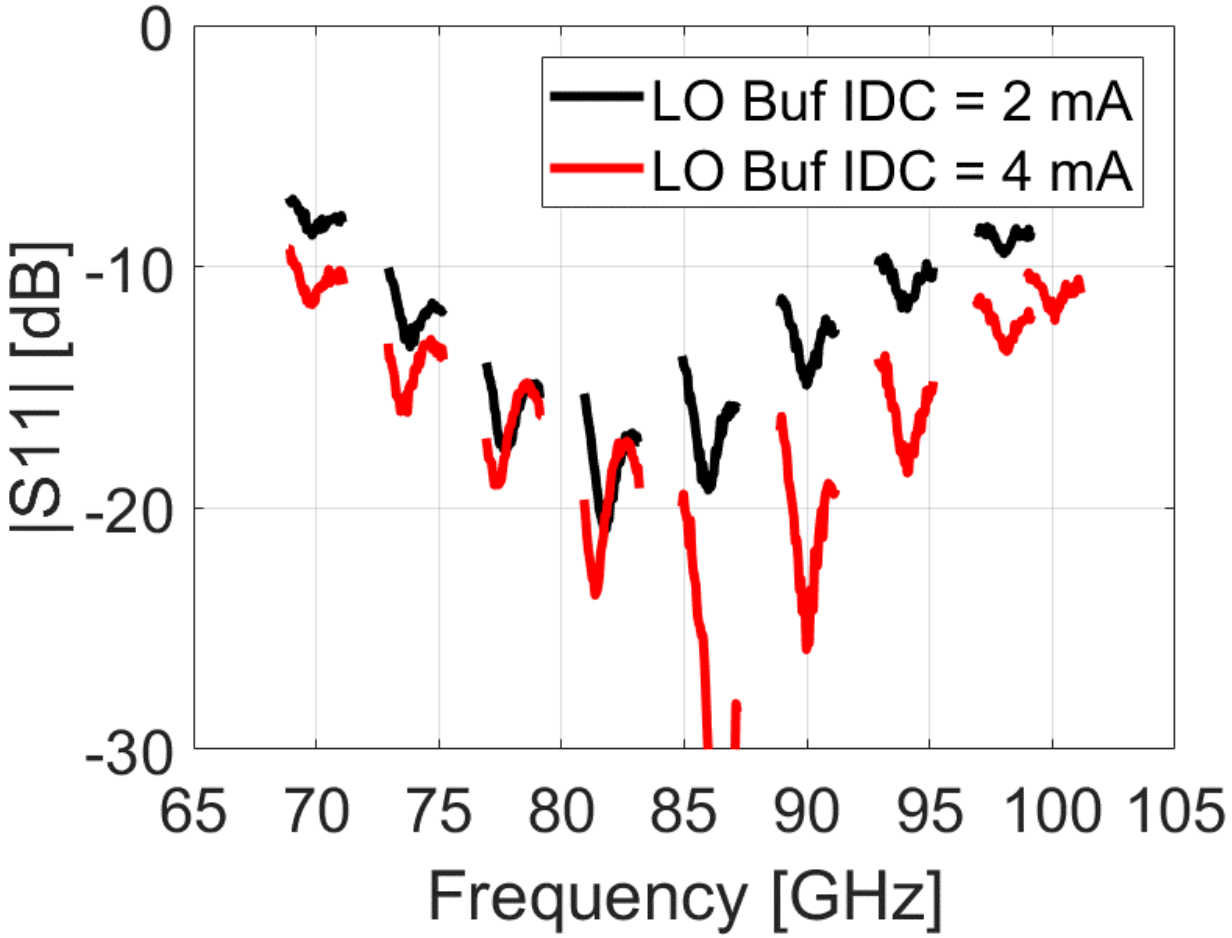
Input Matching Measurements



RF signal swept ±1GHz around fLO

S11<-10dB over 70-100GHz
35% fractional BW

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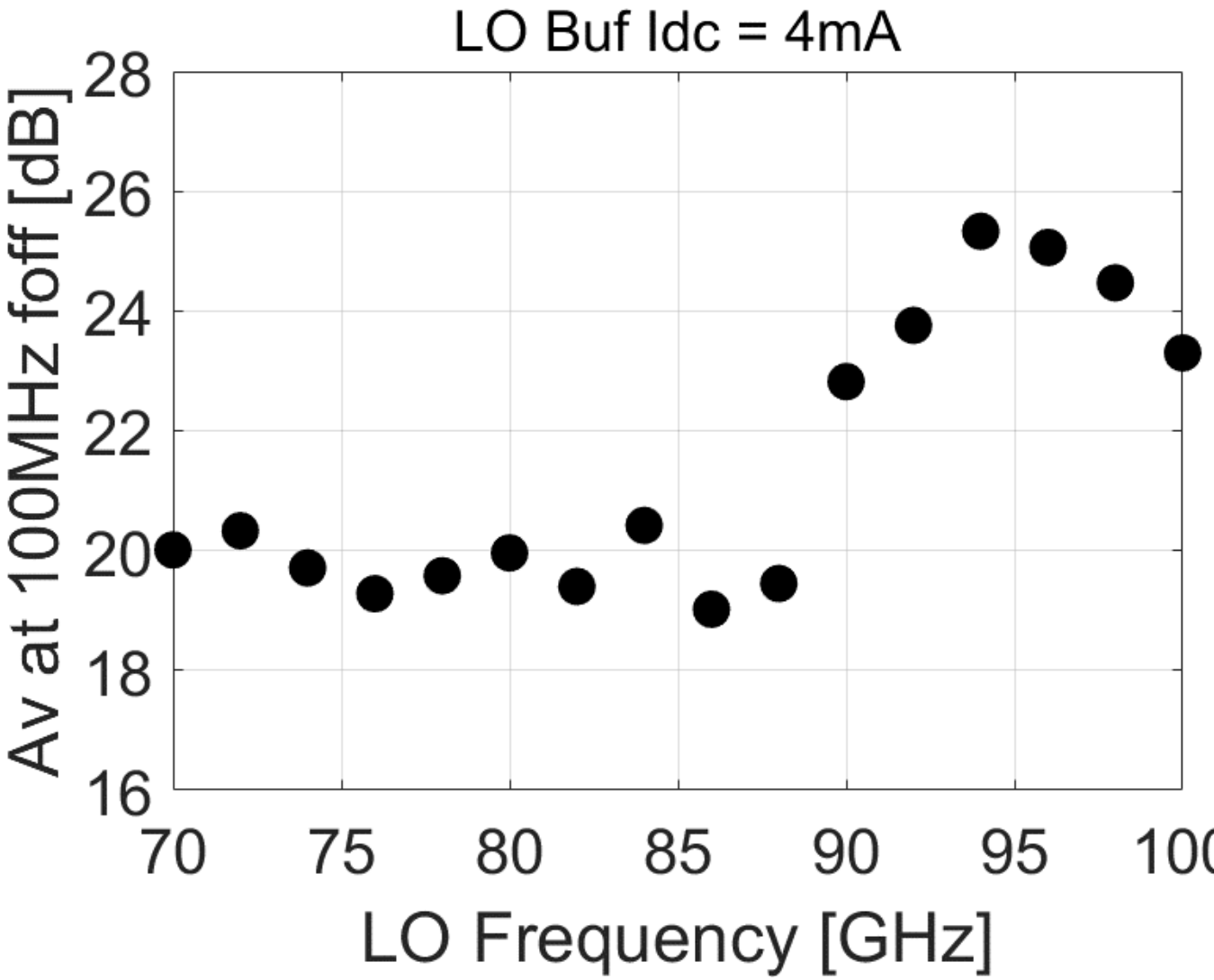
Conversion Gain Measurements



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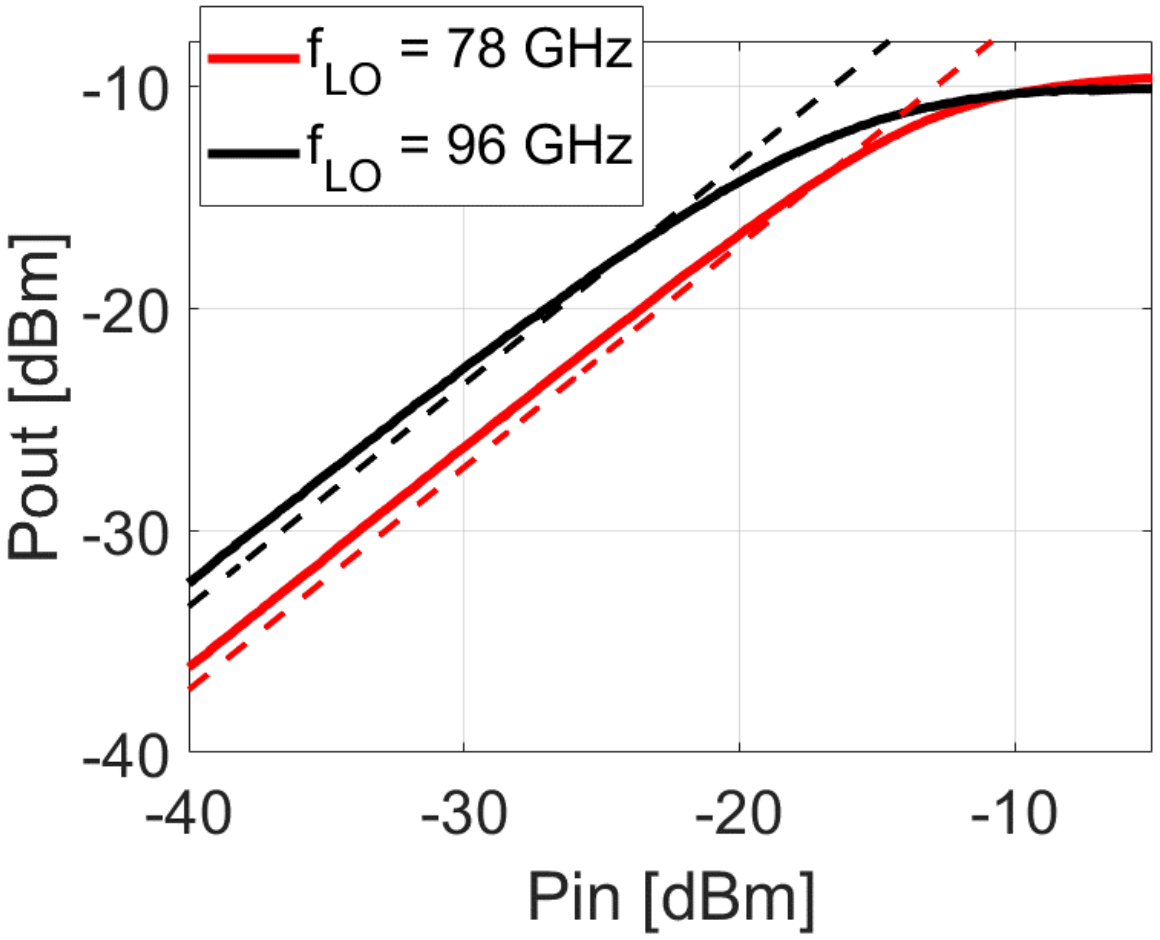
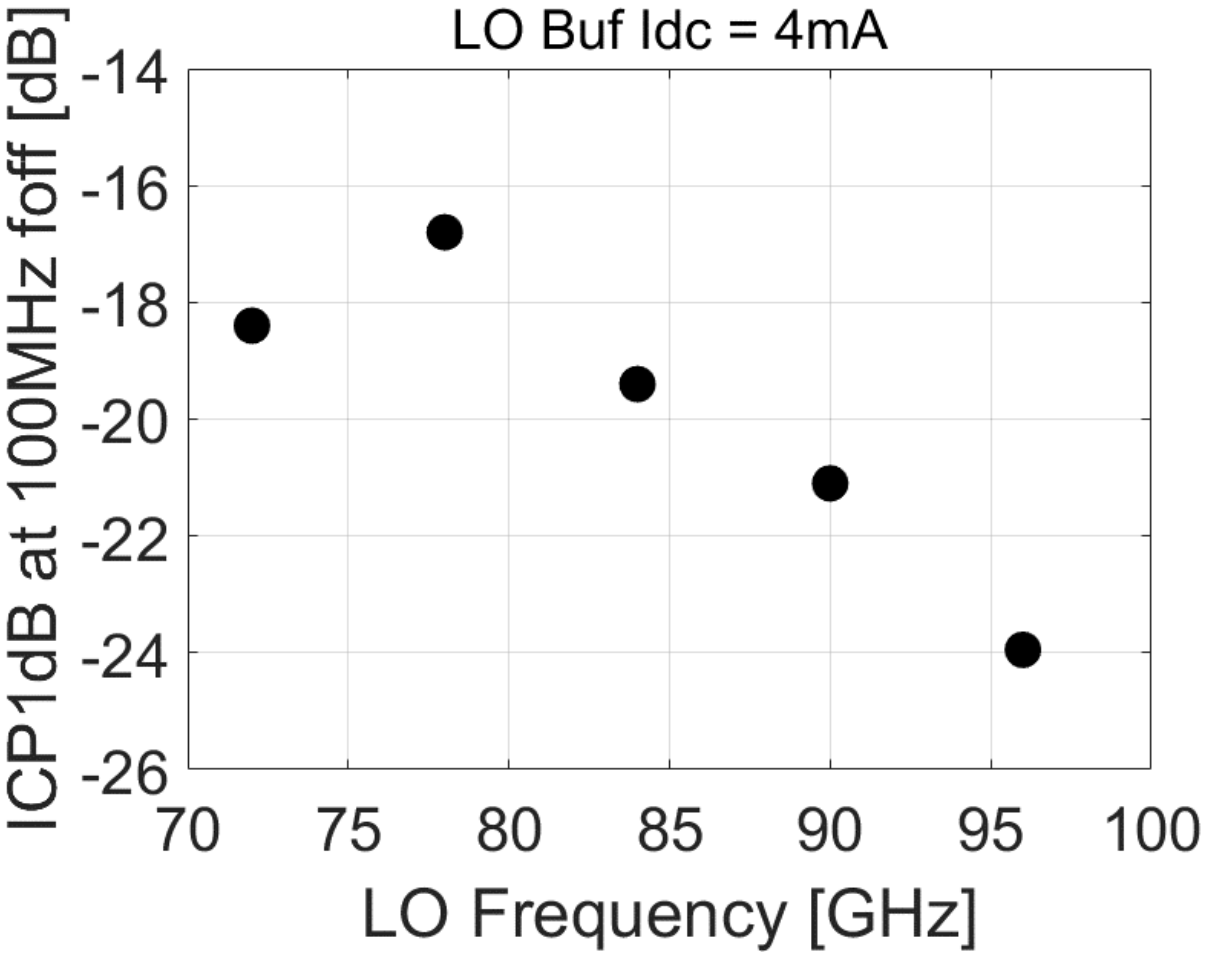
Linearity Measurements





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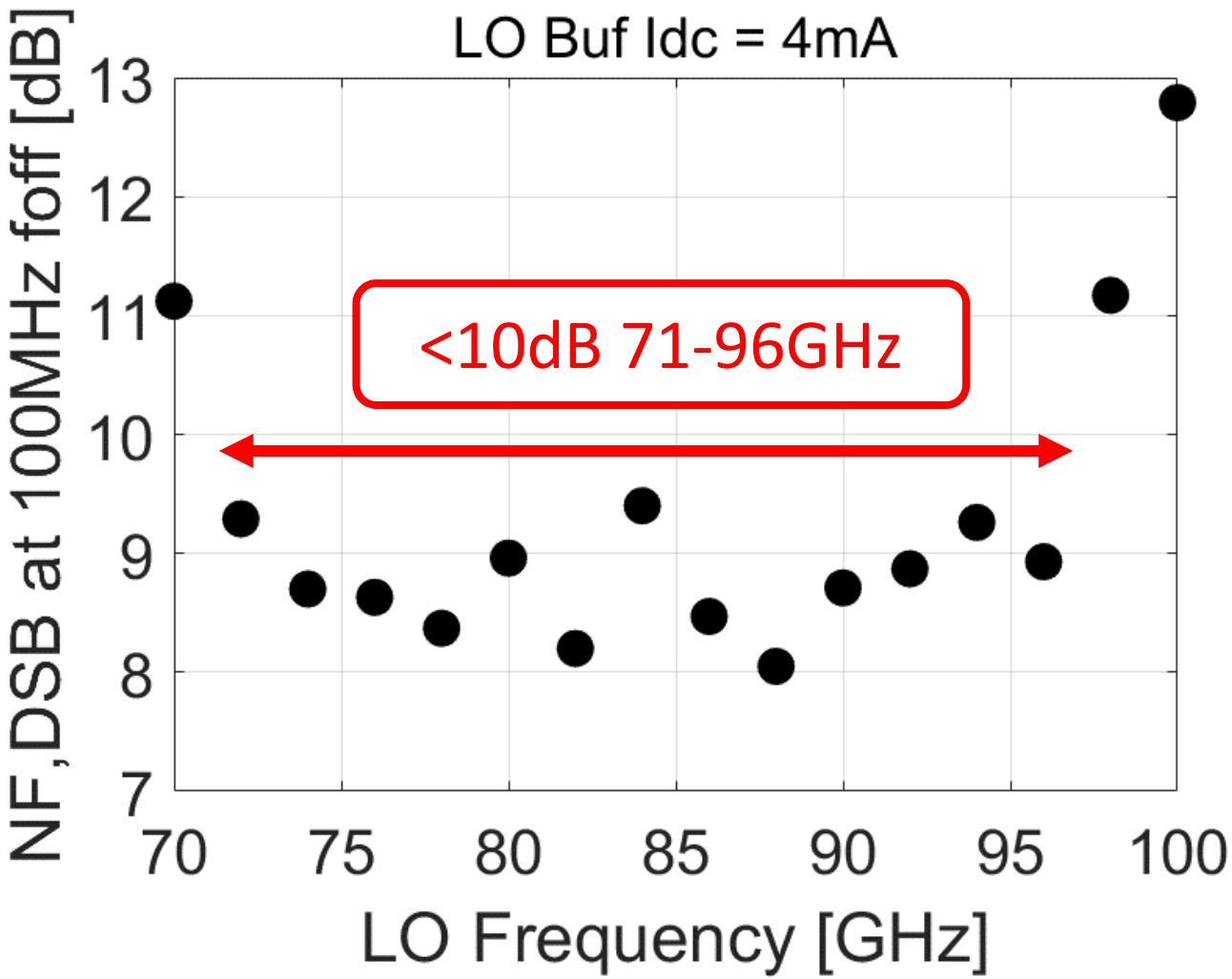
Noise Figure Measurements



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Performance Summary

	This work		Moroni RFIC10	Vigilante JSSC17		Khanpour JSSC08	Kundu JSSC15	
Tech	28nm CMOS		65nm CMOS	28nm CMOS		65nm CMOS	45nm CMOS SOI	
Architecture	Mixer-first direct conversion		Mixer-first	Sliding IF heterodyne		Direct conv (no IQ)	Direct conversion	
Center freq [GHz]	85		58	75		83	55	
Vdd [V]	1		1.2	0.9		1.8	0.6	1.1
Pdc [mW]	8	12	14	57		89	14	30
Frac RF BW	26.5%	35.3%	>31%	36.7%		19%	38%	
BB BW [GHz]	1.8	1.8	0.32	//	//	9	1.2	
Av[dB]	21-26	19.5-25	13	23.6	30.8	13	20.2	26.2
NF,DSB [dB]	8.2-10.8	8-12.7	11-14	7.3-9	9.5-13	5.5-7.5	7.7-12	5.5-10
Max ICP1dB [dBm]	-18	-16.8	-12	-25	-20	-16	-28	-27
Area [mm^2]	0.085		0.18	0.675		0.23	0.225	

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Conclusions

- A 70-100GHz mixer-first RX is proposed, leveraging frequency-translational feedback and a wideband matching network
- Proposed RX achieves ultra-low power operation, without severe impact on NF and linearity
- Suitable as a front-end for E-Band massive MIMO systems

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- Prof. F. Svelto (Univ. of Pavia) for supporting the project
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A 13th-Order CMOS Reconfigurable RF BPF with Adjustable Transmission Zeros for SAW-Less SDR Receivers

Pingyue Song, Hossein Hashemi

University of Southern California

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Outline

- **Radio Frequency Band-Pass Filters**
- **Switch-Capacitor-Resonator-Based RF BPF Synthesis**
- **Circuit Implementation and Measurement Results**
- **Conclusion**

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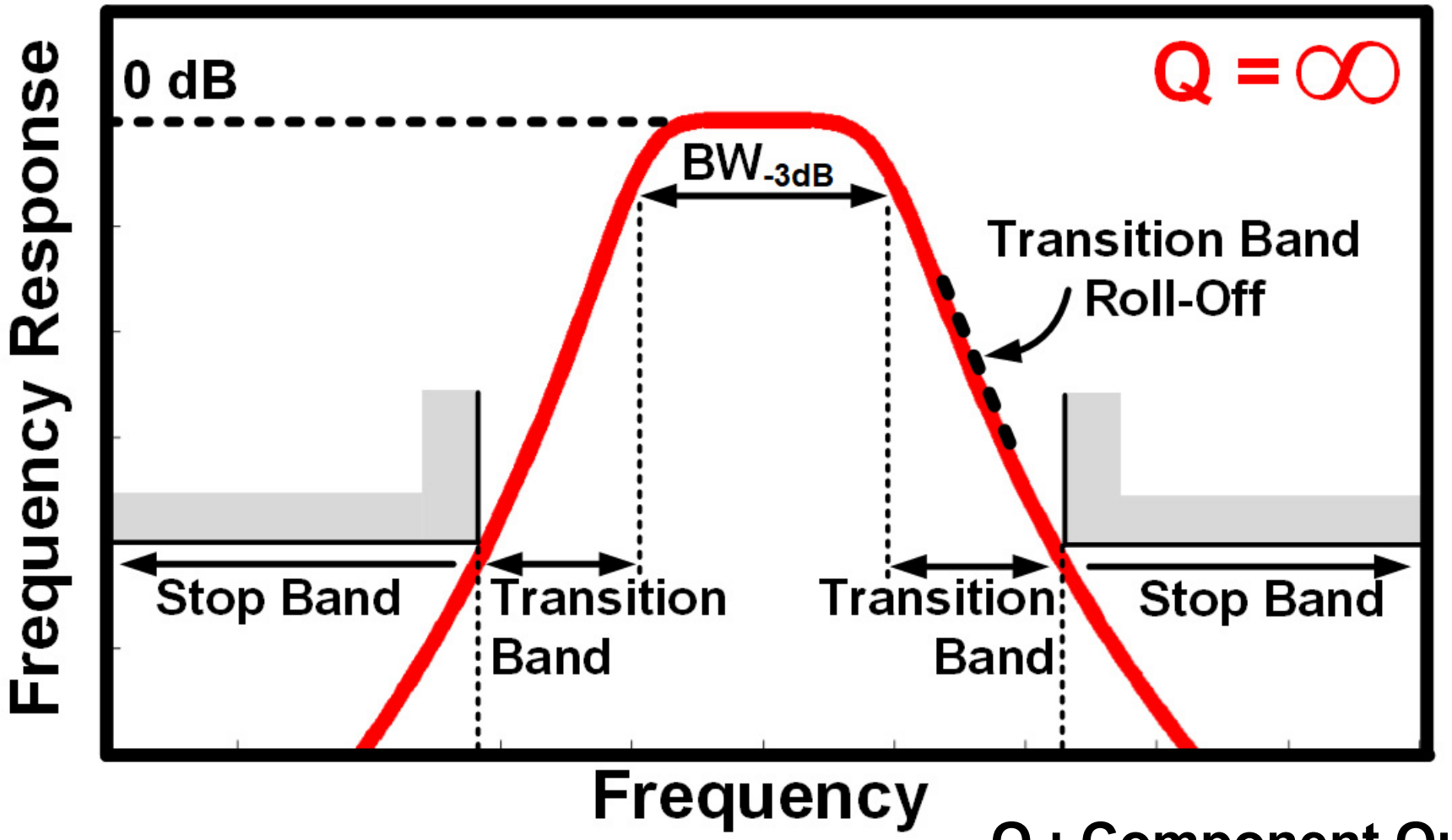
Passive Band-Pass Filters



Q : Component Quality Factor

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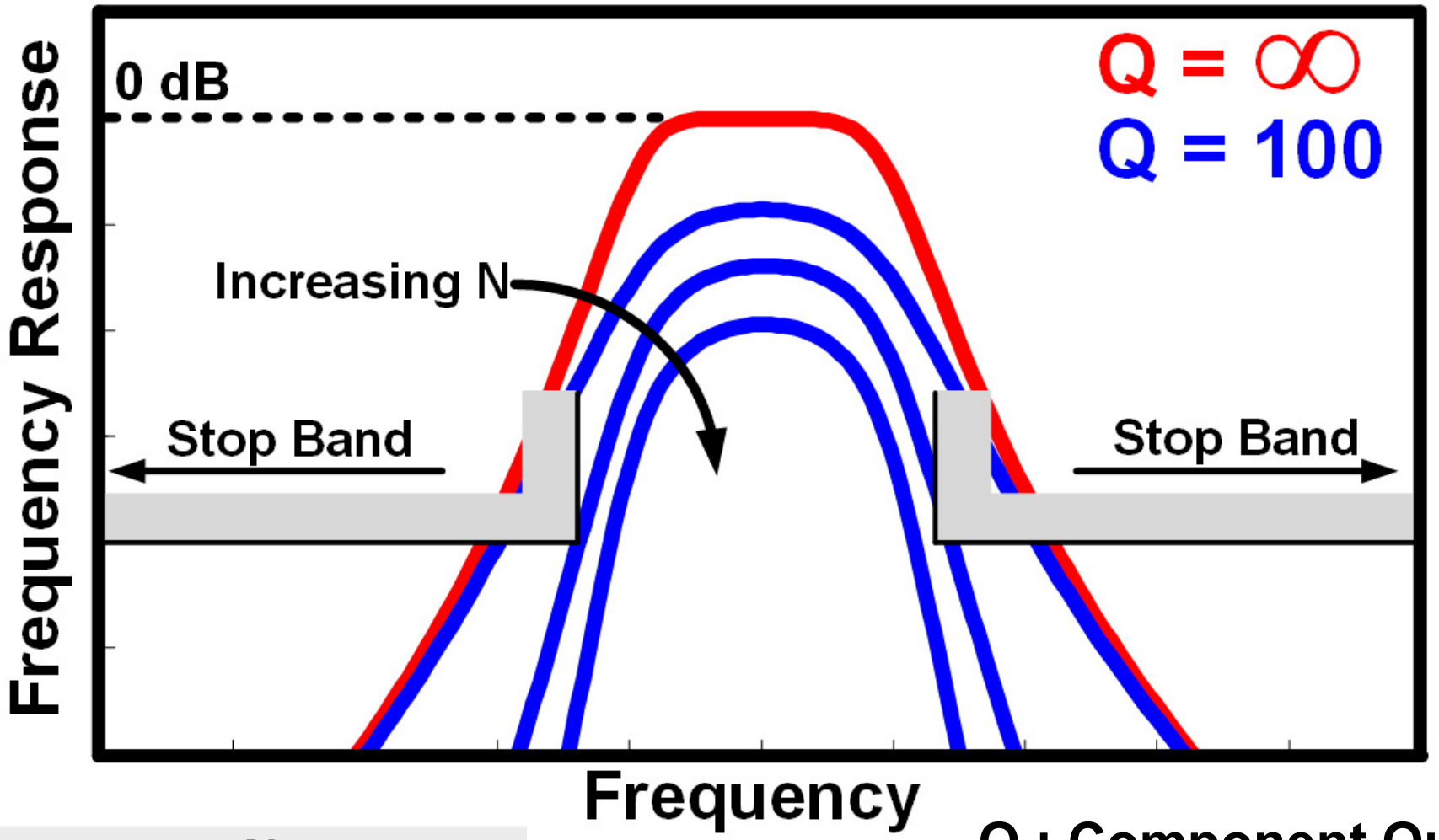
All-Pole Passive BPF



$$\text{Insertion Loss (dB)} \approx K \times \frac{N}{Q} \times \frac{\omega_0}{\Delta\omega_{-3dB}}$$

$$\text{Transition-Band Roll-Off} \propto N$$

Q : Component Quality Factor

N : Filter Order

K : Filter-Type Factor

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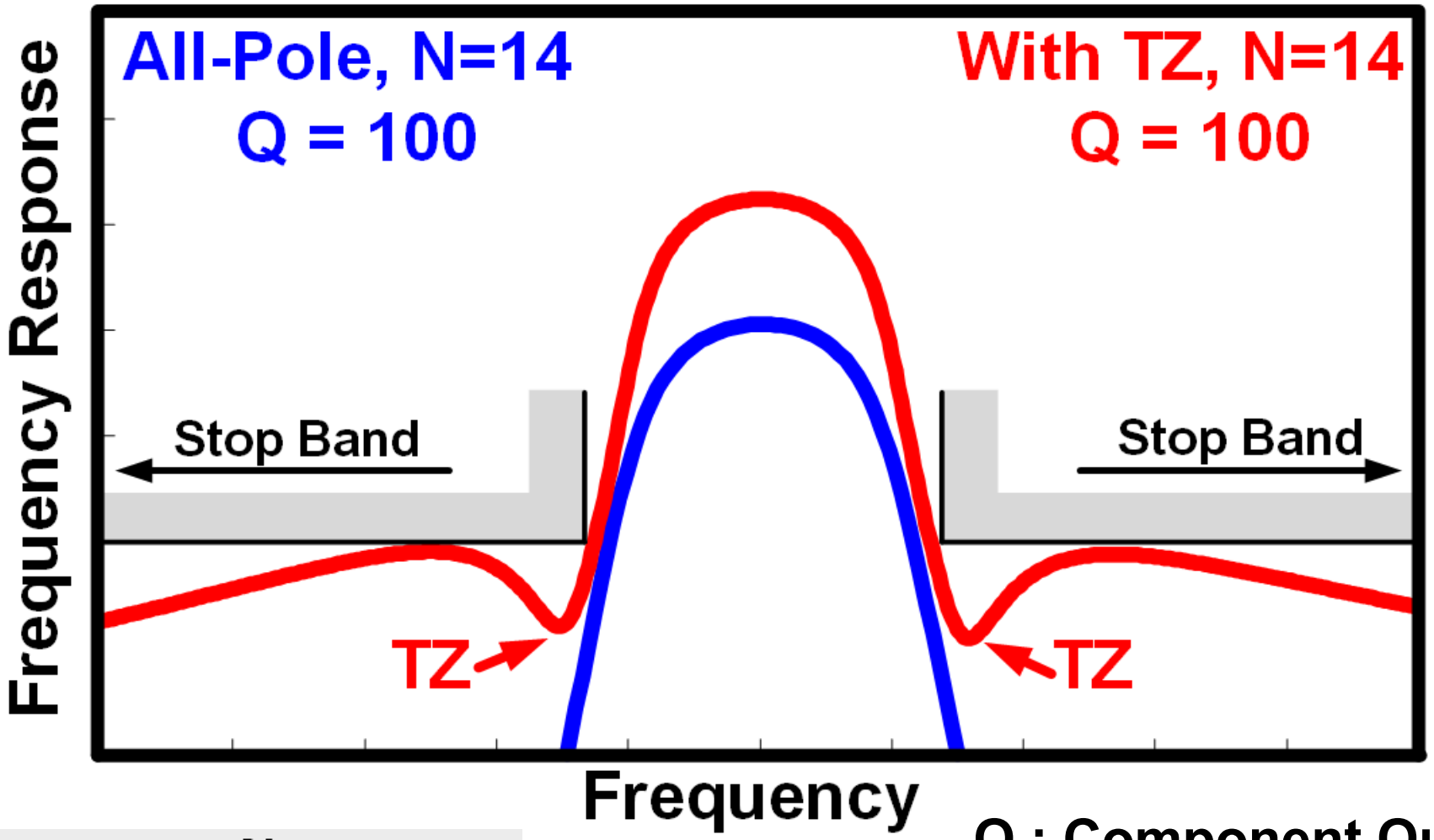
BPF with Transmission Zeros(TZ)



$$\text{Insertion Loss (dB)} \approx K \times \frac{N}{Q} \times \frac{\omega_0}{\Delta\omega_{-3dB}}$$

Transition-Band Roll-Off $\propto$ N, TZ

Q : Component Quality Factor
N : Filter Order
K : Filter-Type Factor

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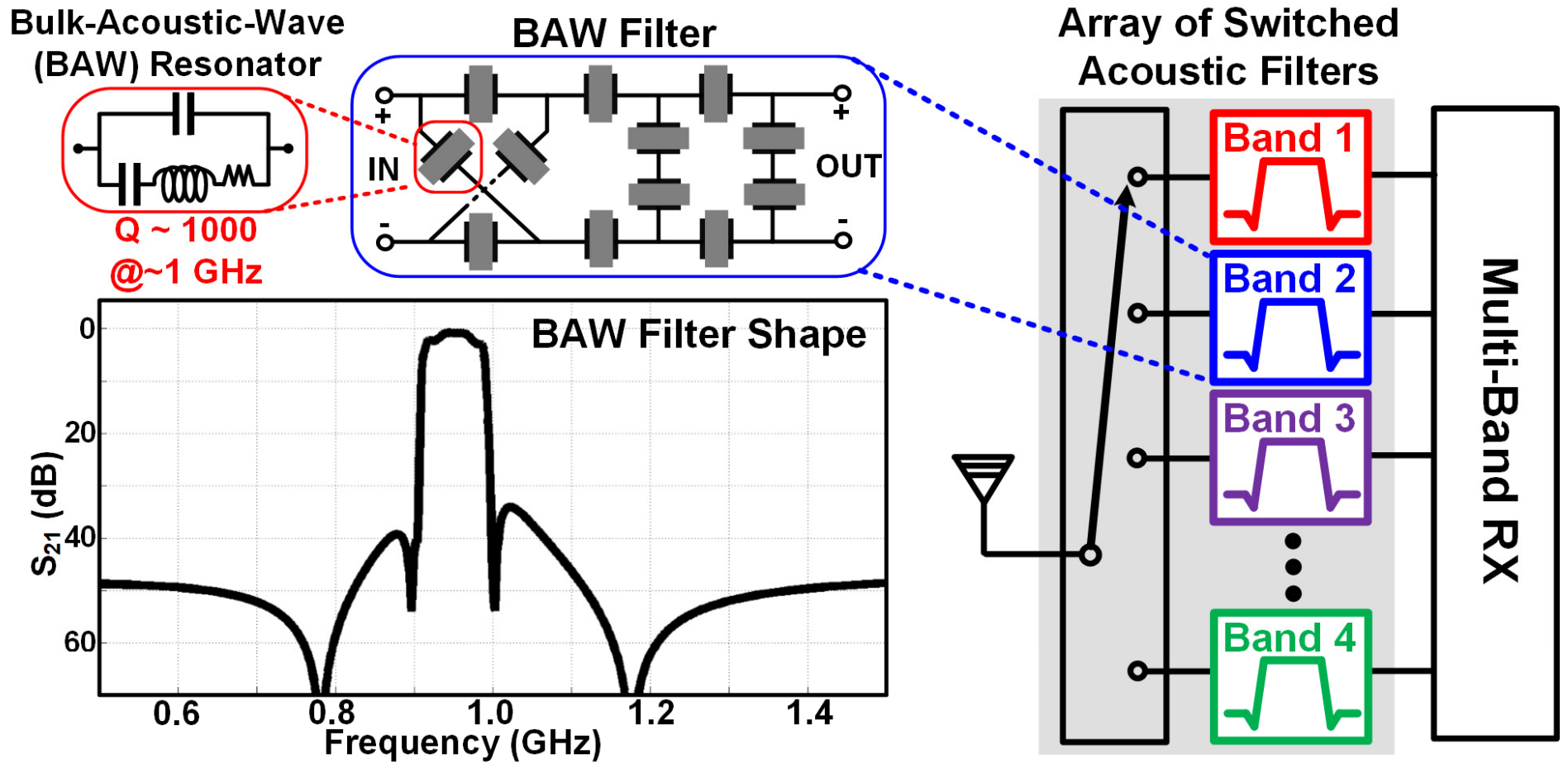
RF Acoustic Filters in Multi-Band Receivers



Array of Switched Acoustic Filters (SAW, BAW)

✓ High Selectivity ✓ Low Insertion Loss ✓ High Linearity

✗ Not CMOS Compatible

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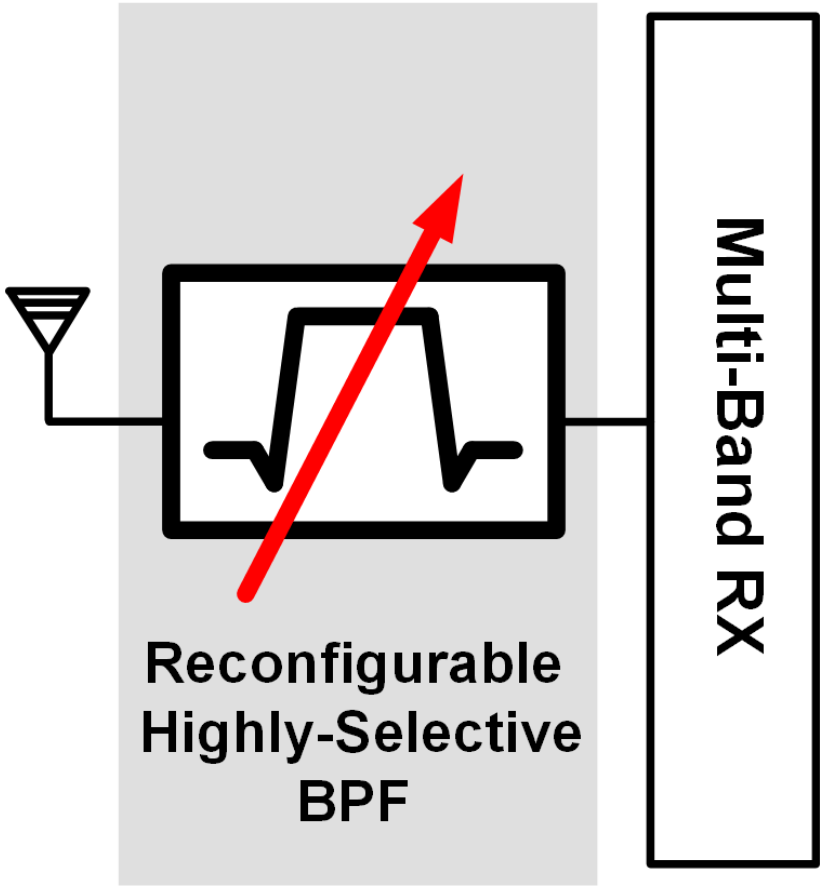
Objective



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Outline

- Radio Frequency Band-Pass Filters
- **Switch-Capacitor-Resonator-Based RF BPF Synthesis**
- Circuit Implementation and Measurement Results
- Conclusion

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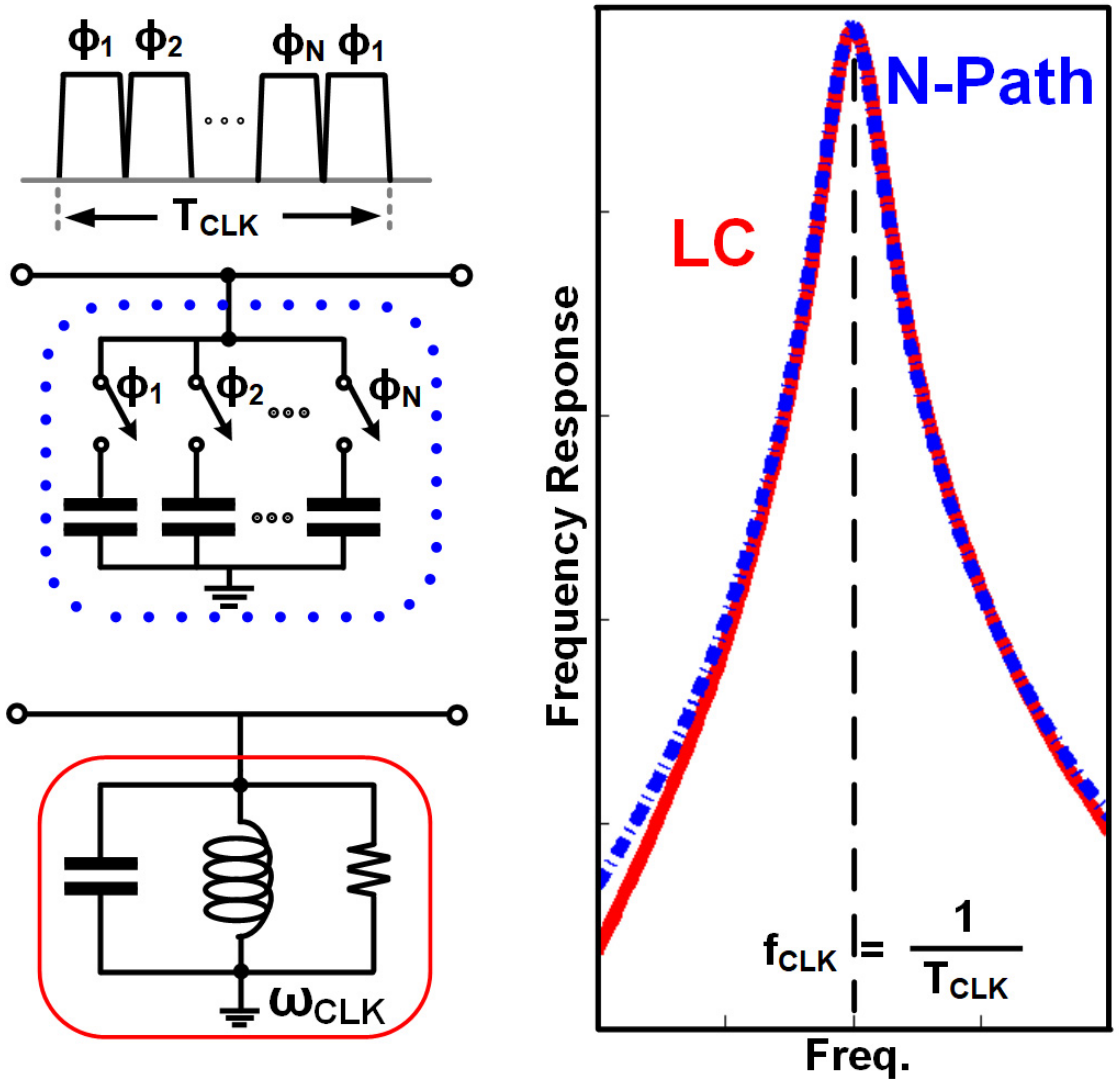
Switch-Capacitor (N-Path) Resonator

N-Path Resonators



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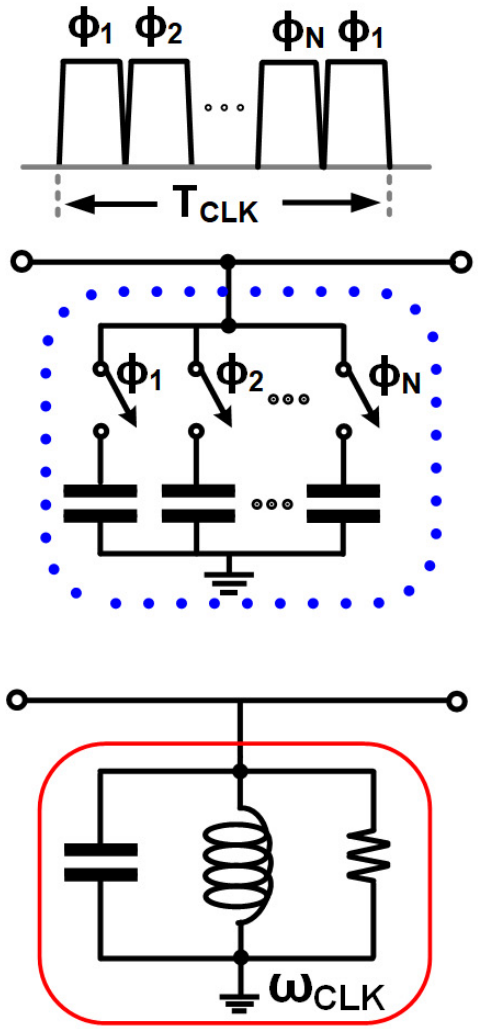
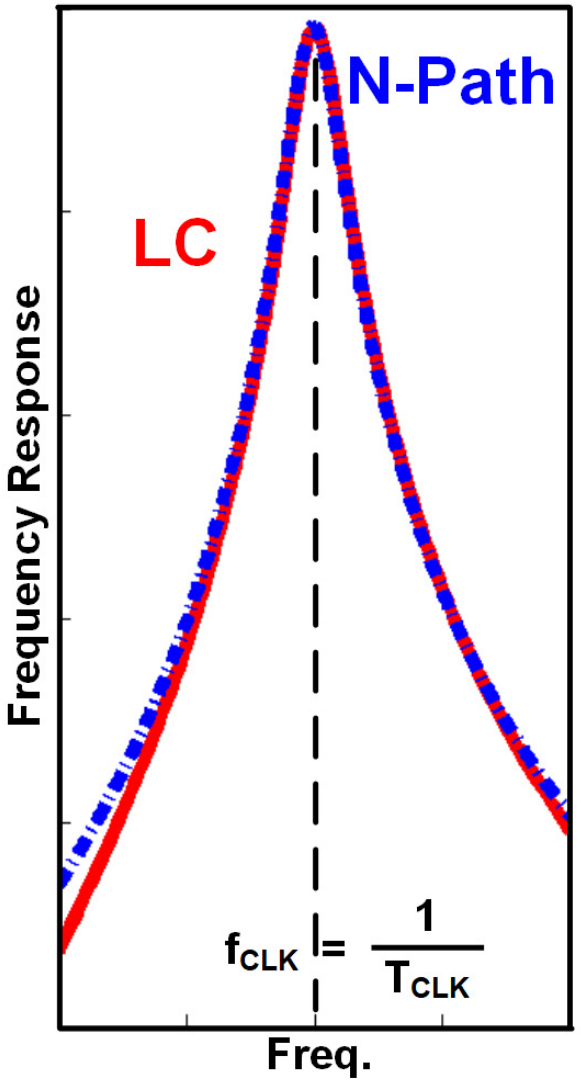
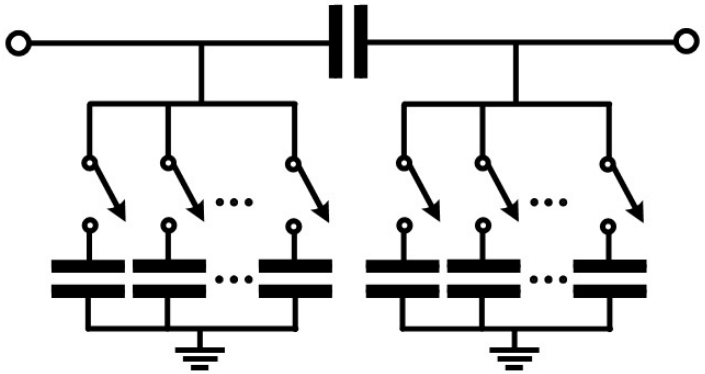
N-Path-Resonator-Based BPF

N-Path Resonators



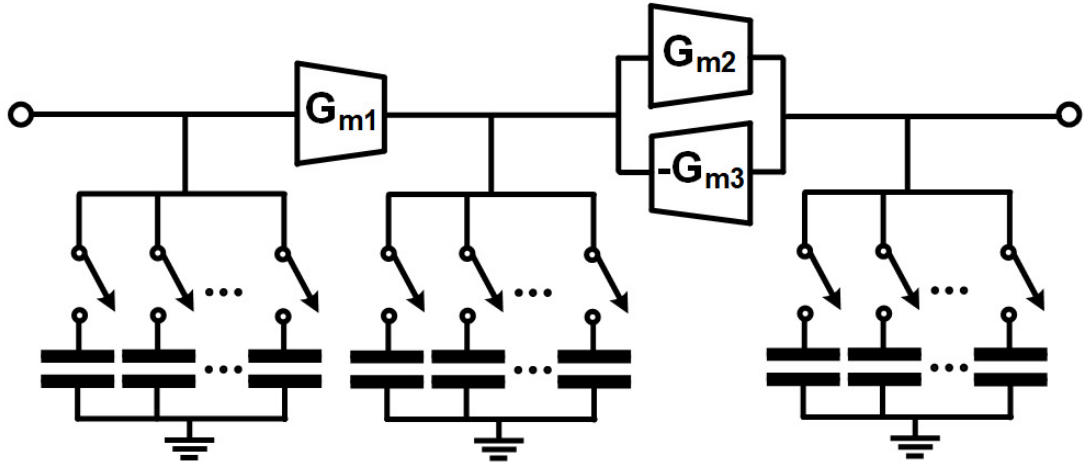


Passively-Coupled N-Path Resonators



[Chen, RFIC 2016]

Actively-Coupled N-Path Resonators



[Darvishi, ISSCC 2013]

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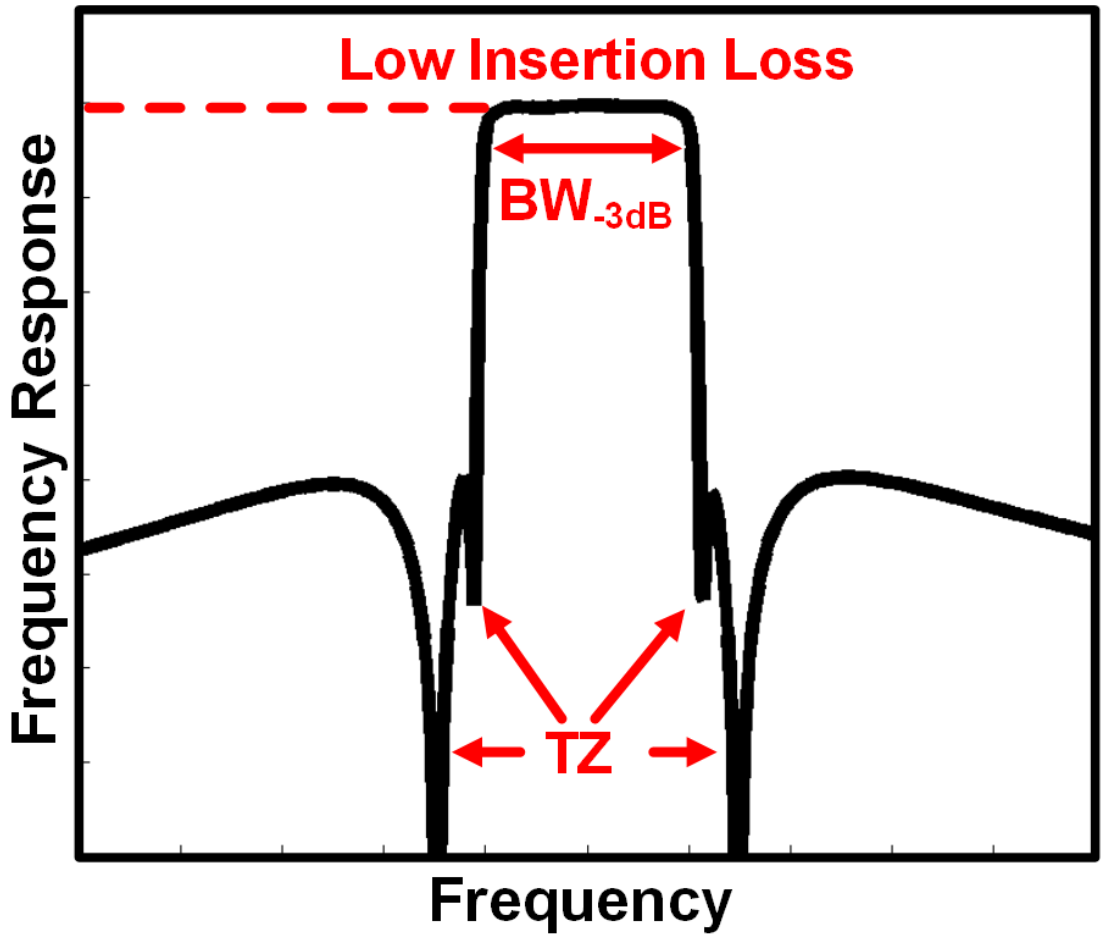
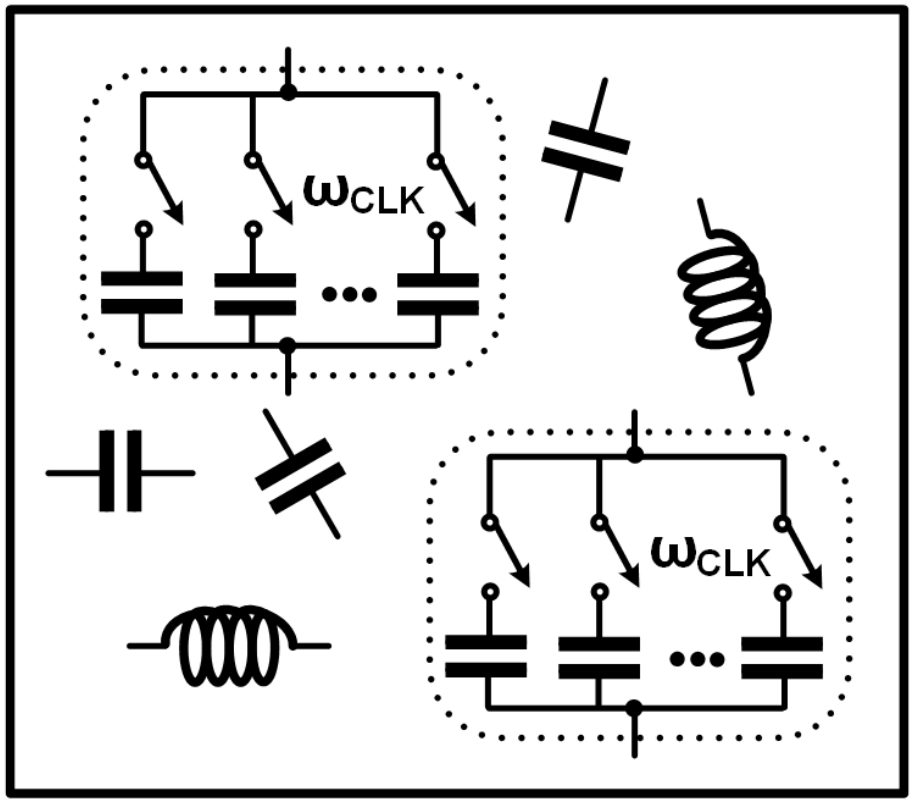
N-Path BPF Synthesis with TZs



Filter Synthesis



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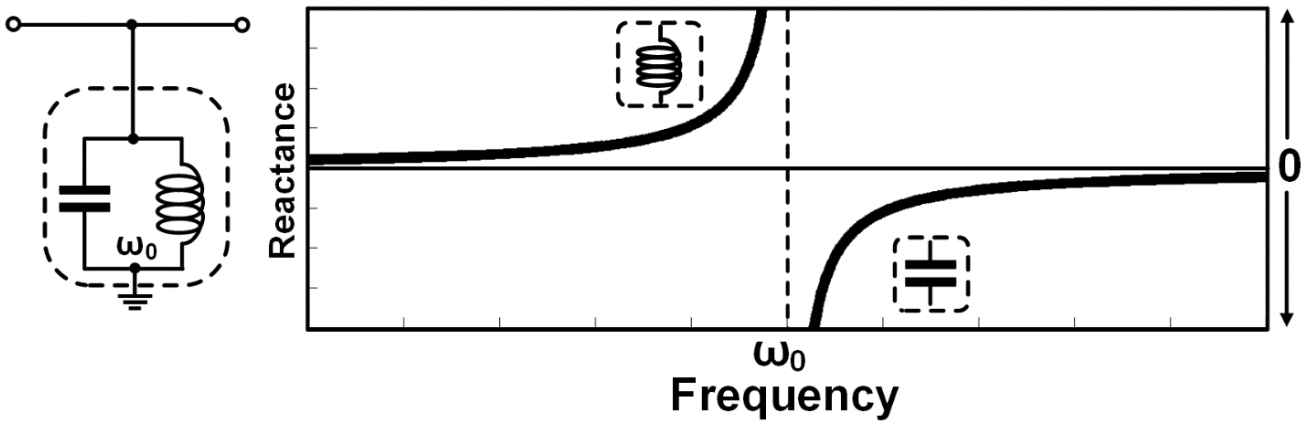
“Anatomy” of LC-Based BPF with TZs



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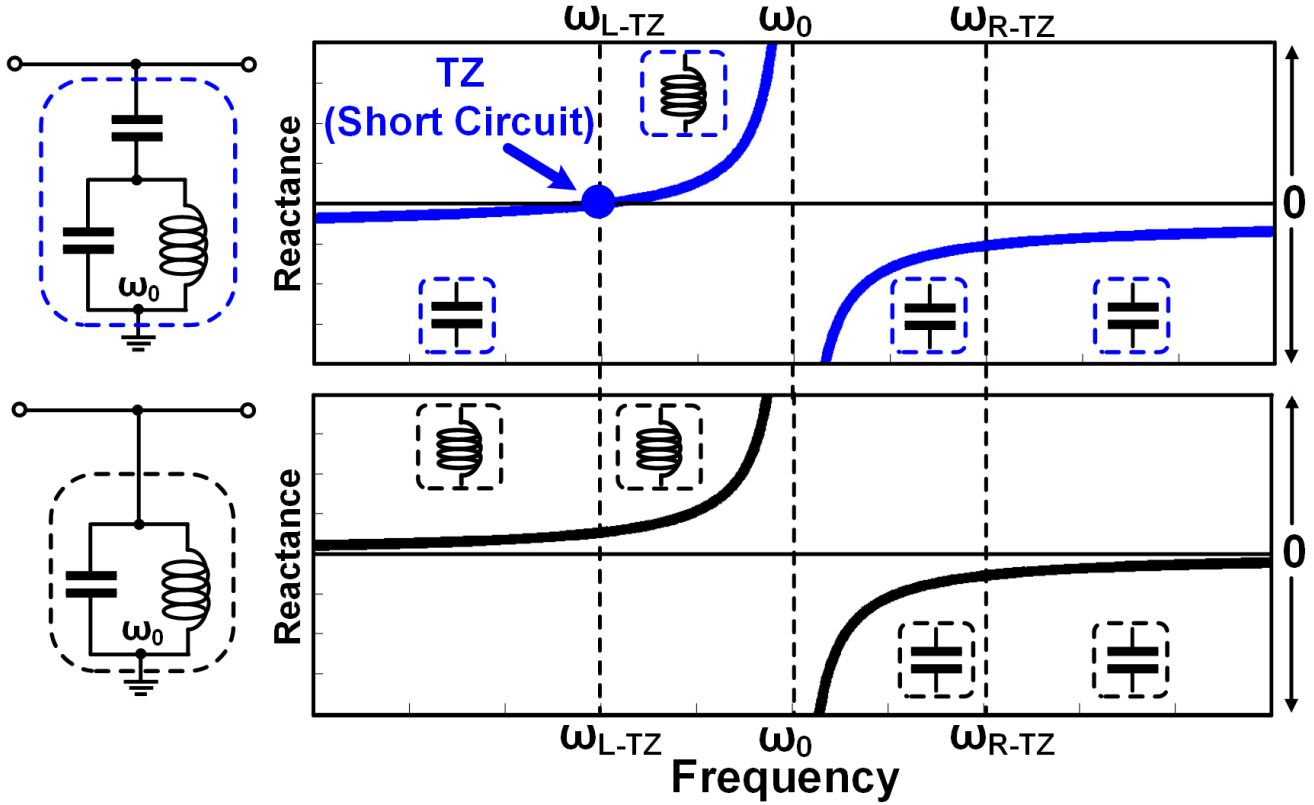
“Anatomy” of LC-Based BPF with TZs



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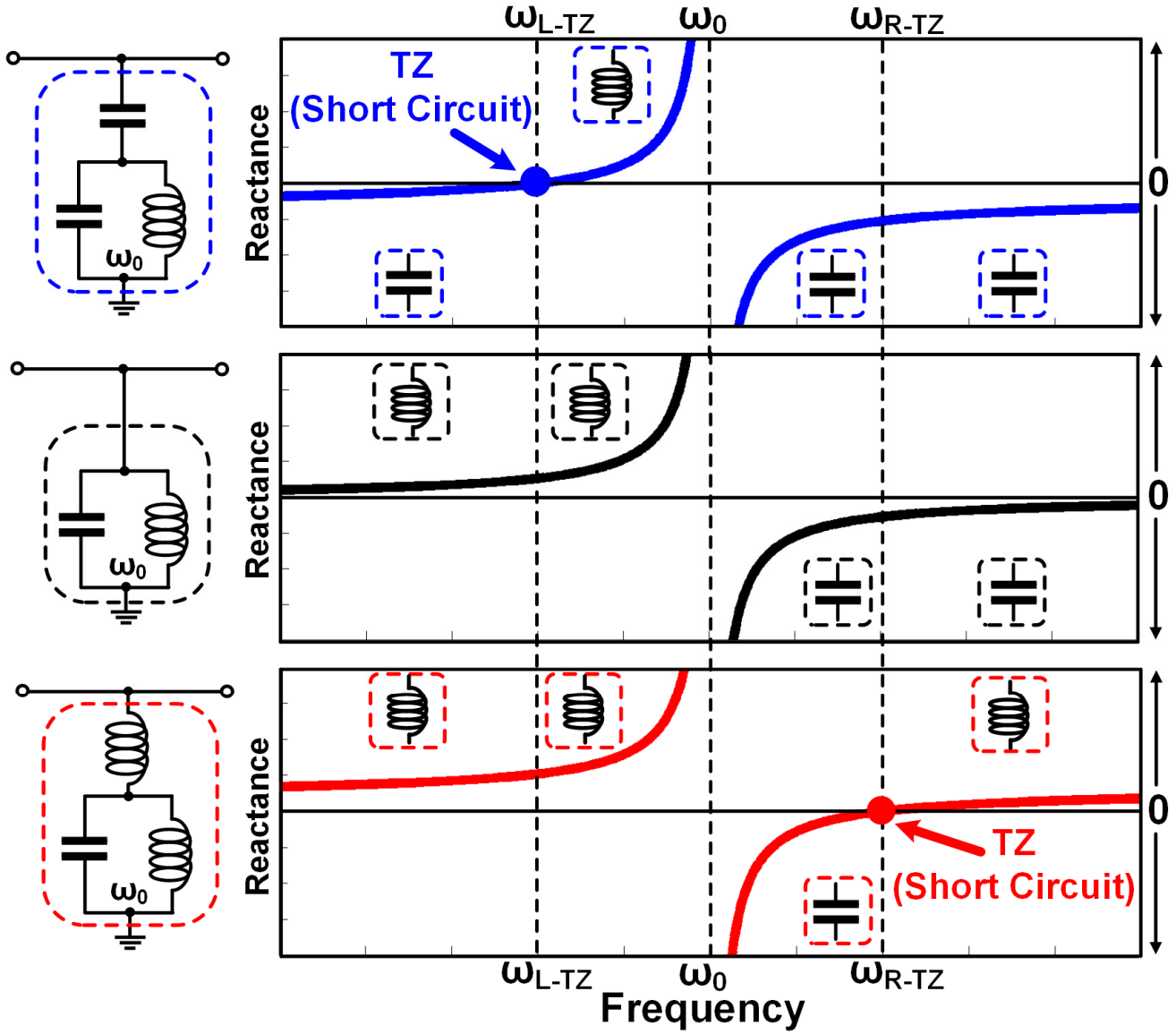
“Anatomy” of LC-Based BPF with TZs



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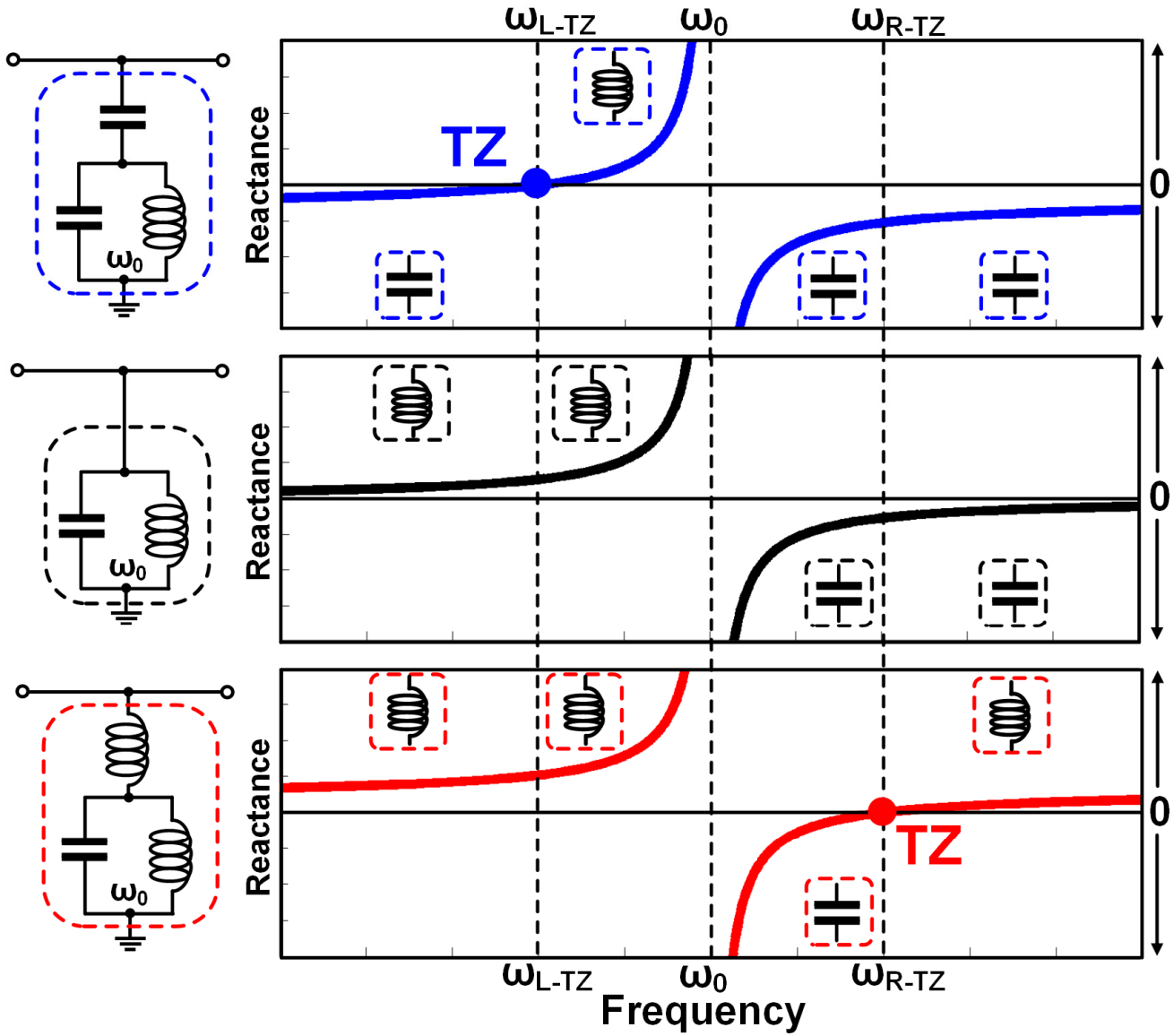
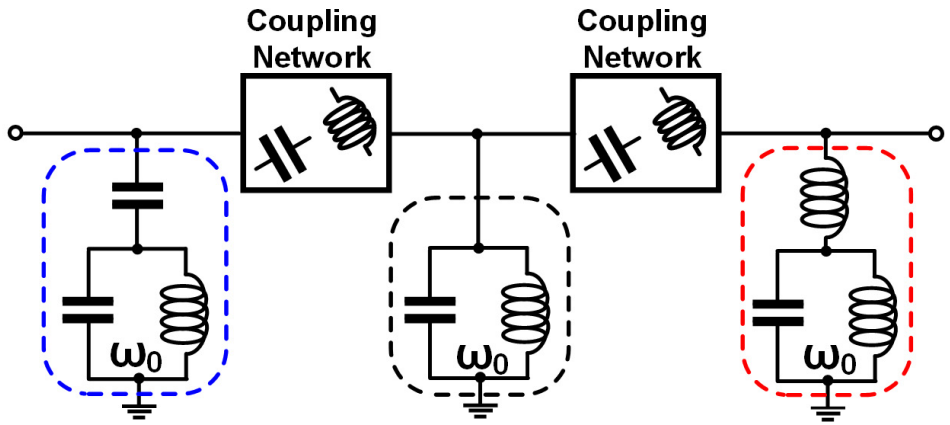
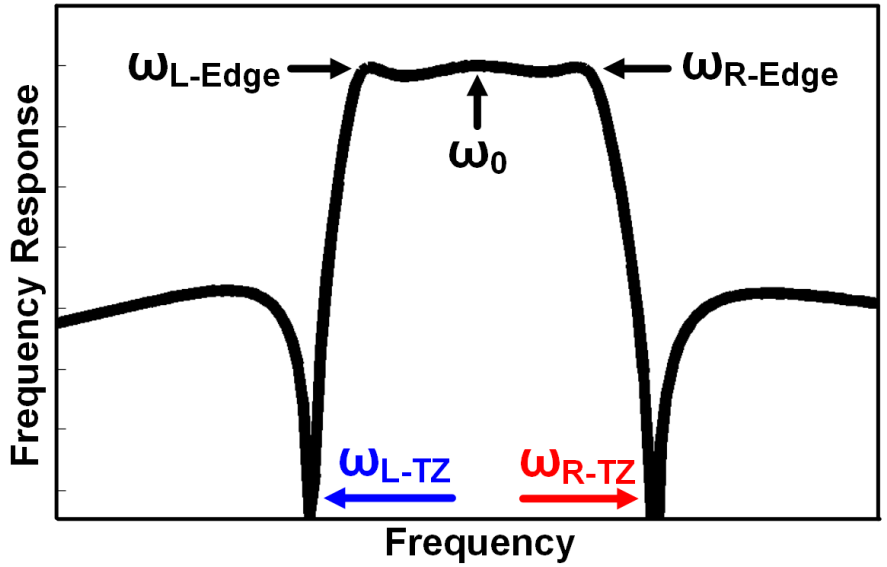
“Anatomy” of LC-Based BPF with TZs







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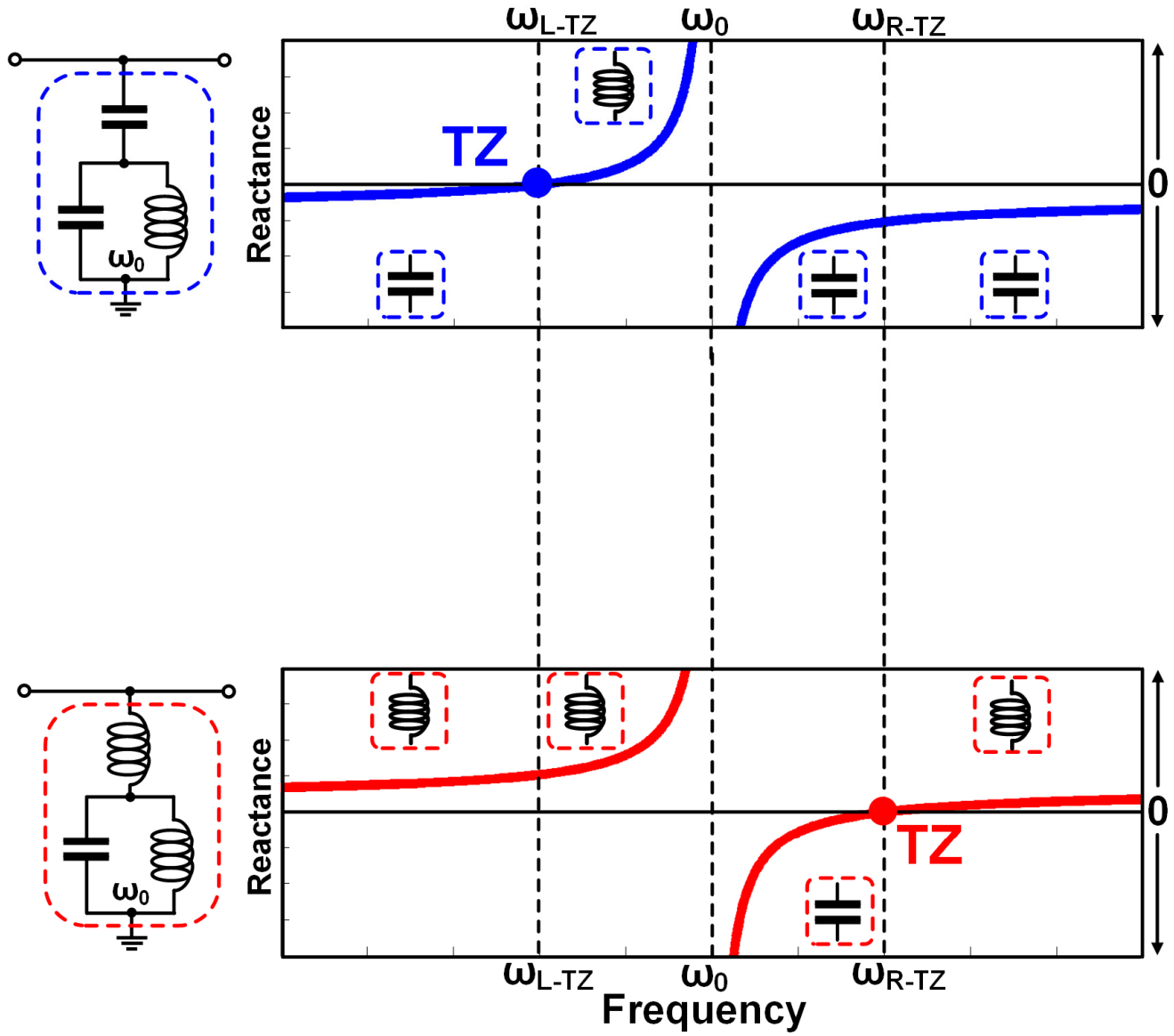
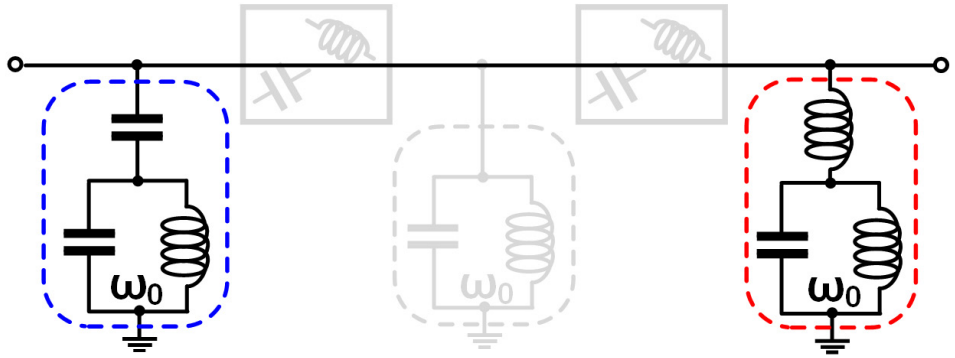
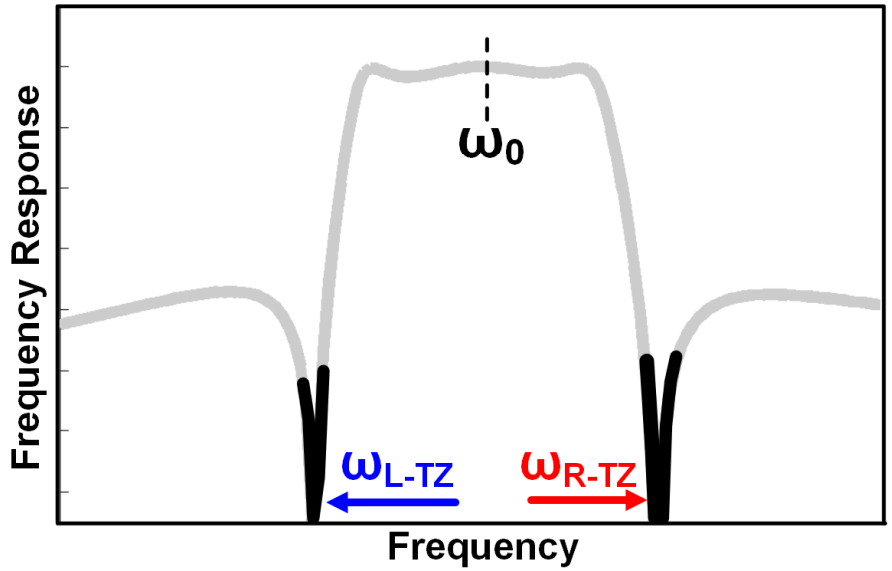
“Anatomy” of LC-Based BPF with TZs







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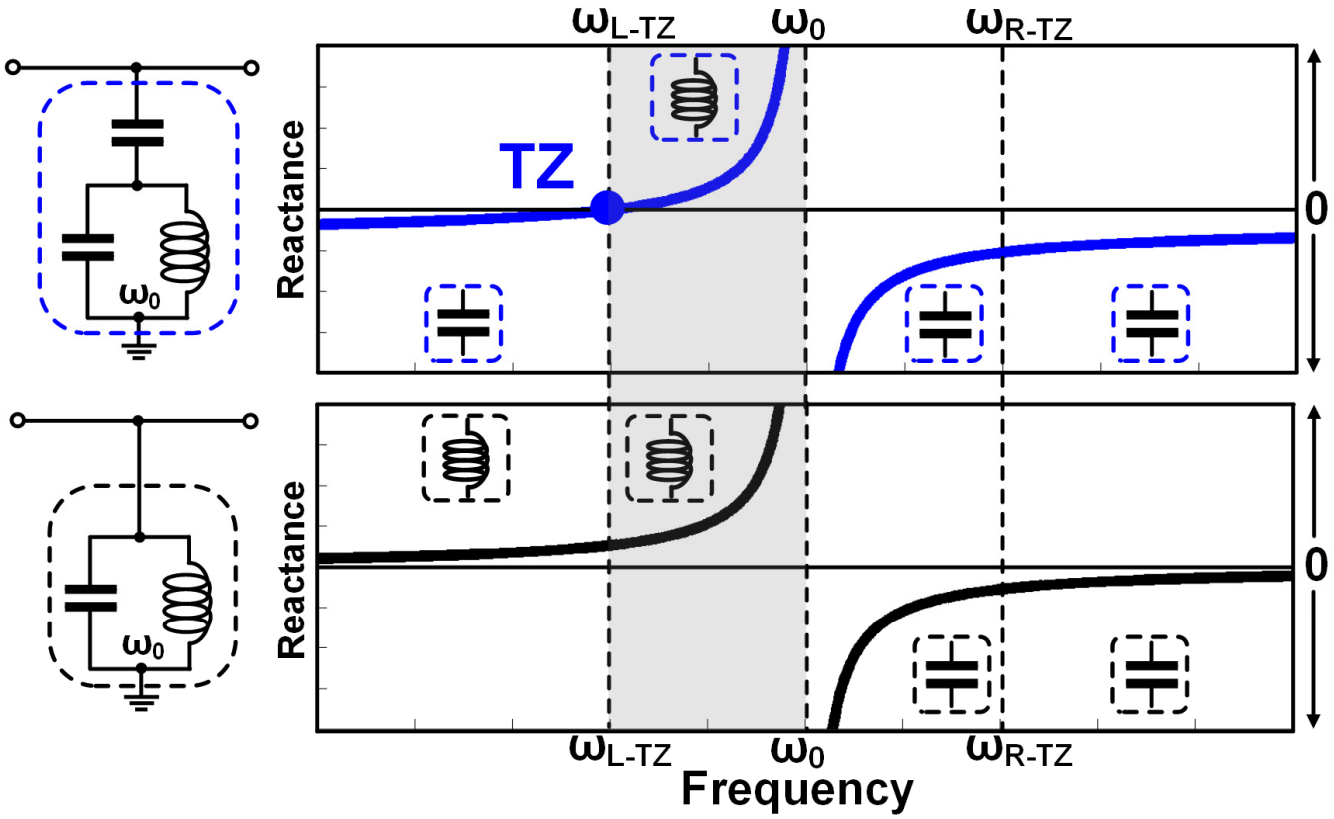
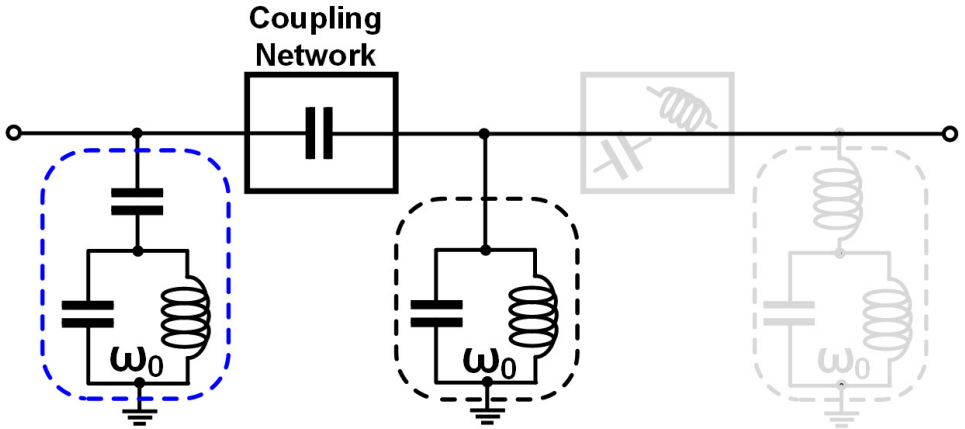
“Anatomy” of LC-Based BPF with TZs





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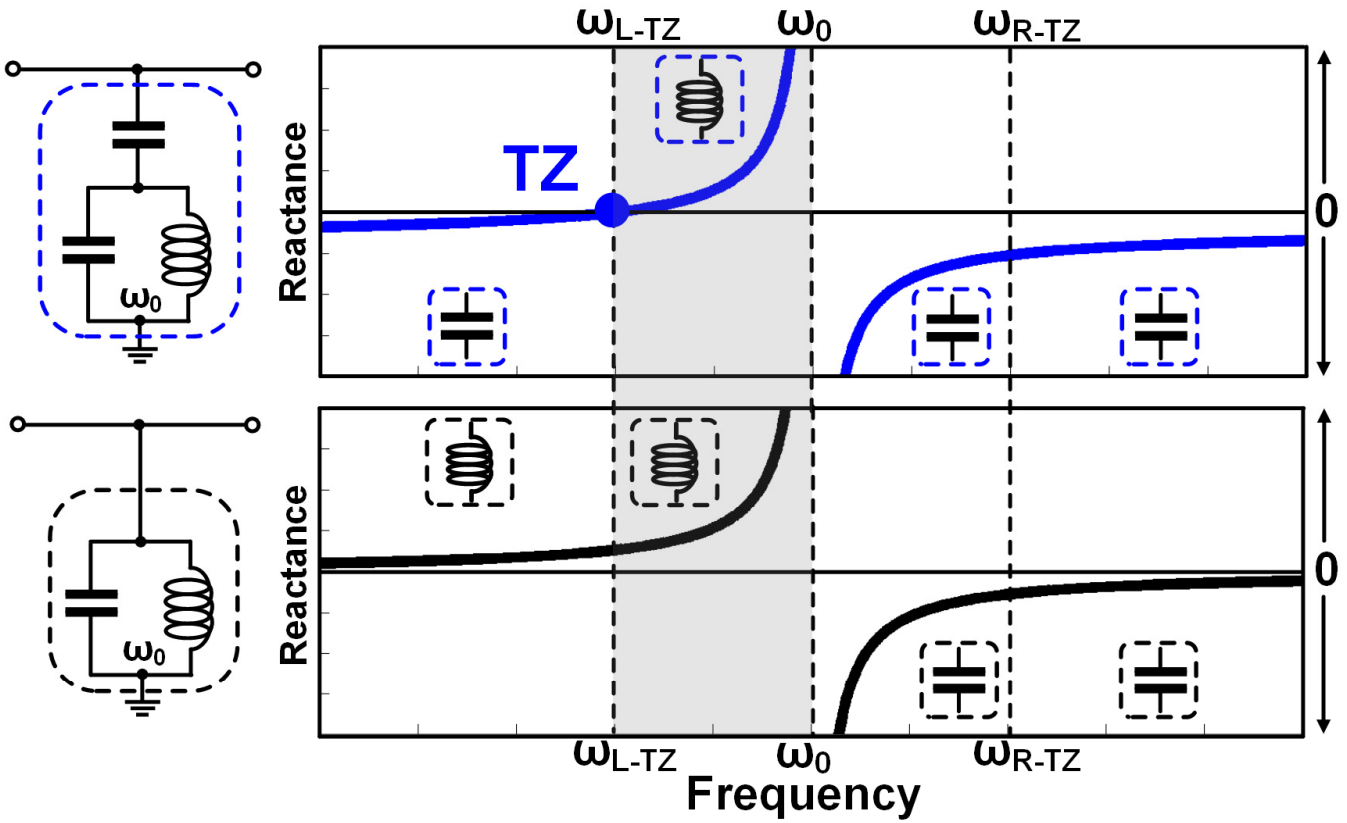
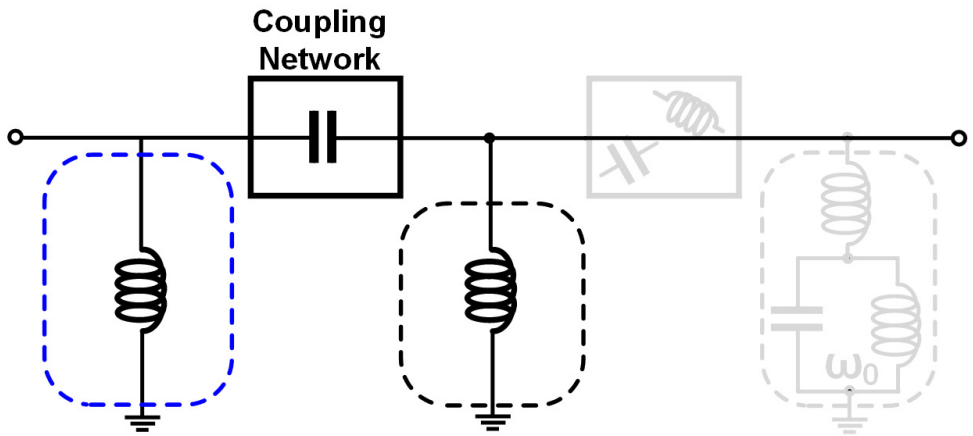
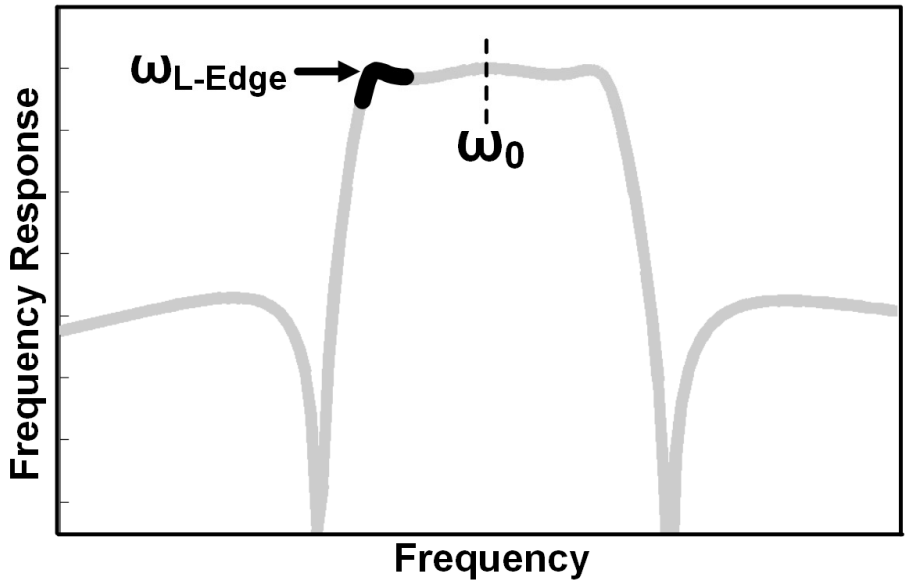
“Anatomy” of LC-Based BPF with TZs







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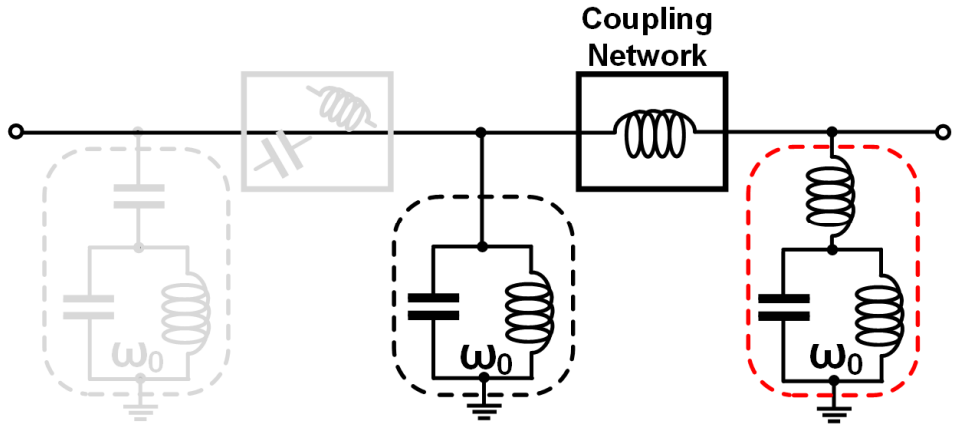
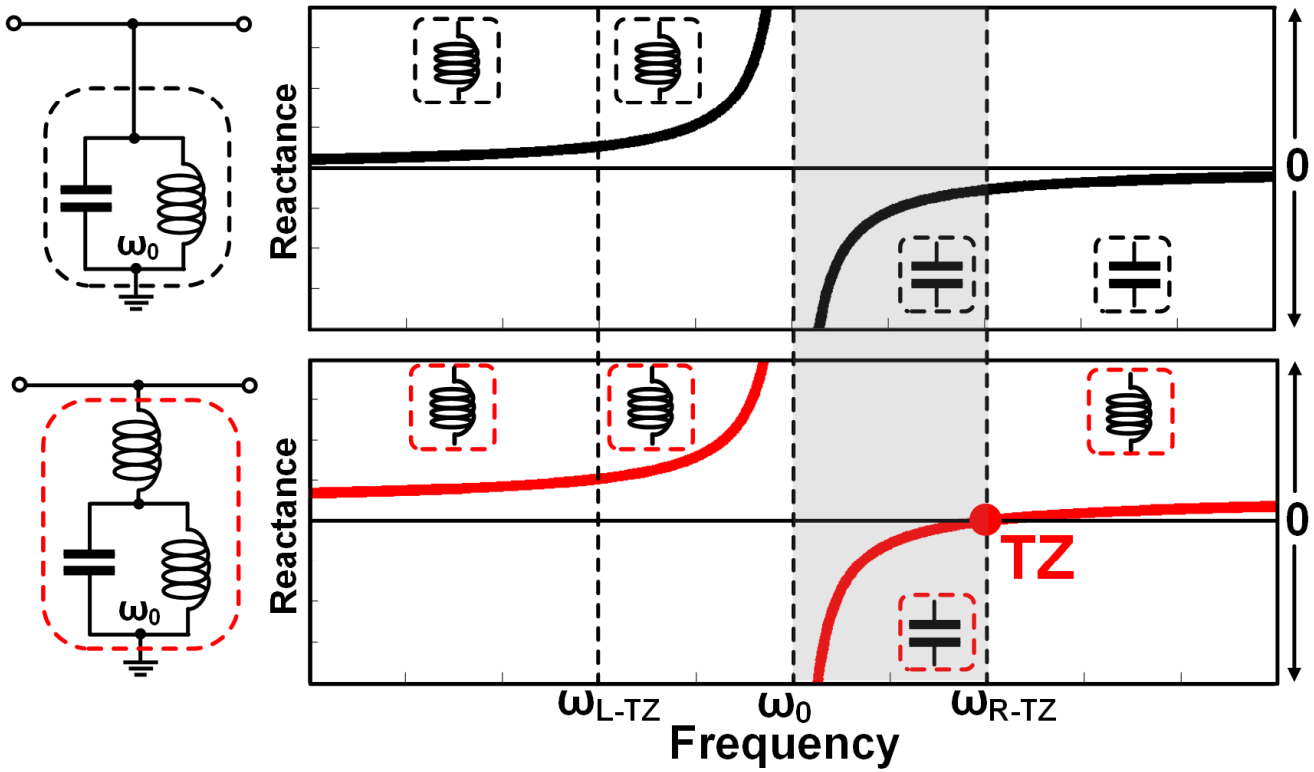
“Anatomy” of LC-Based BPF with TZs





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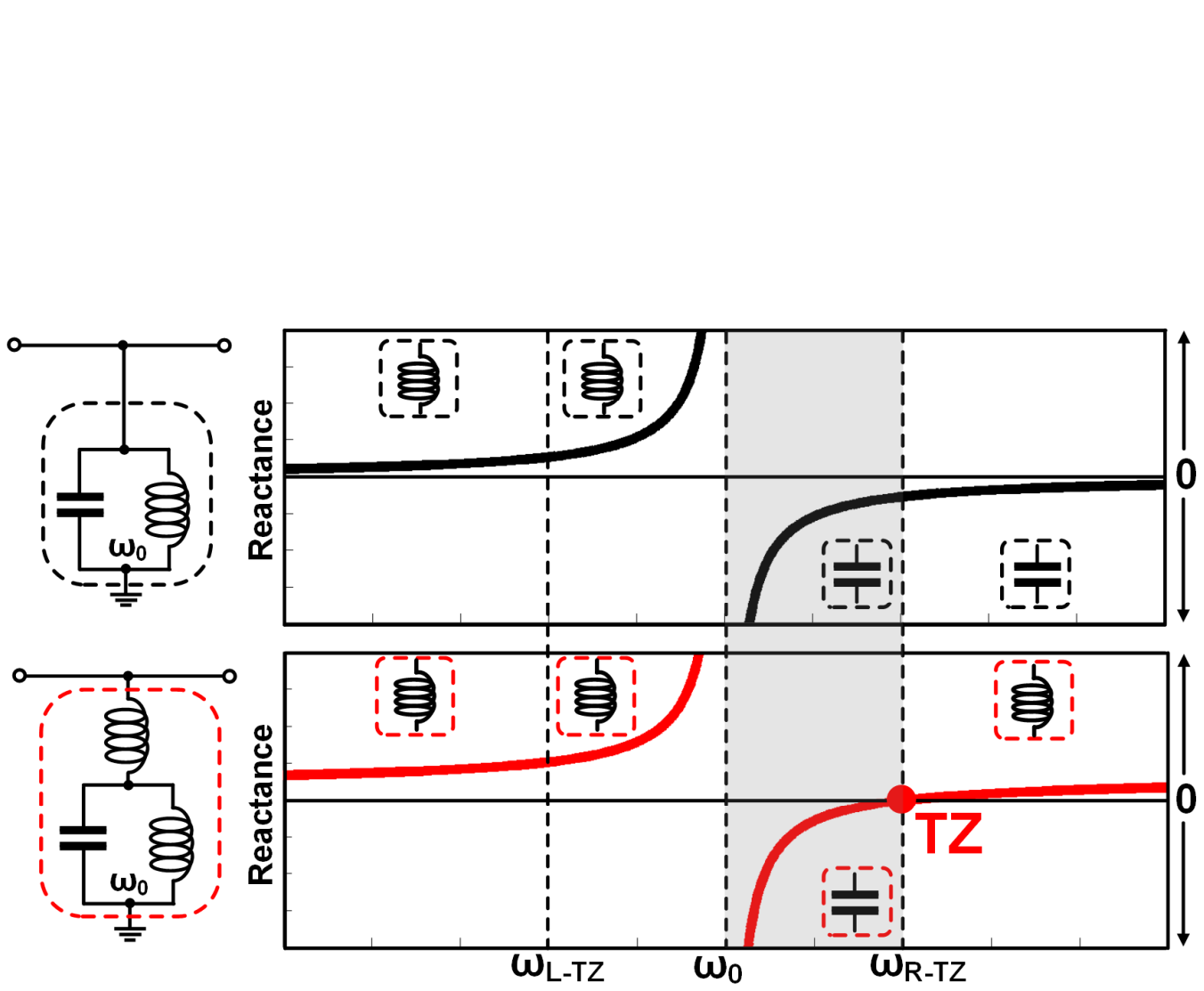
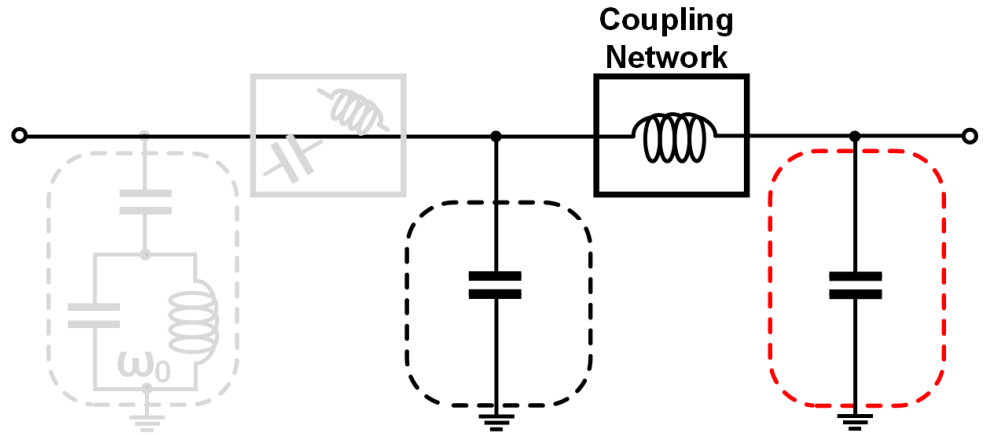
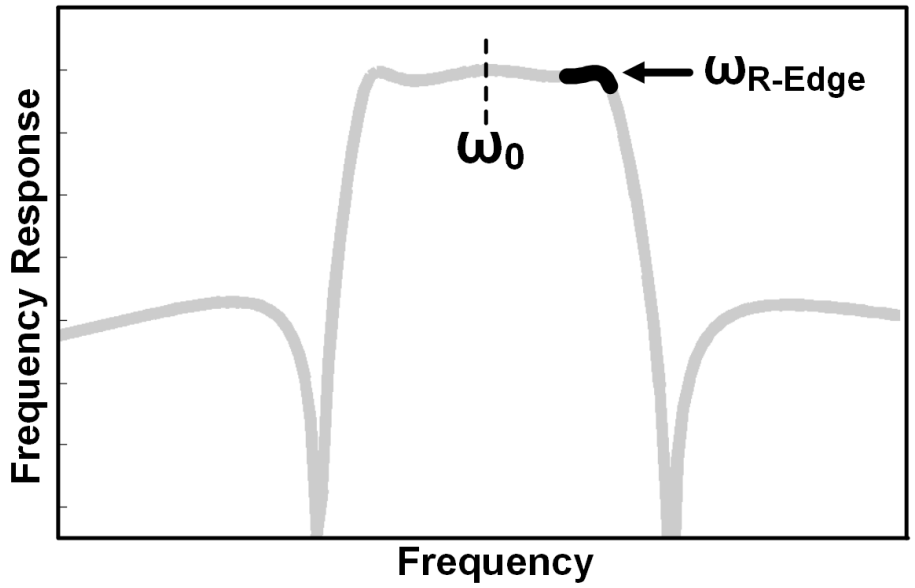
“Anatomy” of LC-Based BPF with TZs







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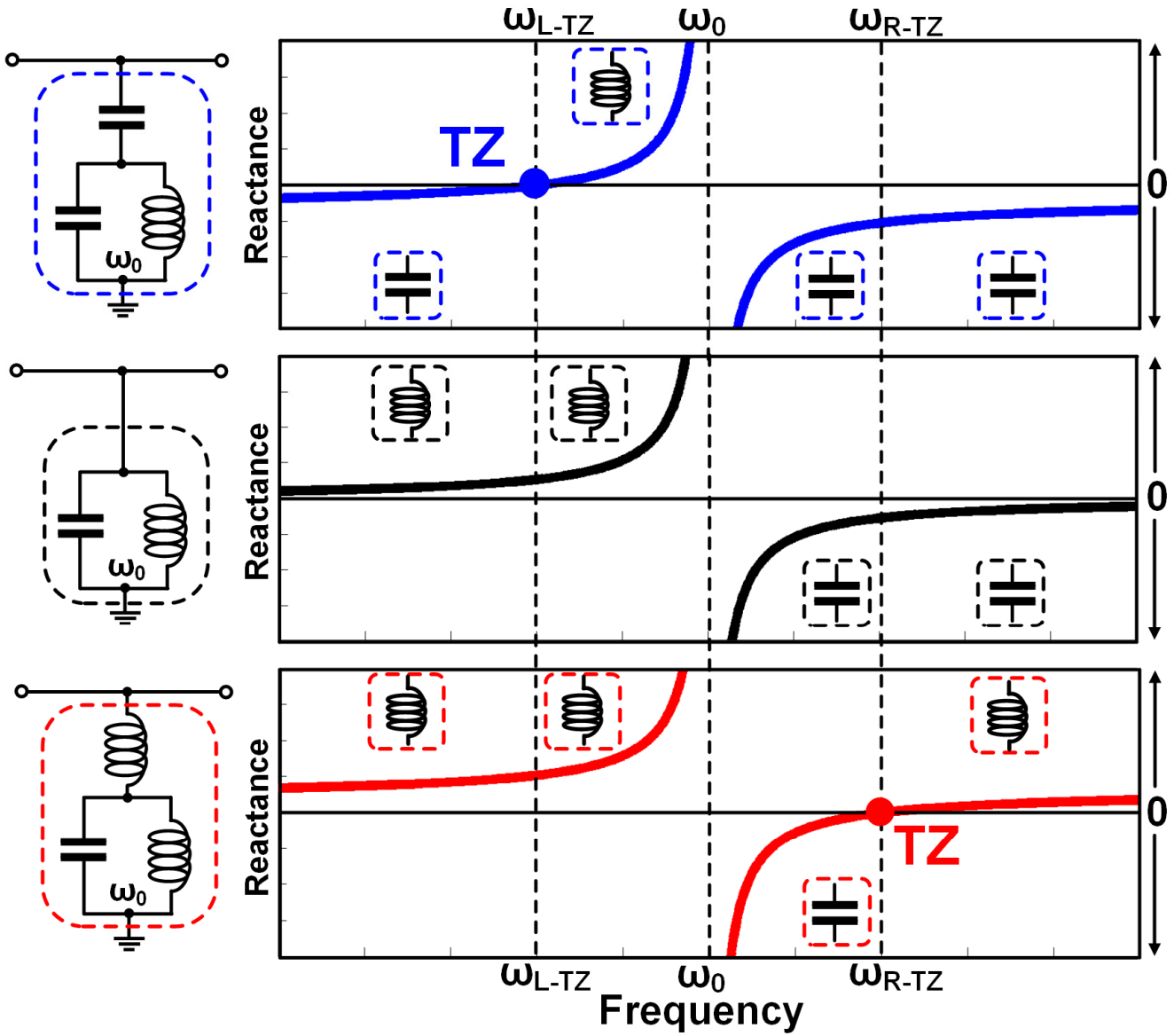
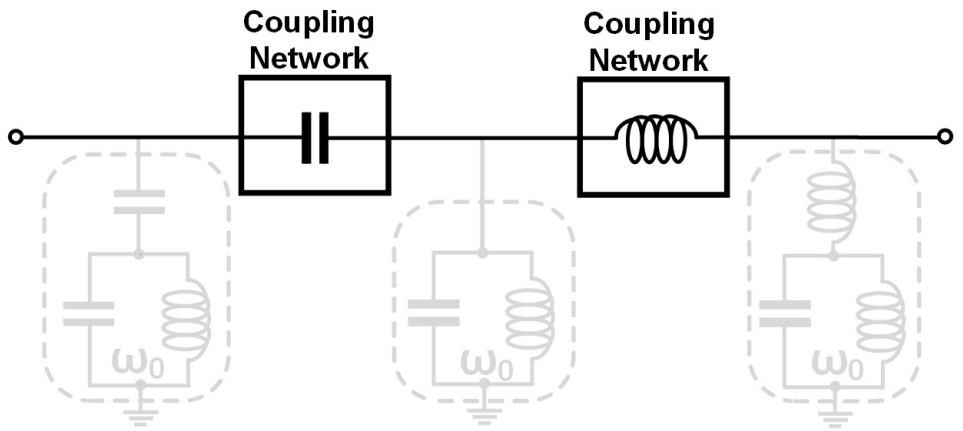
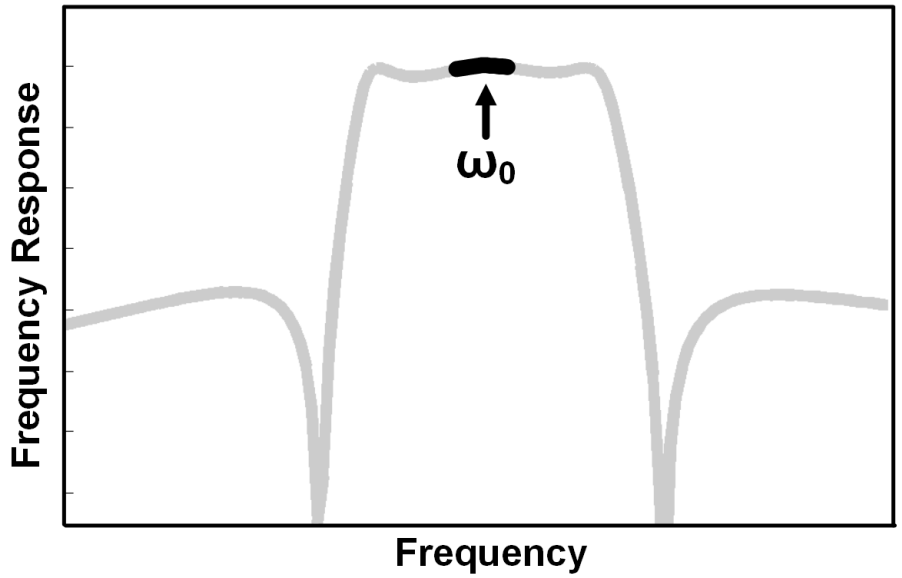
“Anatomy” of LC-Based BPF with TZs







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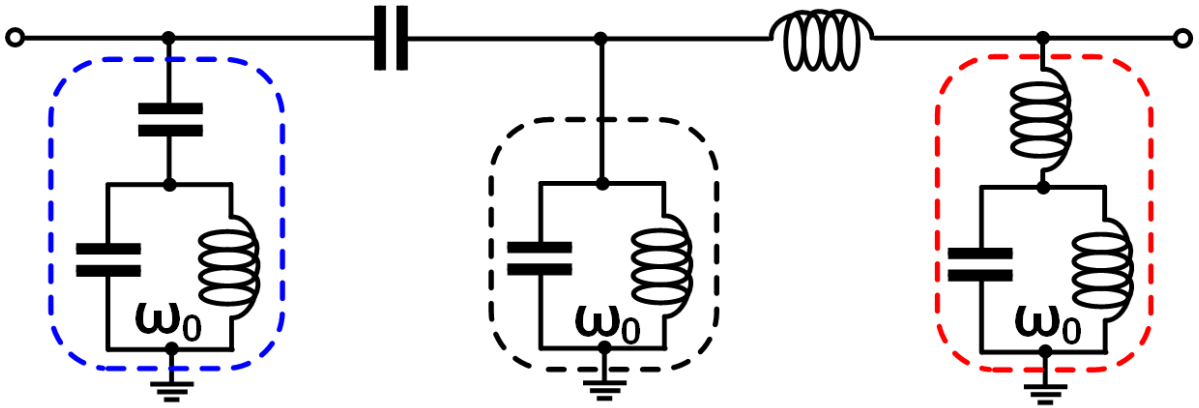
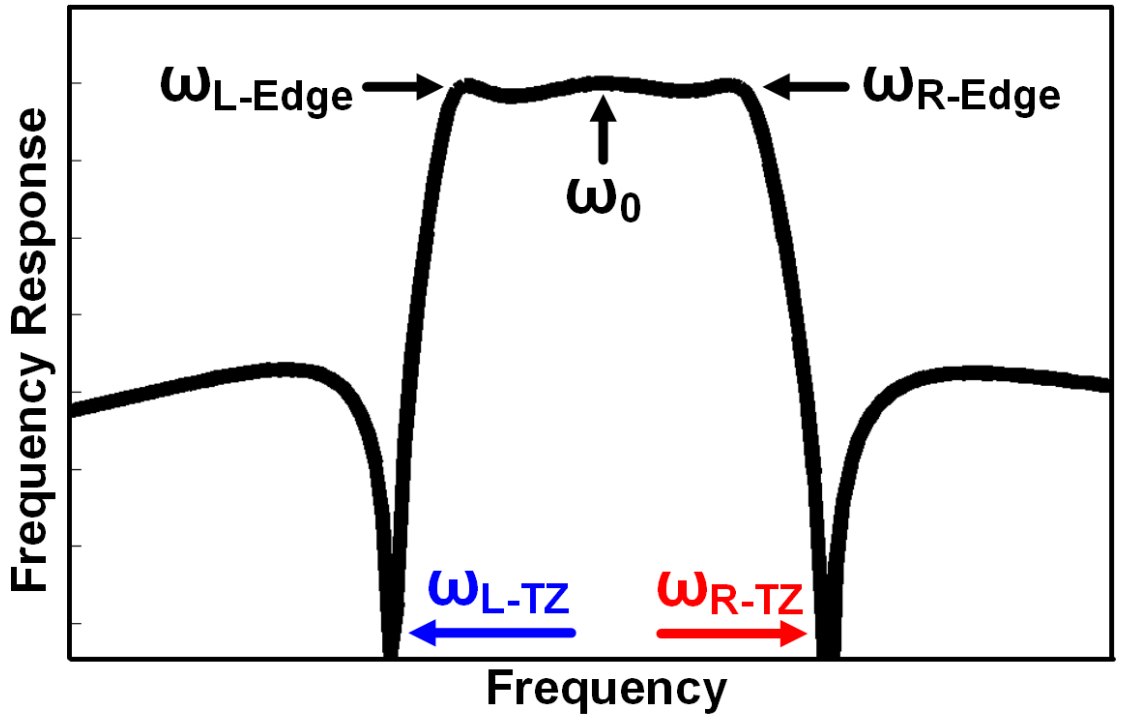
LC-Resonator-Based BPF with TZs





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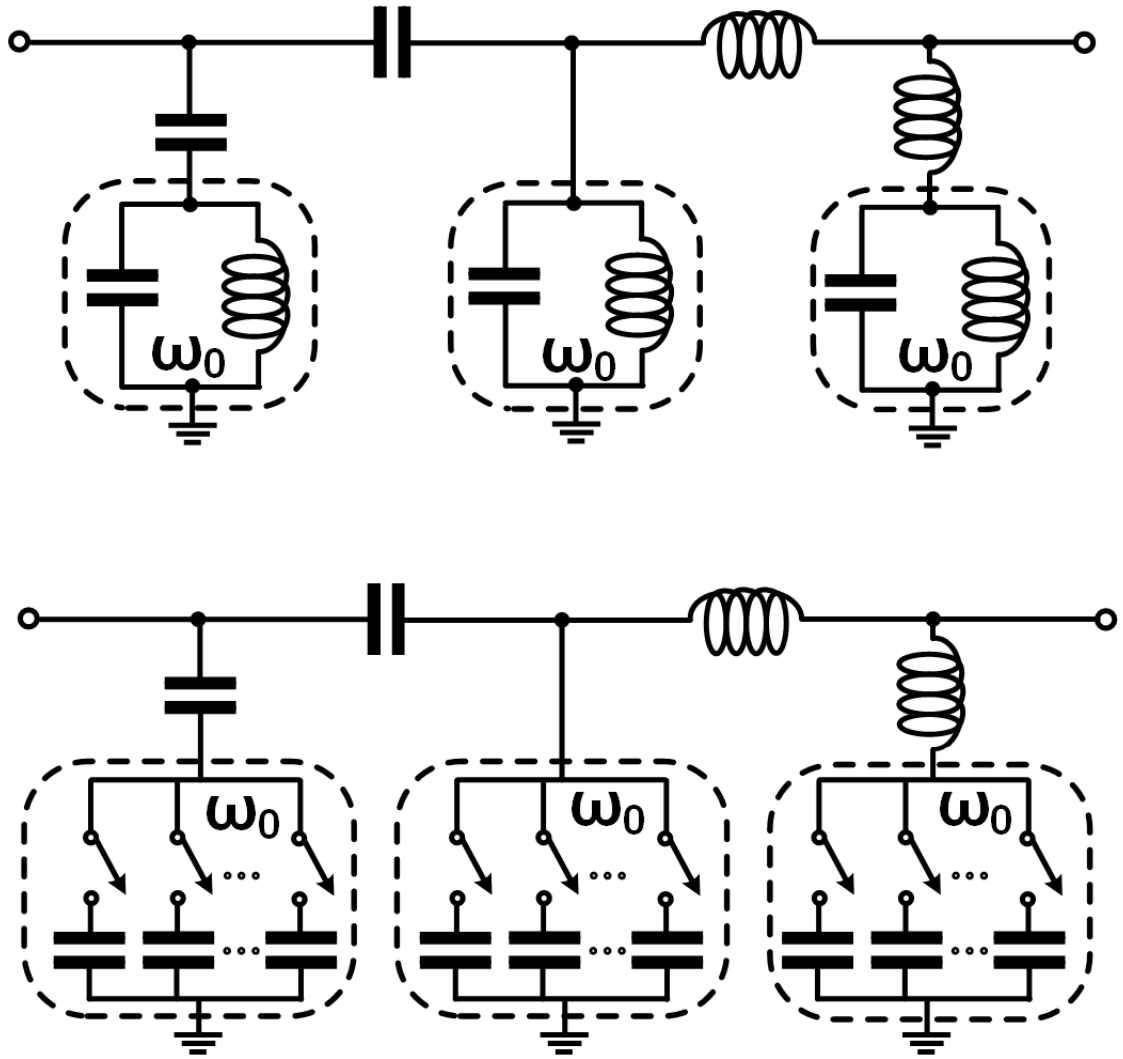
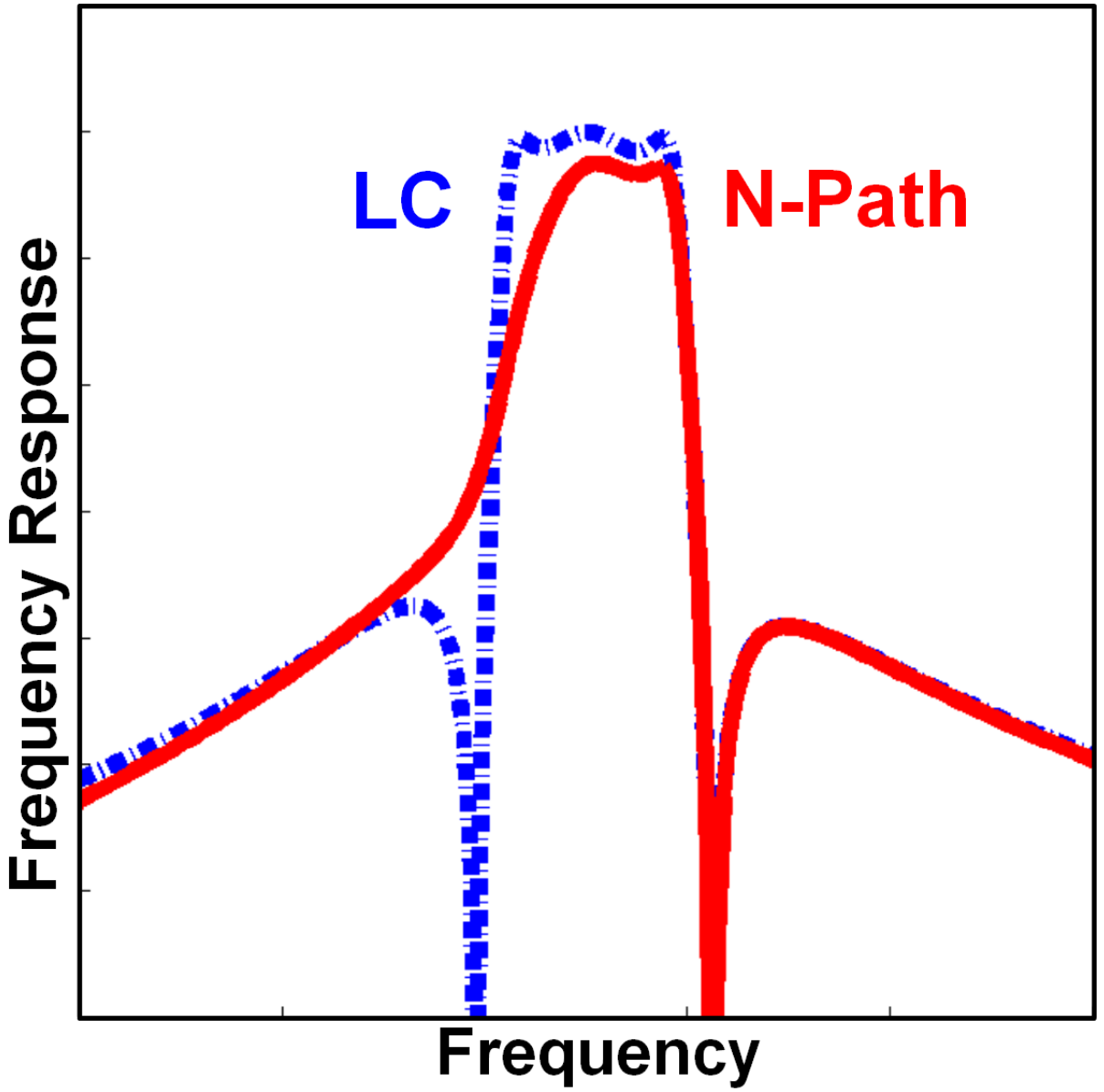
Replacing LC with N-Path Resonators





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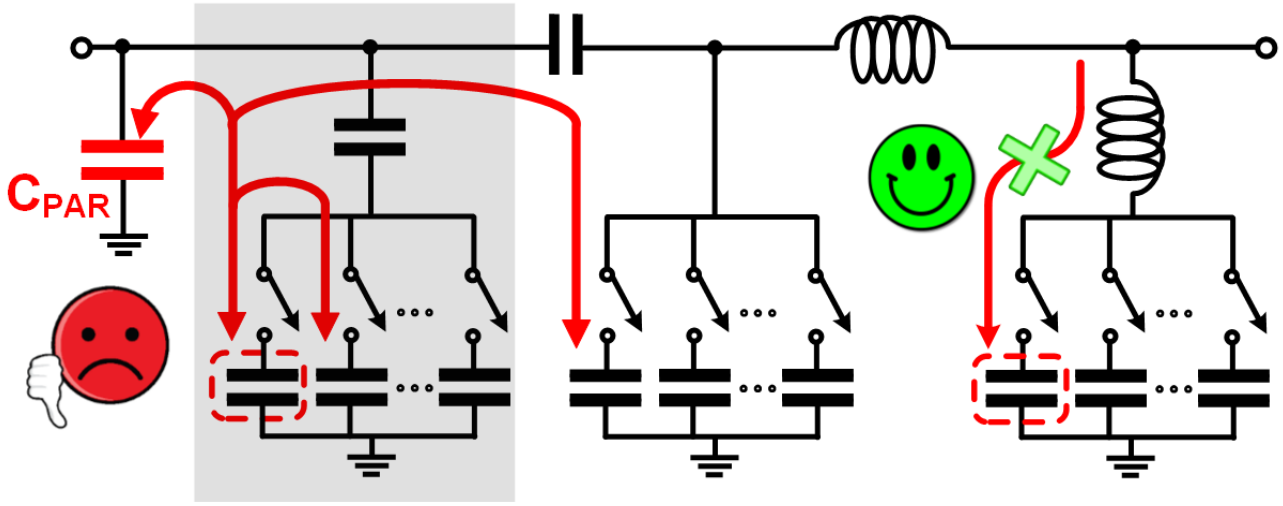
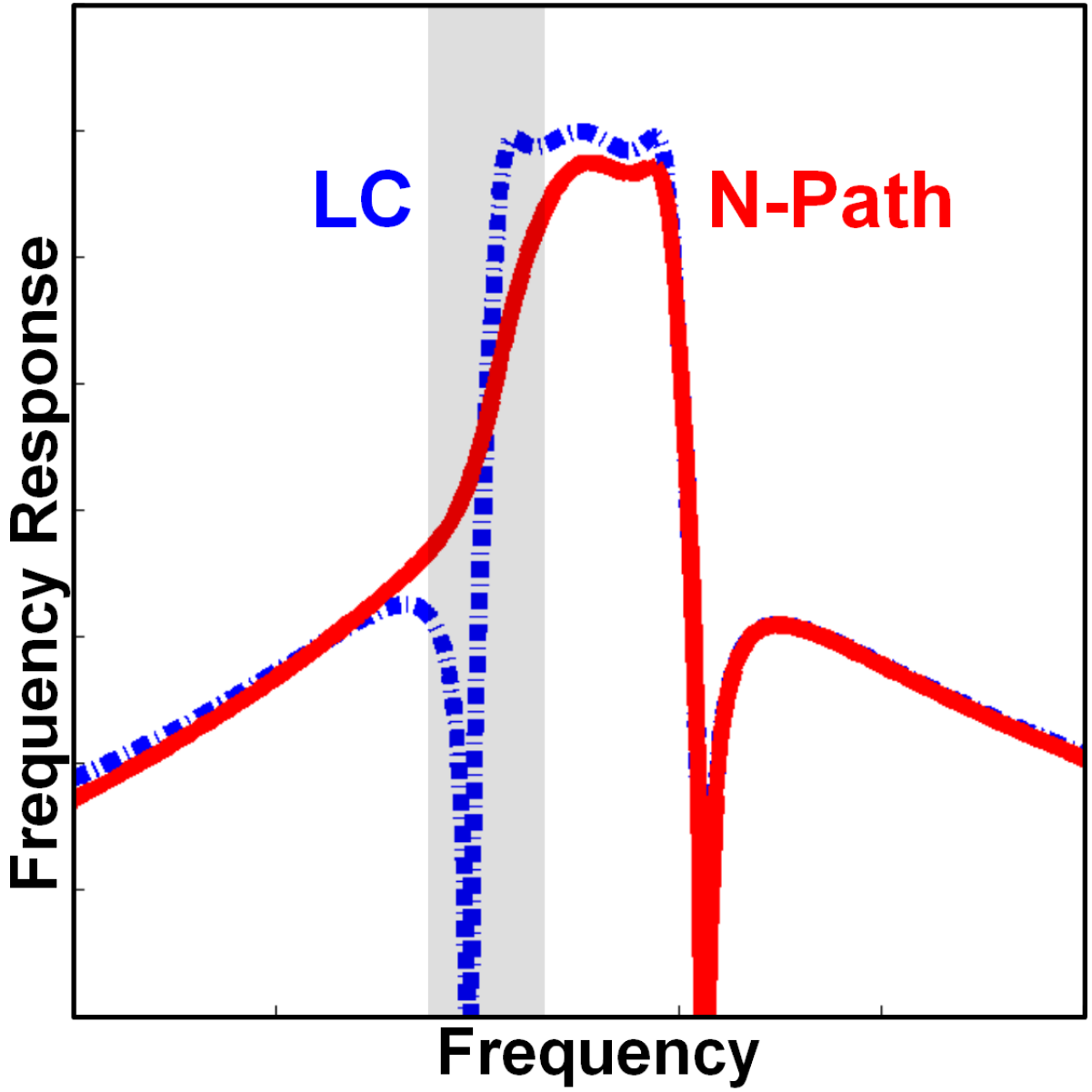
Problem: Unwanted Charge Sharing



[Chen, ISCAS 2016]



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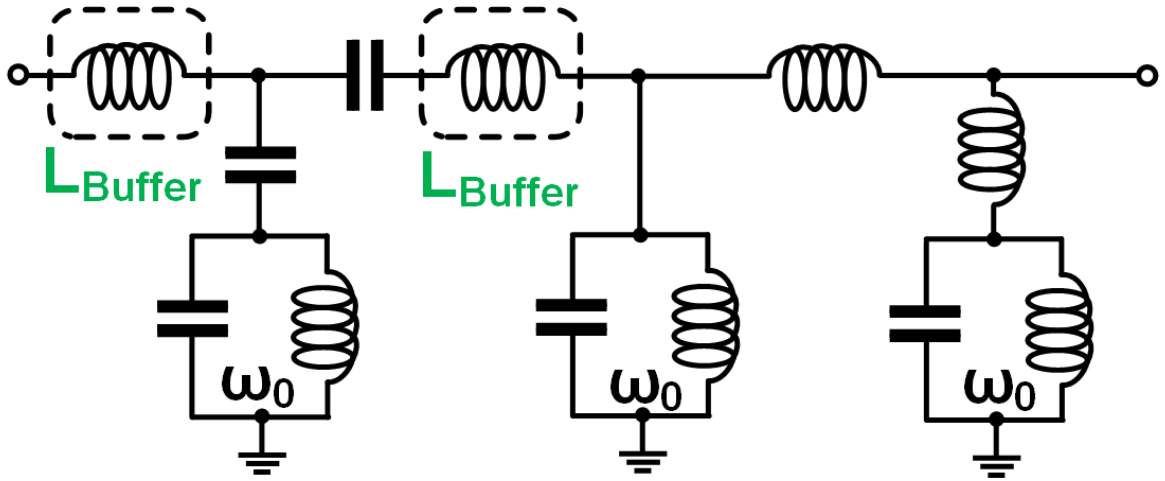
Solution: Add Buffering Inductors



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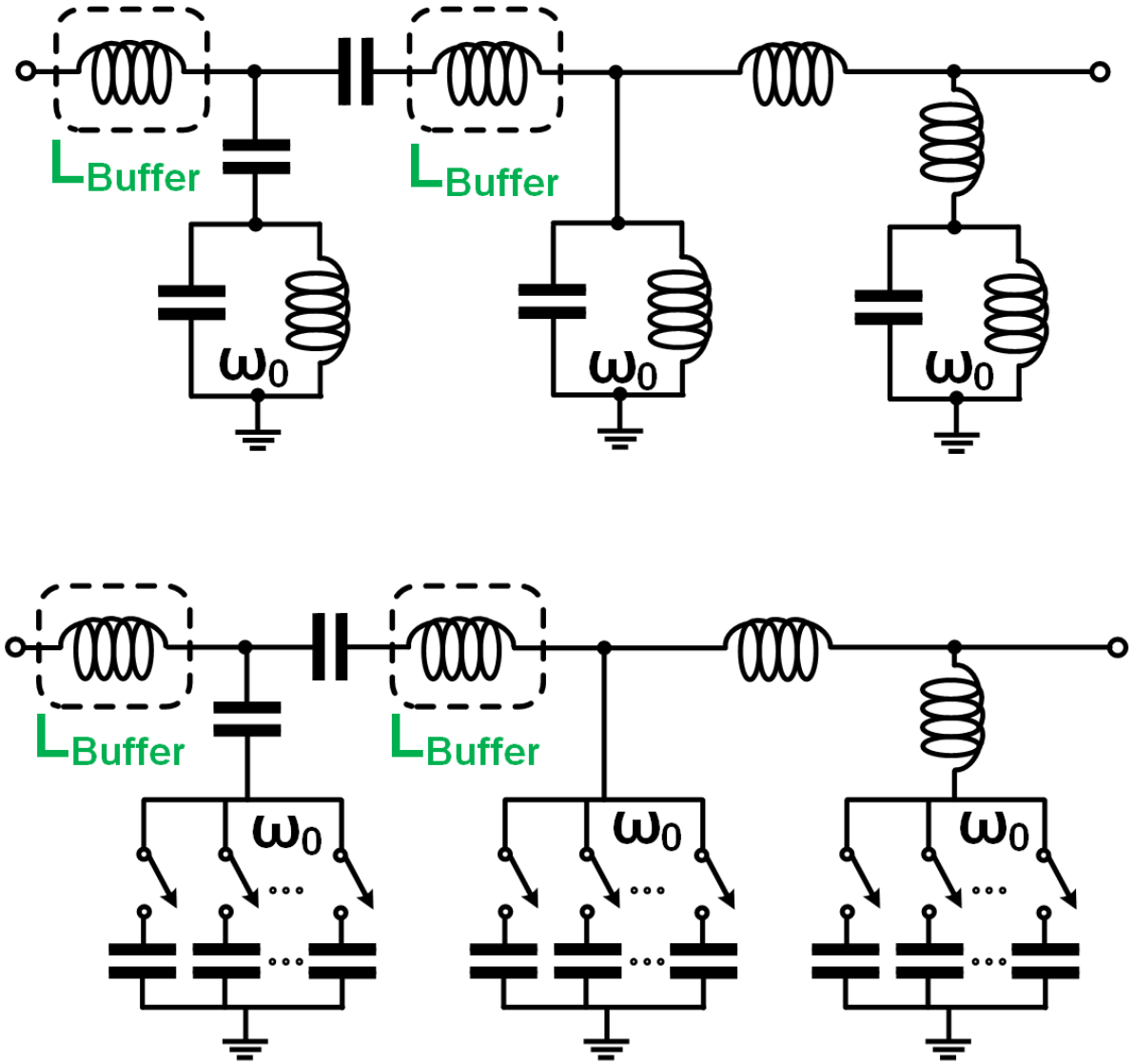
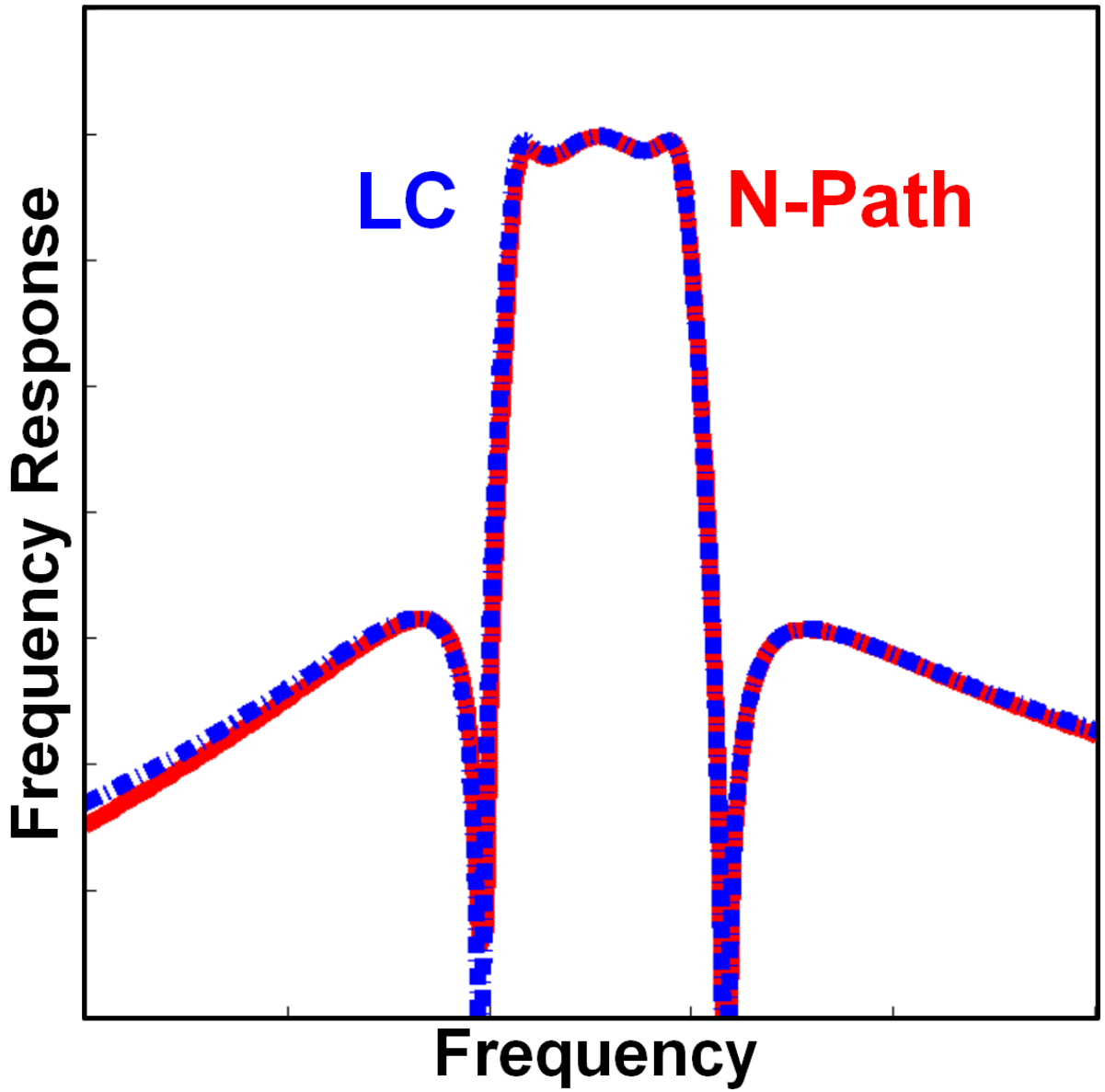
Modified BPF with Buffering Inductors





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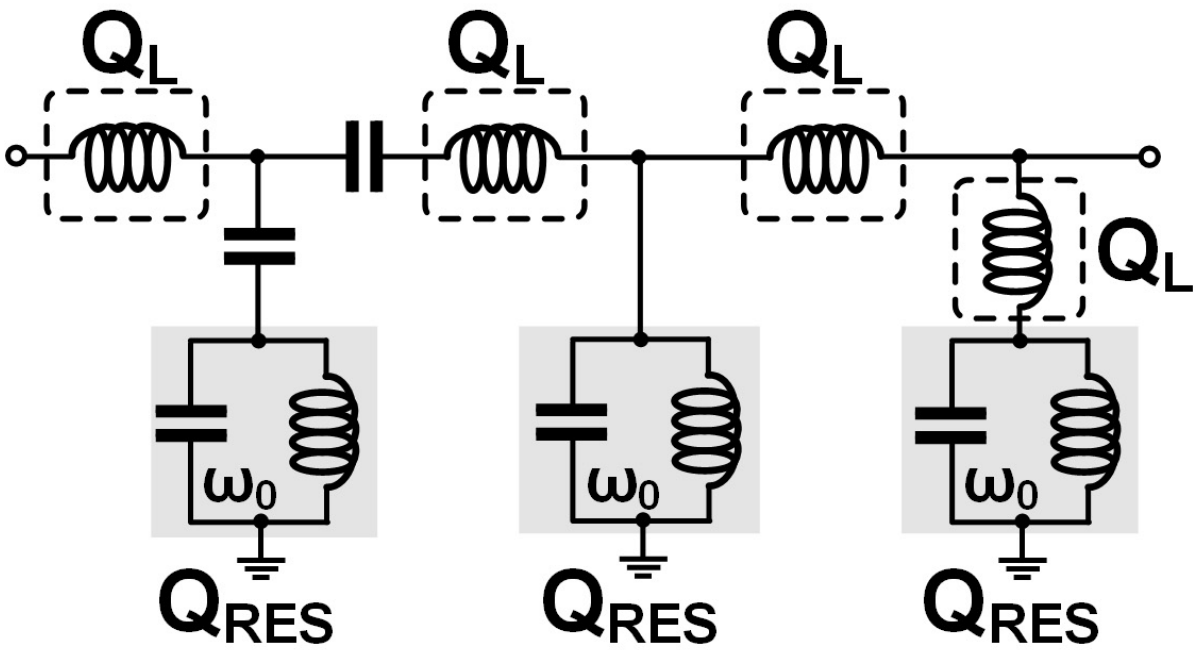
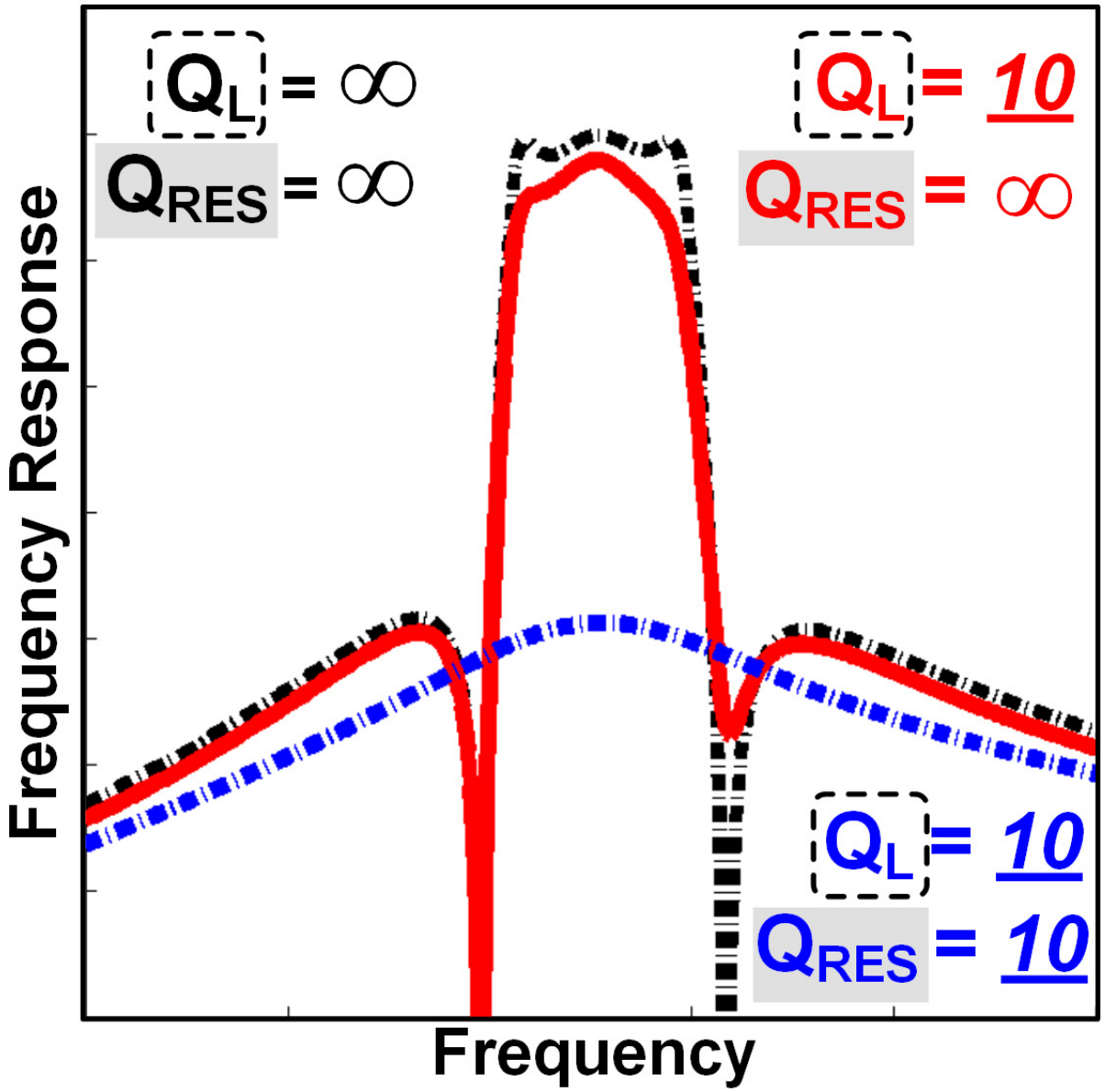
Effects of Inductor and Resonator Q





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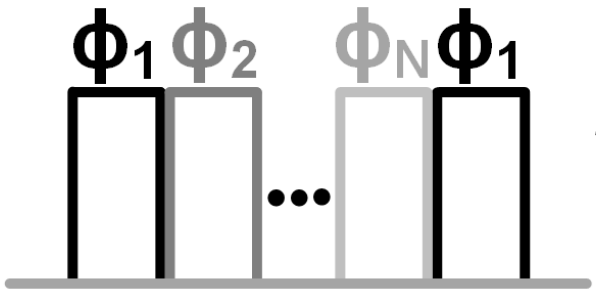
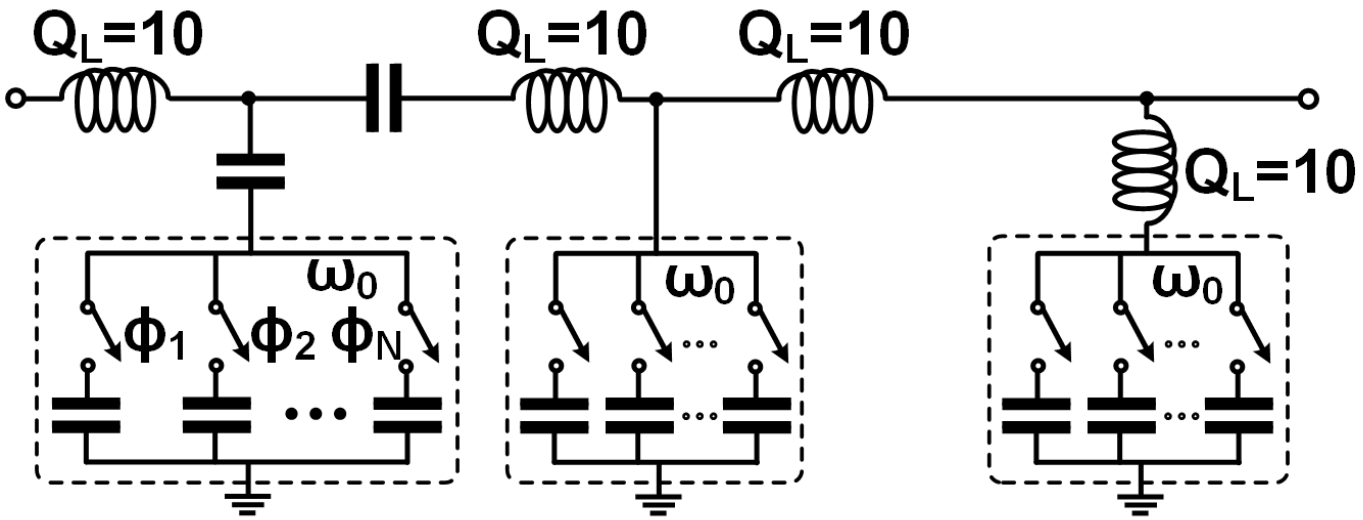
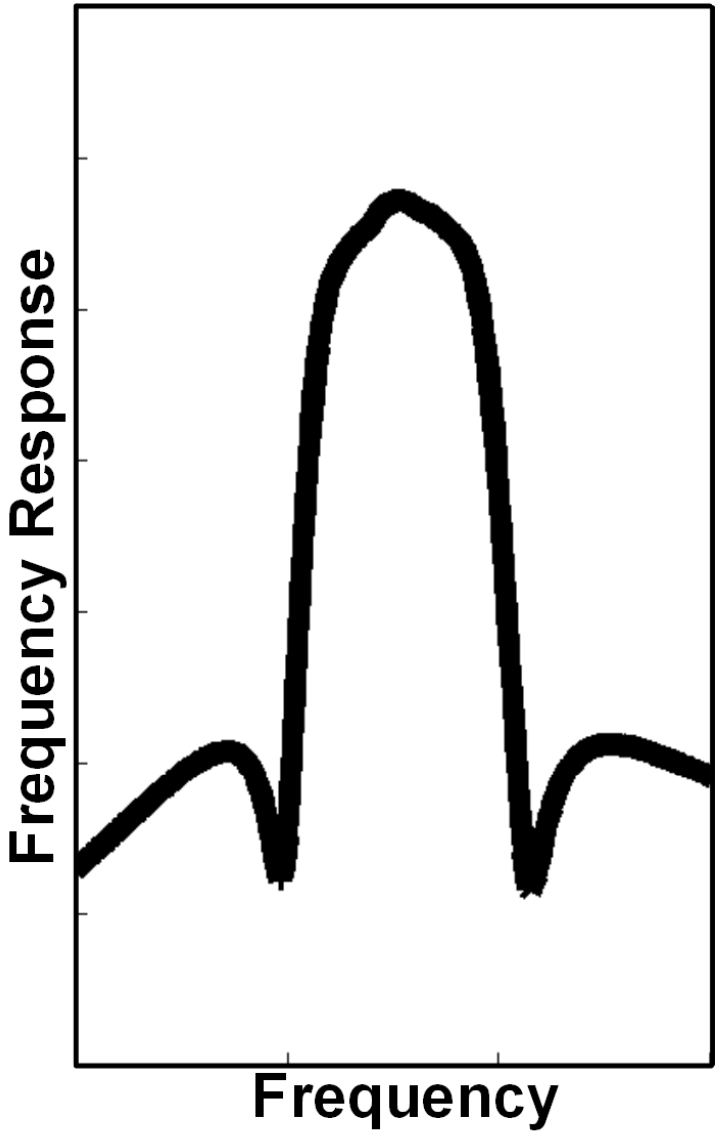
N-Path-Based BPF



Non-Overlapping CLK

Good CLK





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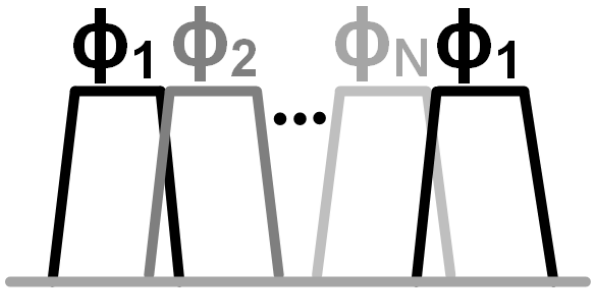
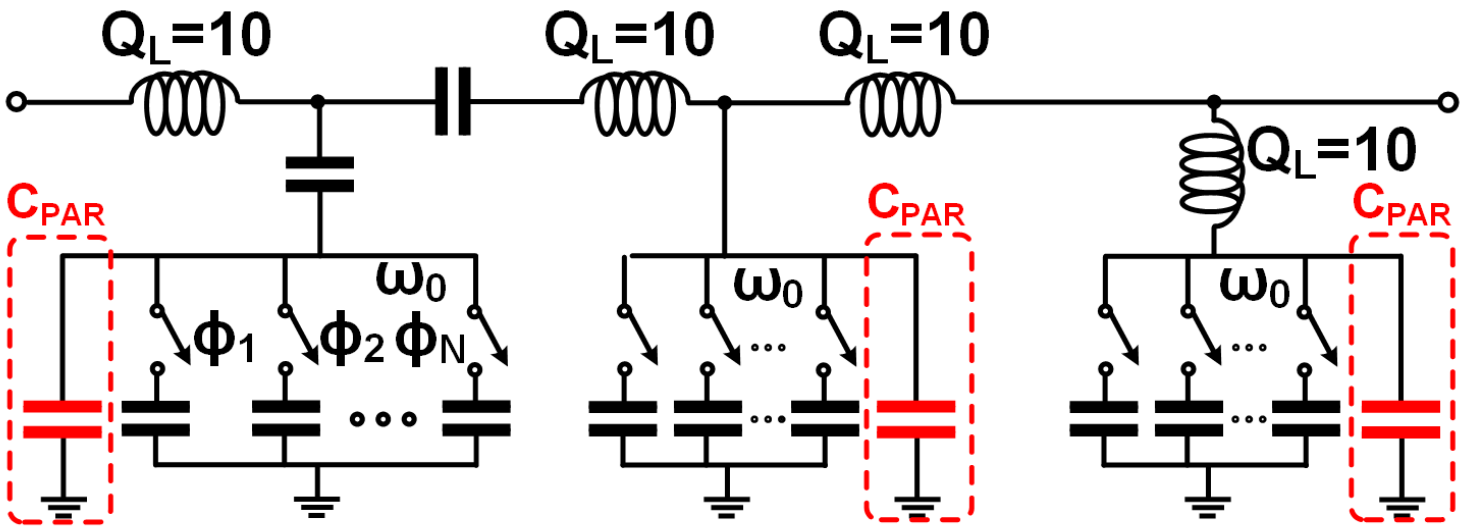
Problem: Clock Phase Overlaps and C_{PAR}

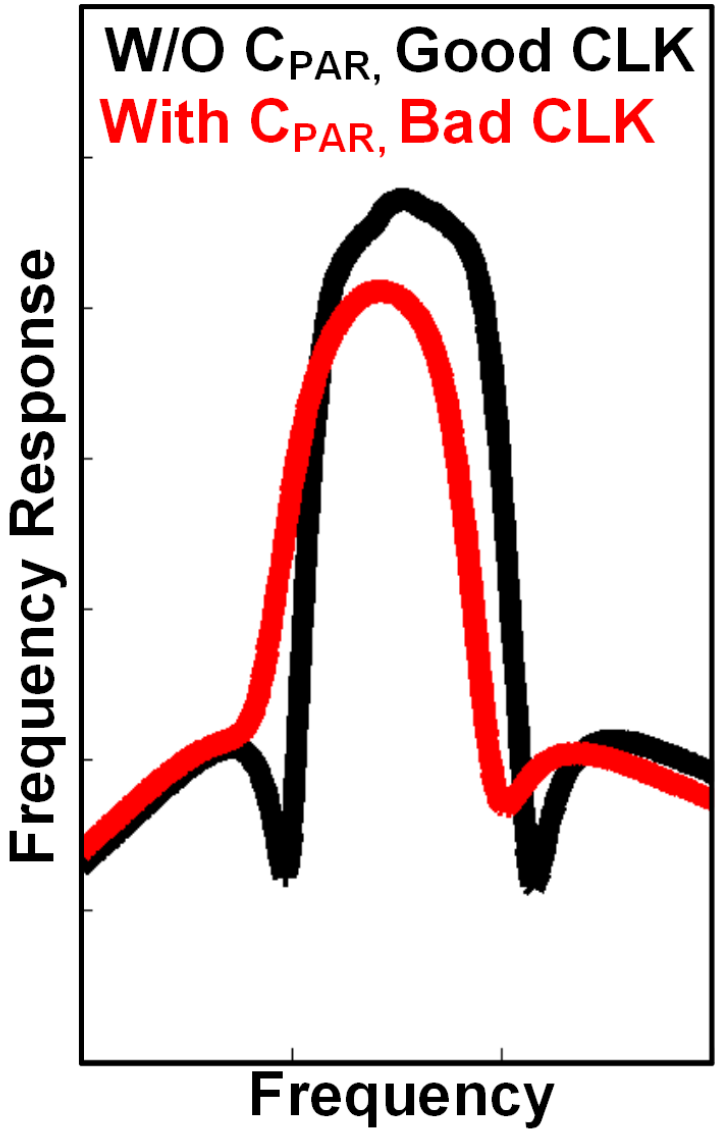


Overlapping CLK

↓

Bad CLK





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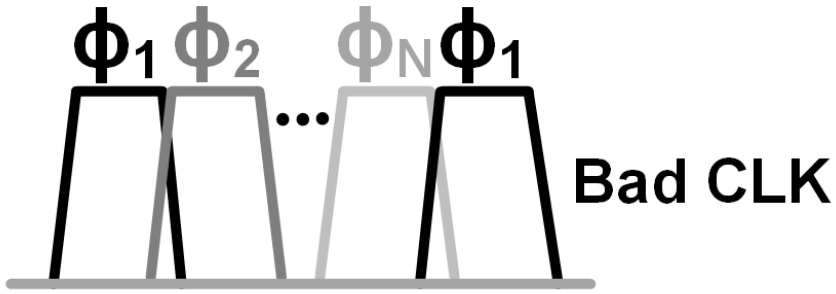
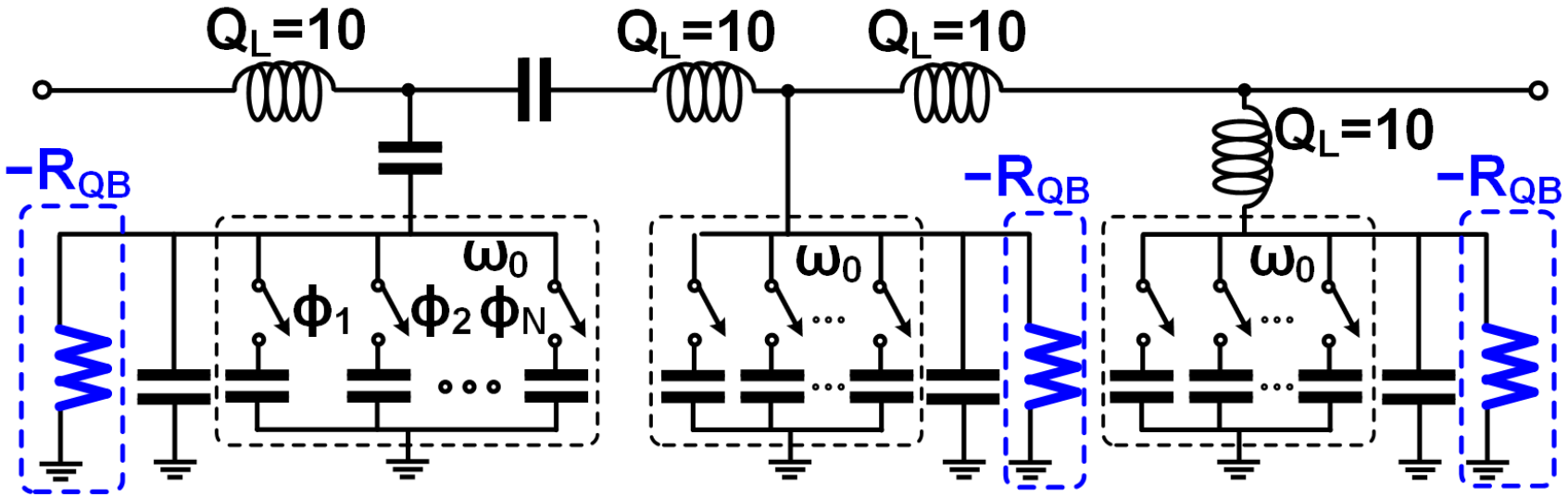
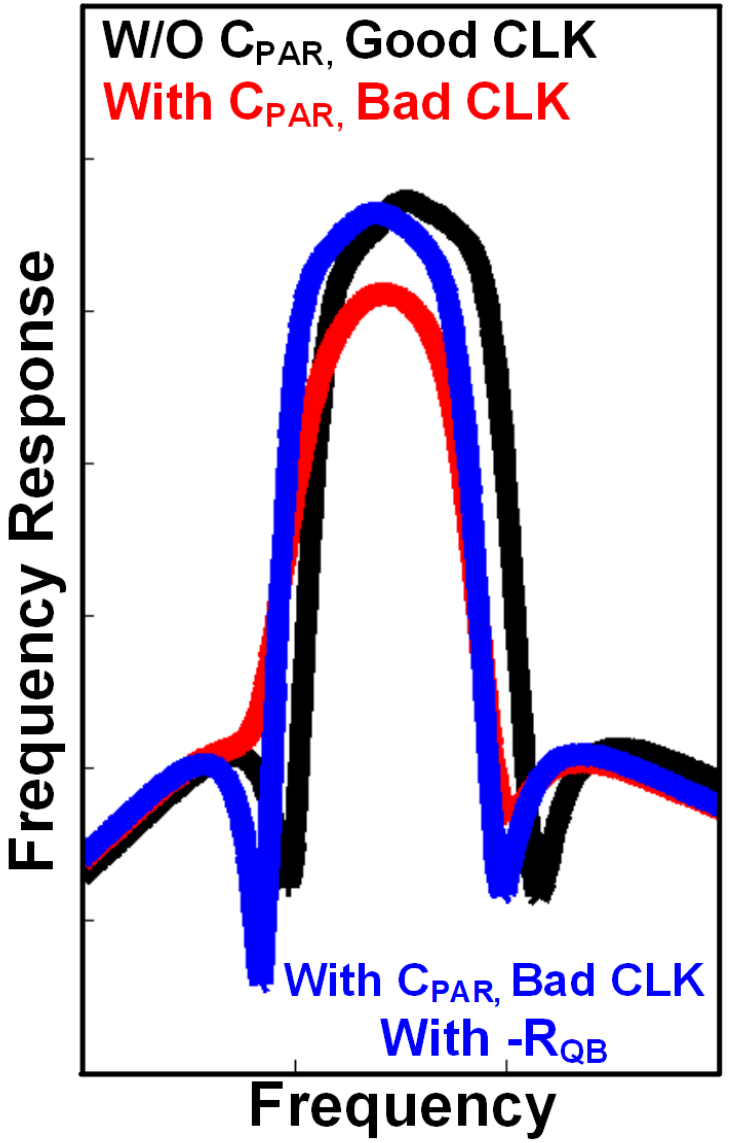
Solution: Add Negative Resistance ($-R_{QB}$)







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Outline

- Radio Frequency Band-Pass Filters
- Switch-Capacitor-Resonator-Based RF BPF Synthesis
- **Circuit Implementation and Measurement Results**
- Conclusion

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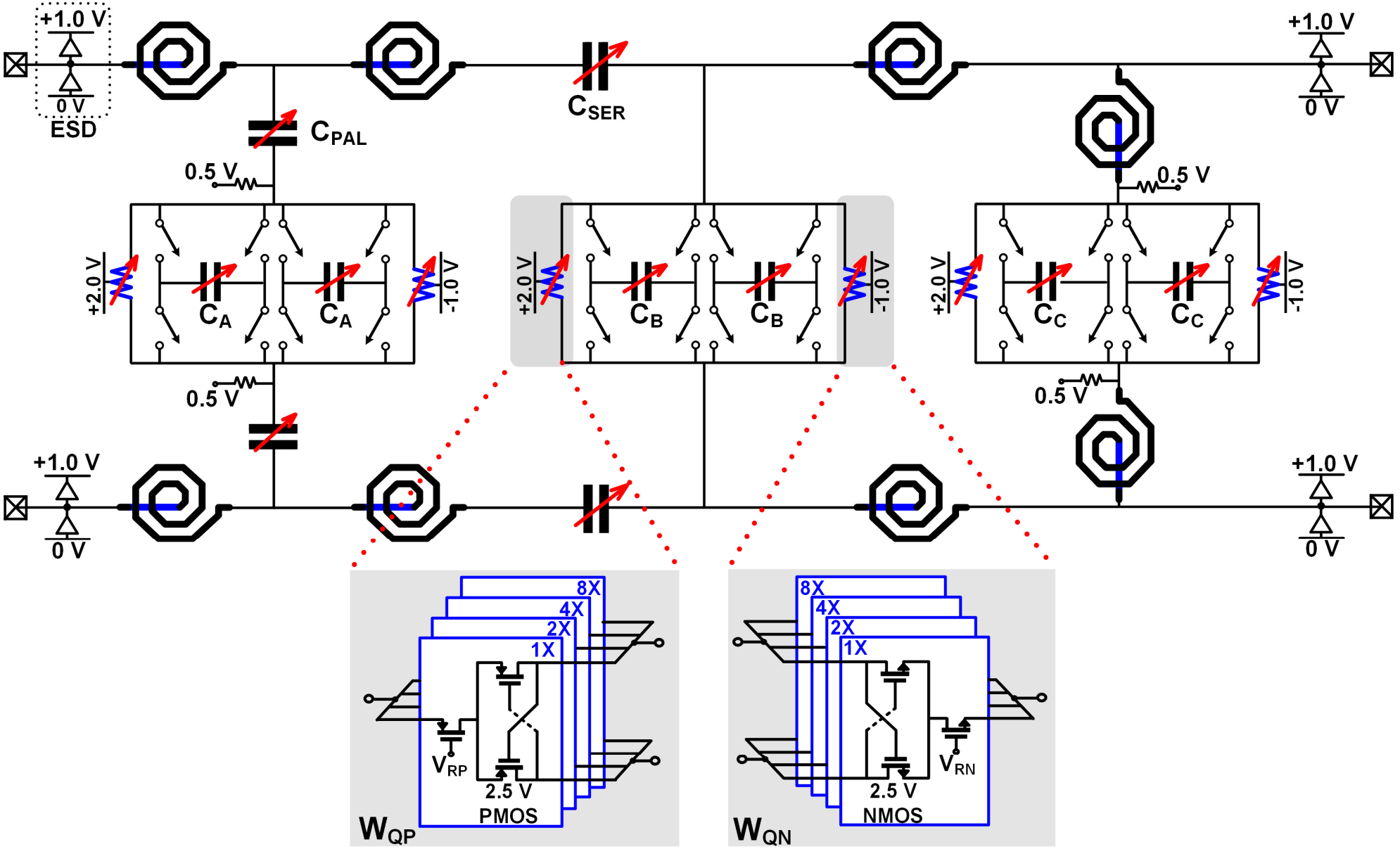
Differential N-Path-Based BPF Schematic



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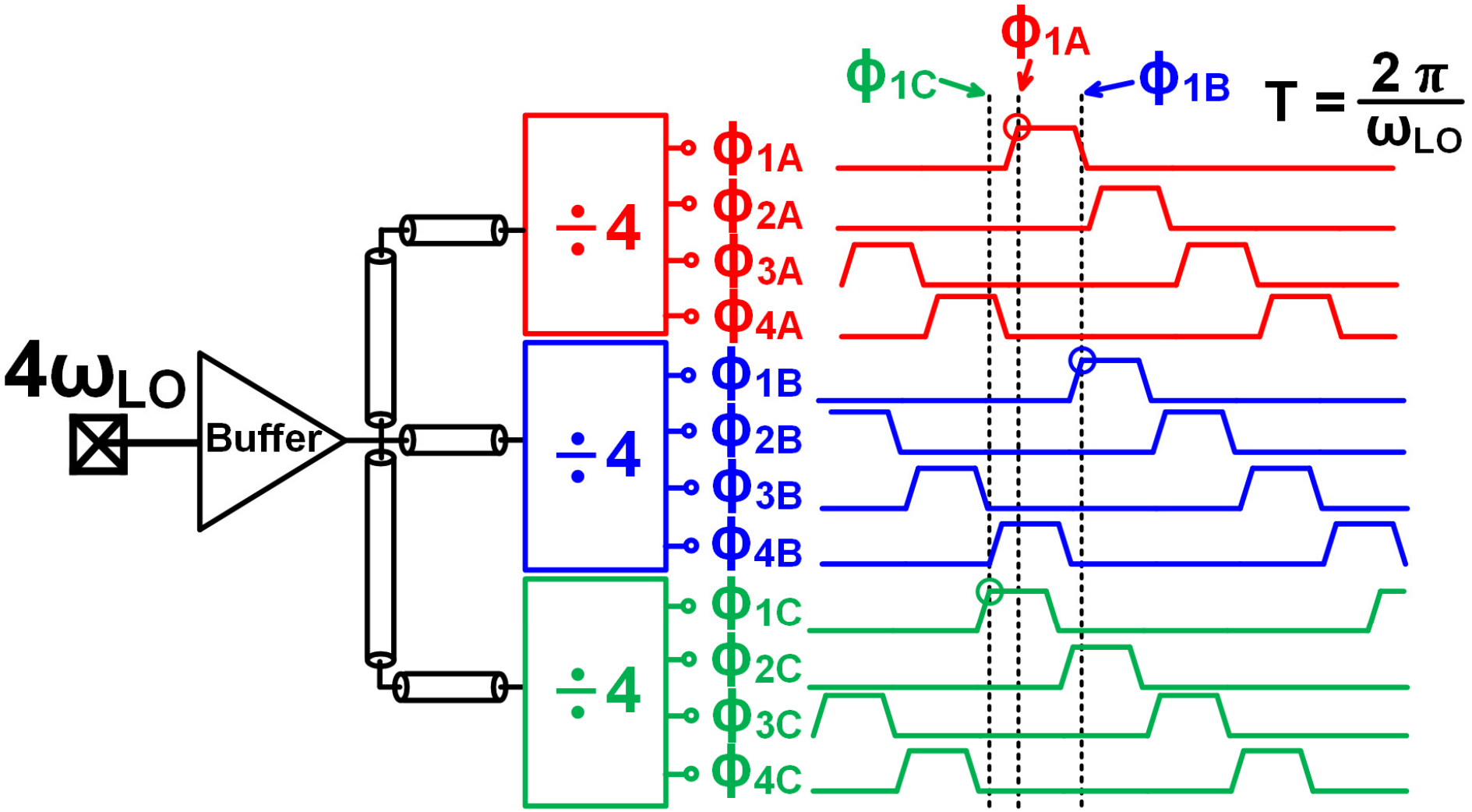
Clock Generation for N-Path Resonators



N-Path Resonators are Decoupled

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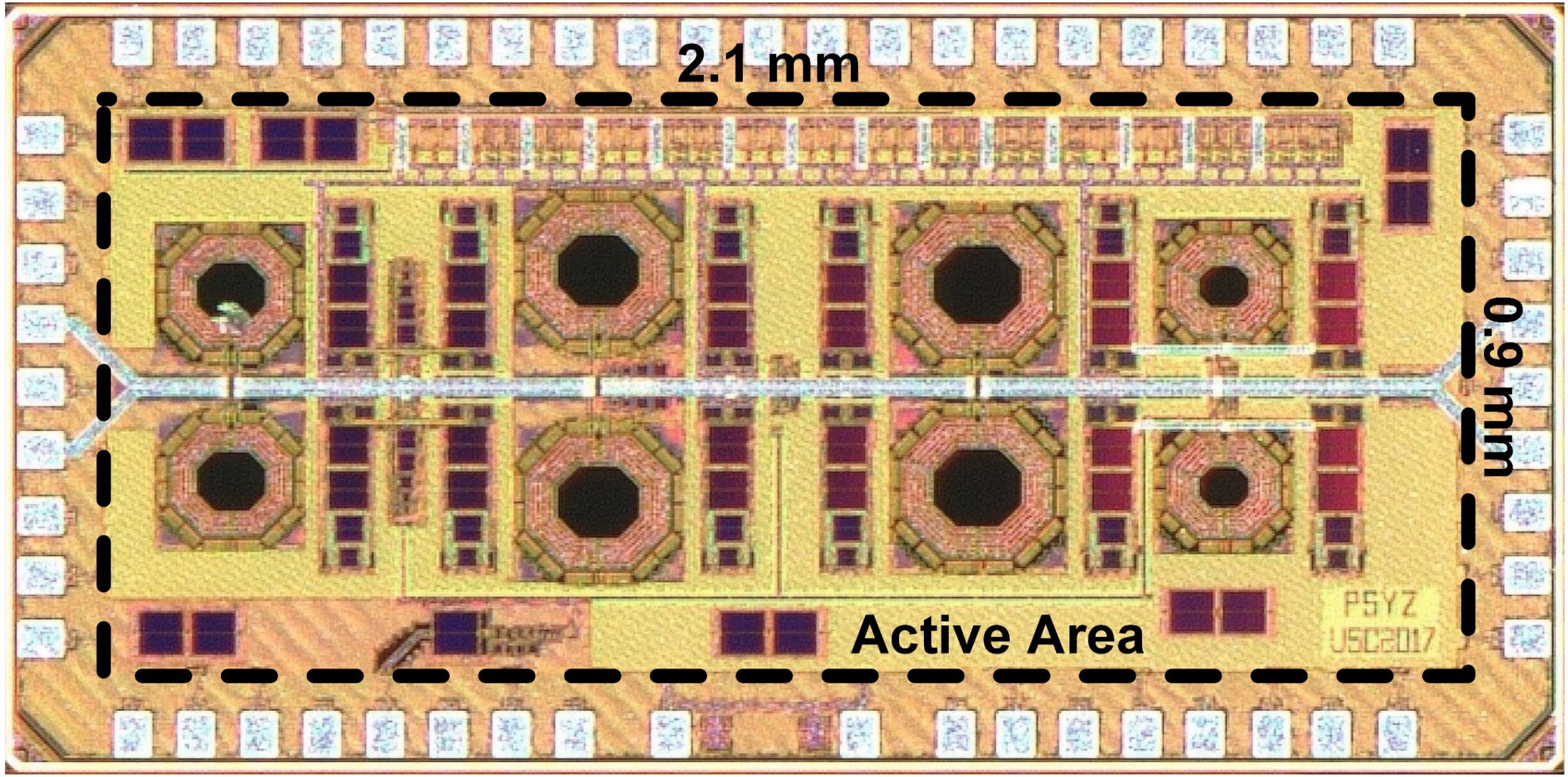
65 nm CMOS Chip



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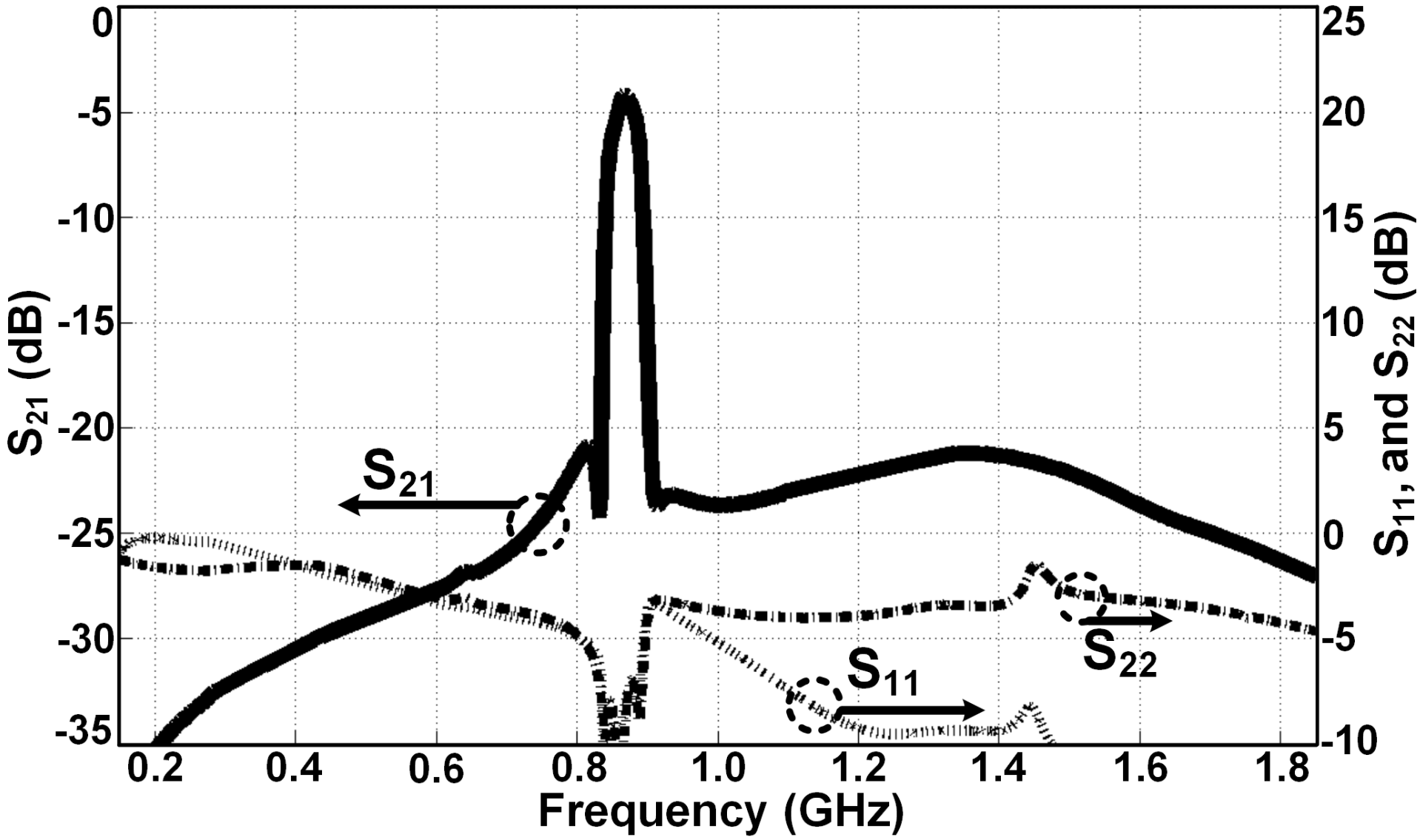
Representative Small-Signal Measurement



f_{LO}	875	CLK Freq. (MHz)
C_A	20	Main Cap. (pF)
C_B	32	
C_C	28	
W_{QN-A}	14	X-Pair NMOS Width (um)
W_{QN-B}	3	
W_{QN-C}	3	
$W_{QP} = 2.5W_{QN}$		PMOS Width
C_{PAL}	3.2	Coupling Cap. (pF)
C_{SER}	1.9	
P	82	Power (mW)

BW_{-3dB} = 40 MHz

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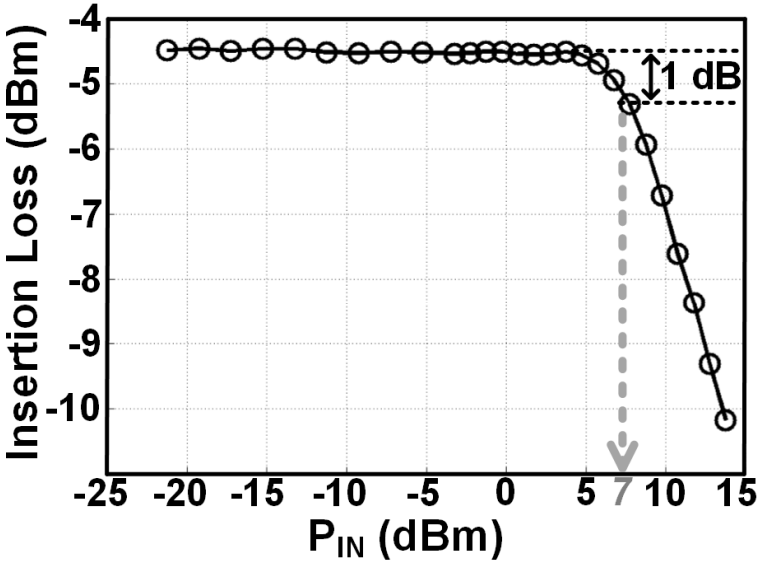
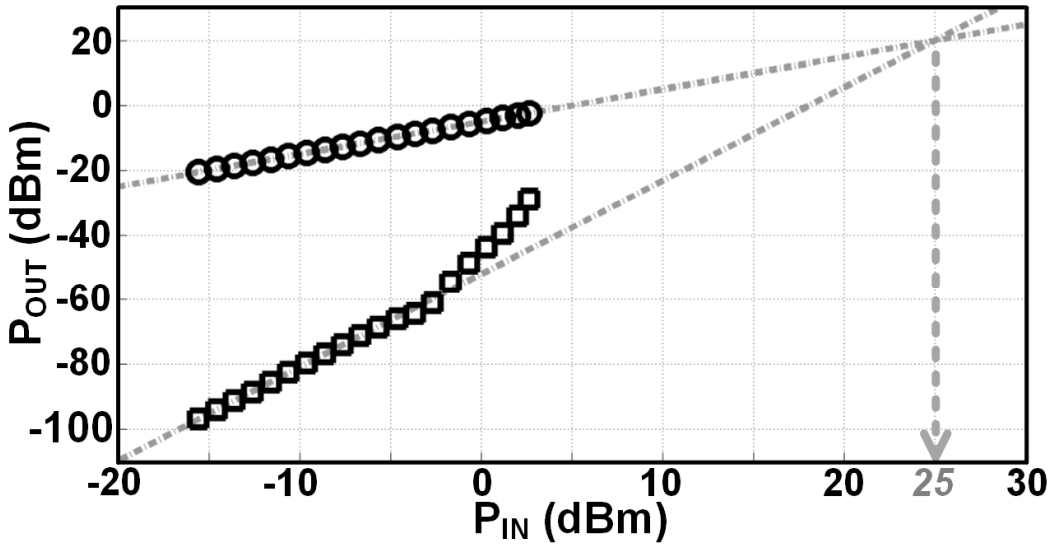
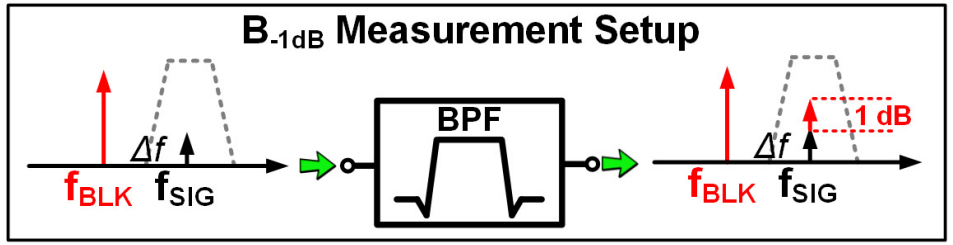
Corresponding Large-Signal Measurements

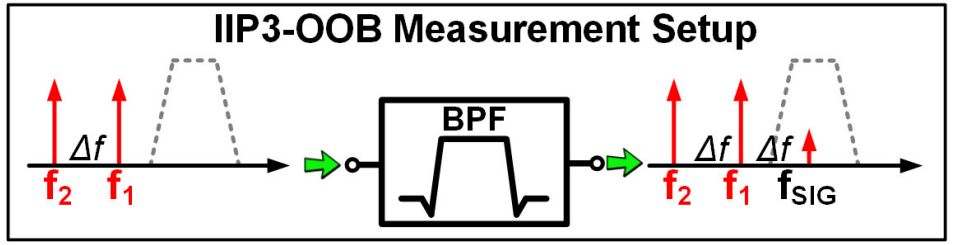
In-Band Linearity

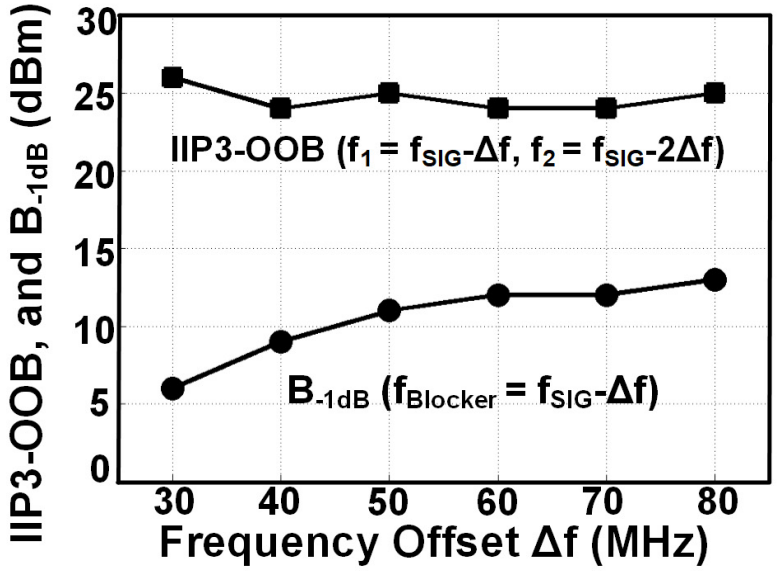




Out-Of-Band Linearity







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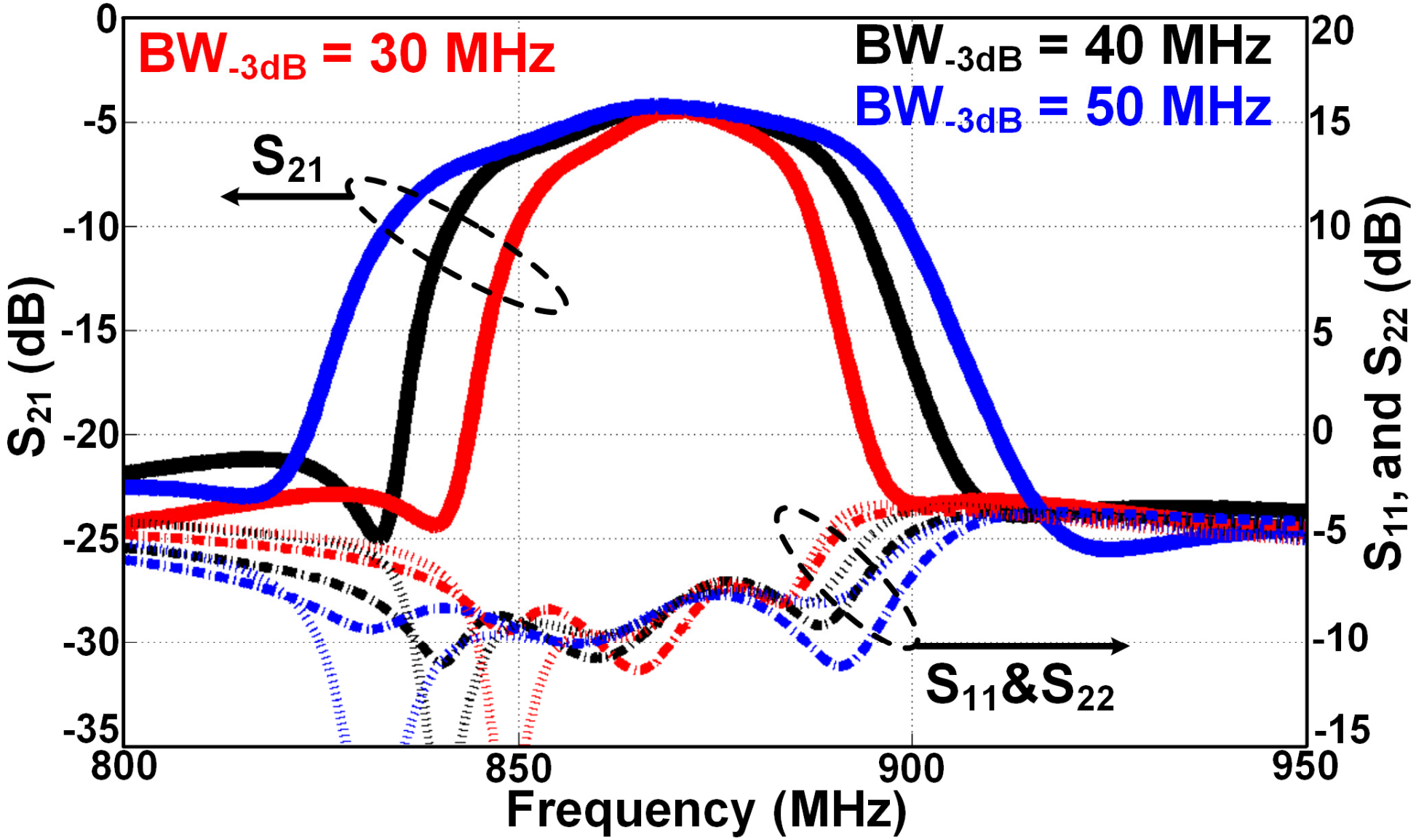
Representative BPFs with Different Bandwidths



f_{LO}	875	875	875
C_A	28	20	16
C_B	44	32	28
C_C	44	28	20
W_{QN-A}	14	14	14
W_{QN-B}	2	3	2
W_{QN-C}	3	3	4
$W_{QP} = 2.5W_{QN}$			
C_{PAL}	3.8	3.2	3.8
C_{SER}	1.9	1.9	2.0
P	80	82	82

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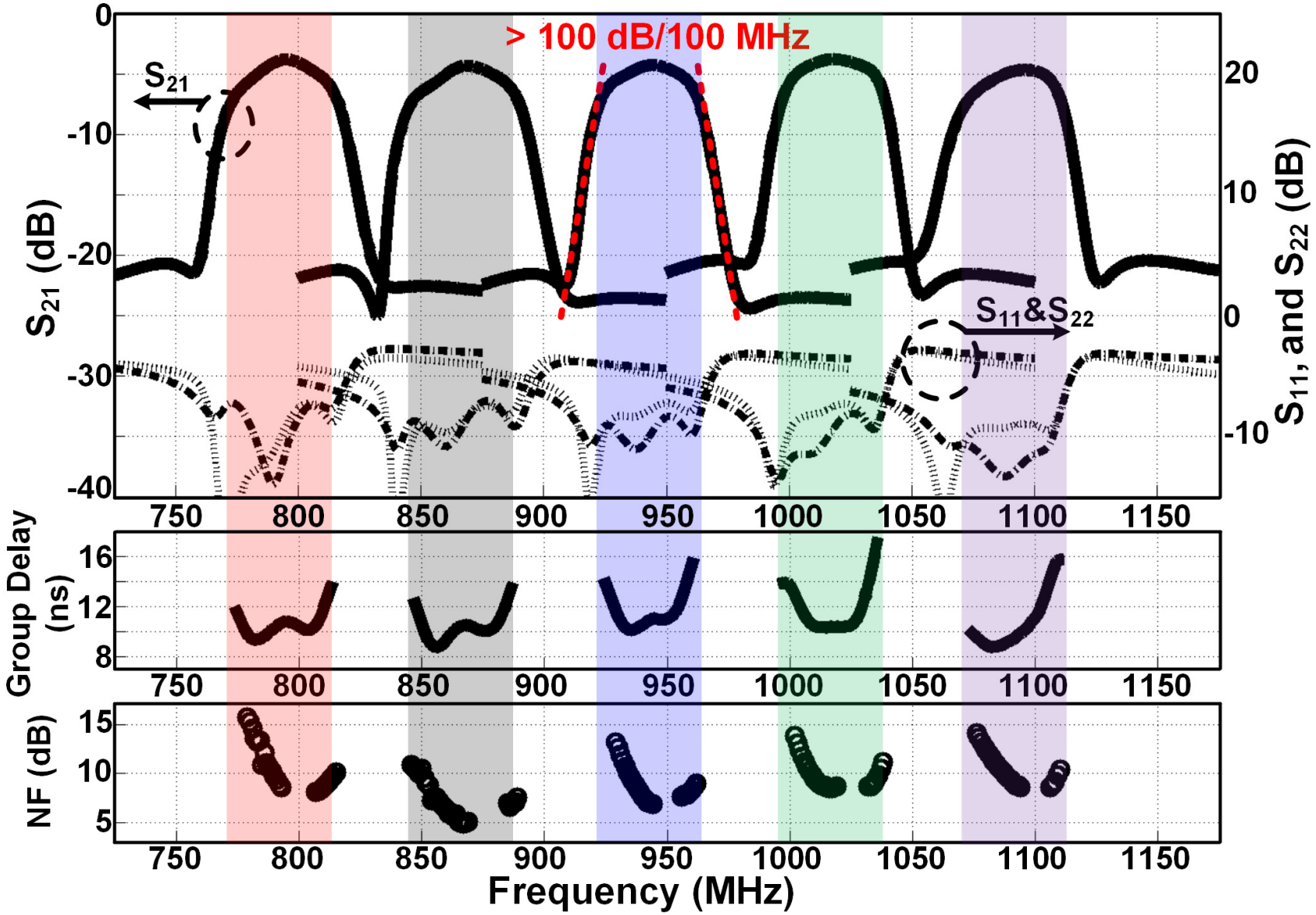
Representative BPFs with Different Center Freq.



f_{LO}	800	875	950	1025	1100
C_A	20	20	24	24	20
C_B	32	32	32	24	24
C_C	32	28	28	28	28
W_{QN-A}	13	14	14	14	14
W_{QN-B}	2	3	2	4	2
W_{QN-C}	4	3	3	4	3
$W_{QP} = 2.5W_{QN}$					
C_{PAL}	4.0	3.2	3.6	3.4	3.0
C_{SER}	2.4	1.9	1.6	1.3	1.2
P	80	82	86	97	92

All Filter Shapes BW_{-3dB} = 40 MHz

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Performance Summary

	RFIC 2016 R. Chen	JSSC 2016 Y. Xu	ISSCC 2017 Y. Lien	RFIC 2017 G. Qi	ISSCC 2017 S. Hameed		This Work
Technology	65nm CMOS	40nm CMOS	28nm CMOS	180nm CMOS SOI	65nm CMOS		**65nm CMOS**
Topology	N-Path	Charge-Domain Filtering	N-Path	N-Path+LNA	Filtering by Aliasing		**N-Path**
Tuning Range (GHz)	0.5 - 1.1	0.1 - 0.7	0.1 - 2.0	0.7 - 1.0	0.1 - 1.0		**0.8 - 1.1**
Filter Order	4	1 - 4	5	8	NA		**13**
Transmission Zero	No	No	No	Yes	Yes		**Yes**
Roll-Off Slope (dB/ 100 MHz)	15 *	98 *	18.3 *	120 *	49 *	800 *	**100**
BW_{3dB} (MHz)	30	3.2 - 4.8	13	8 *	40	2.5	**30 - 50**
ICP_{-1dB} (dBm)	5	-27 *	-6 *	NA	-7 *		**7**
B_{-1dB} (dBm)	11	15 (Δf/BW= 6.2)	13 (Δf/BW= 6.2)	8 (Δf/BW= 5.0)	9.5 (Δf/BW= 2.0) 13 (Δf/BW= 4.0)		**9 (Δf/BW=1.0)**
IIP3-IB (dBm)	19.2	NA	5	NA	8		**25**
IIP3-OOB (dBm)	26	24 (Δf/BW= 6.2)	44 (Δf/BW= 6.2)	32.3 (Δf/BW= 5.0)	21 (Δf/BW= 1.2)		**24 (Δf/BW=1.0)**
NF (dB)	3.8 - 5.8	6.8 - 9.7	4.1 - 10.5	5.5 - 6.4	7		**5.0 - 8.6**
Power (mW)	15 - 25	59 - 105	38 - 96	42 - 57	64 - 84		**80 - 97**
Active Area (mm^2)	0.50 *	2.03	0.49	2.2	2.3		**1.9**

* Estimated from figures

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Conclusions

- Reconfigurable RF BPFs with controllable transmission zeros utilizing N-path resonators (high Q), inductors (low Q), and capacitors can be synthesized.

- A 13th-order N-path-resonator-based RF BPF is demonstrated in 65 nm CMOS.

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  - NSF under the EARS program

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A Fully Integrated 128-pixel 0.56 THz Sensing Array for Real-Time Near-Field Imaging in 0.13µm SiGe BiCMOS

Philipp Hillger[1], Ritesh Jain[1], Janusz Grzyb[1], Laven Mavarani[1], Bernd Heinemann[2], Gaetan Mac Grogan[3], Patrick Monaix[4], Thomas Zimmer[5], Ullrich R. Pfeiffer[1]

[1] IHCT, University of Wuppertal, Germany
[2] IHP, Frankfurt (Oder), Germany
[3] Institut Bergonié, Bordeaux, France
[4] CNRS, Talence, France
[5] University of Bordeaux, Talence, France

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Outline

- Motivation
- Sensing concept
- THz near-field sensing SoC
  - ➢ Circuit design and simulations
  - ➢ Measurement results
  - ➢ Imaging results
- Conclusions

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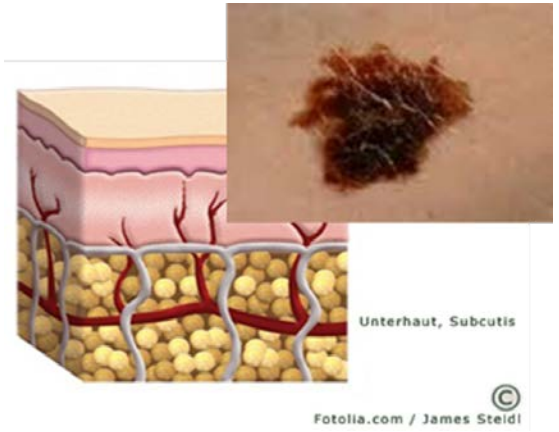
Motivation

μm-scale resolution permittivity imaging

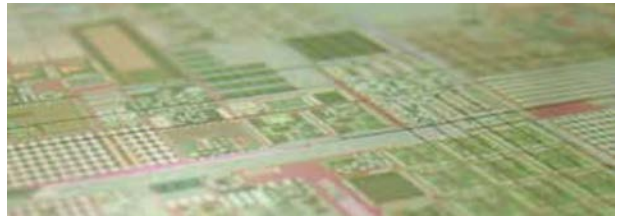
Biomedicine



Industry

Art

Semiconductors



low-cost + ease of use + high sensitivity

many untapped applications

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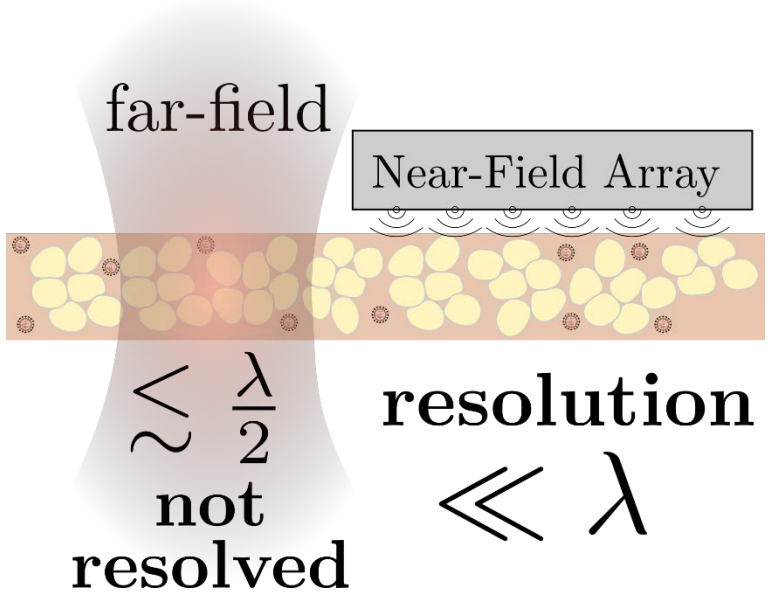
Motivation

Near-Field

Super-resolution
(<< wavelength)
No external optics



THz

Cell-scale resolution
(µm-range)
with
high sensitivity

Silicon

Low-cost
High integration
Scalability
Low-power
Mixed-signal

System-on-a-Chip

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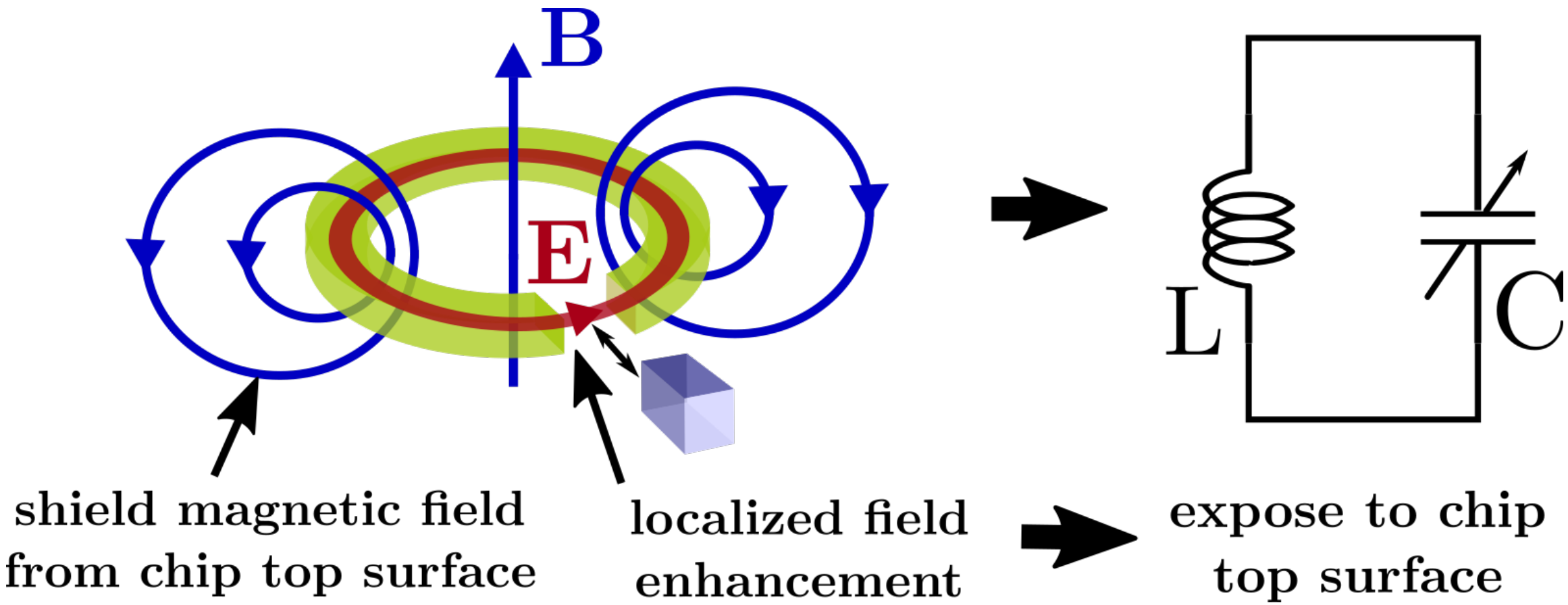
Sensing Mechanism

Split-ring resonator (SRR)



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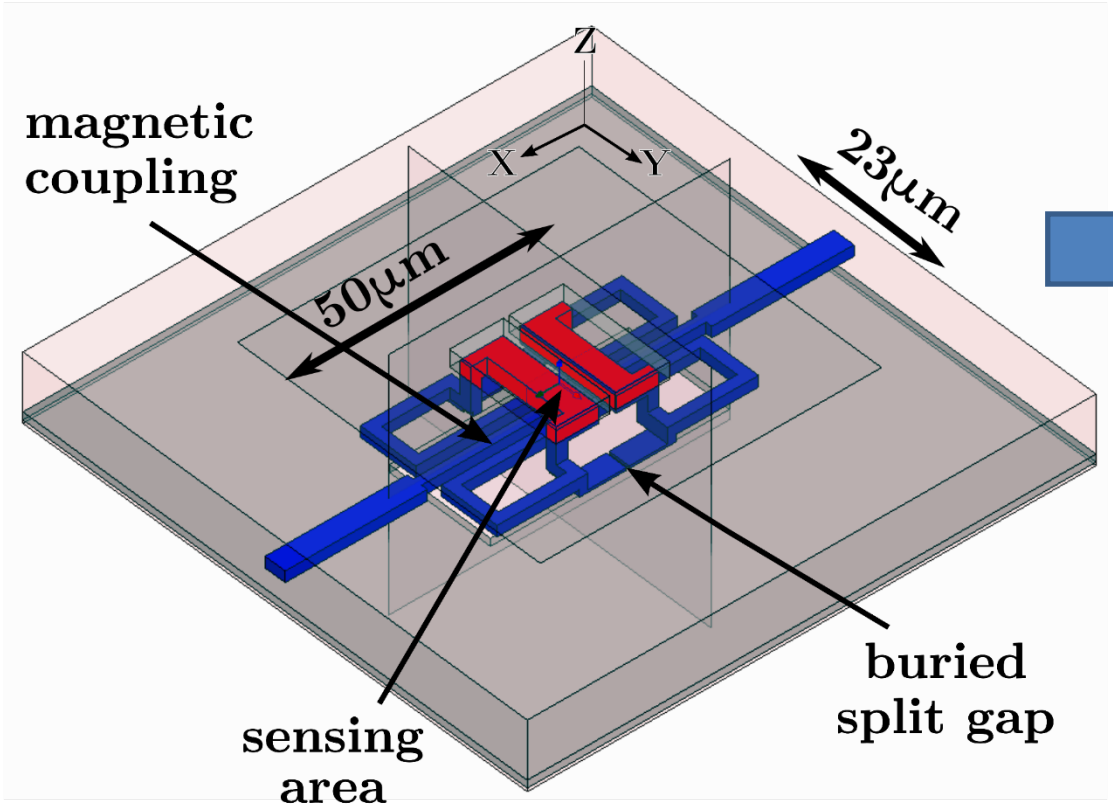
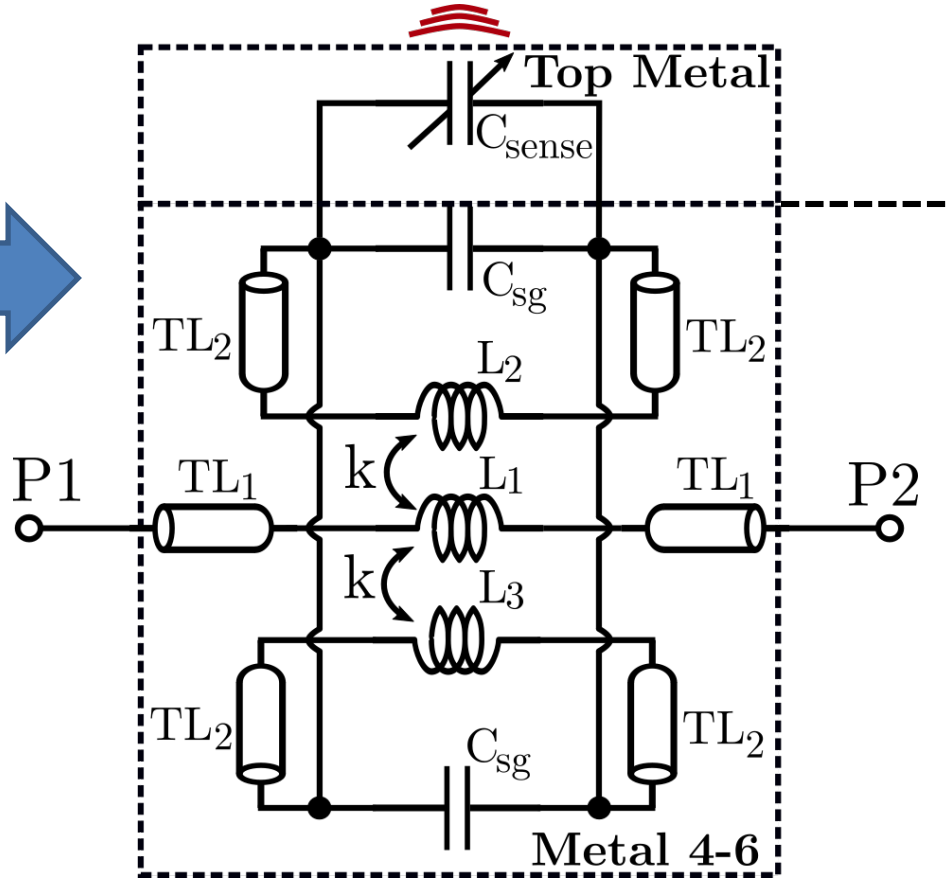
Resonator Design

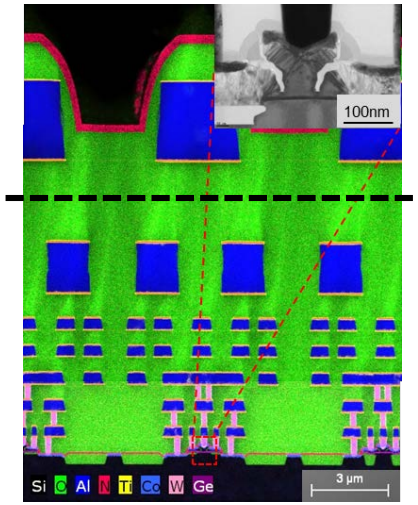
3D view



equivalent circuit



15.3µm thick BEOL



IHP 0.13µm SiGe-BiCMOS

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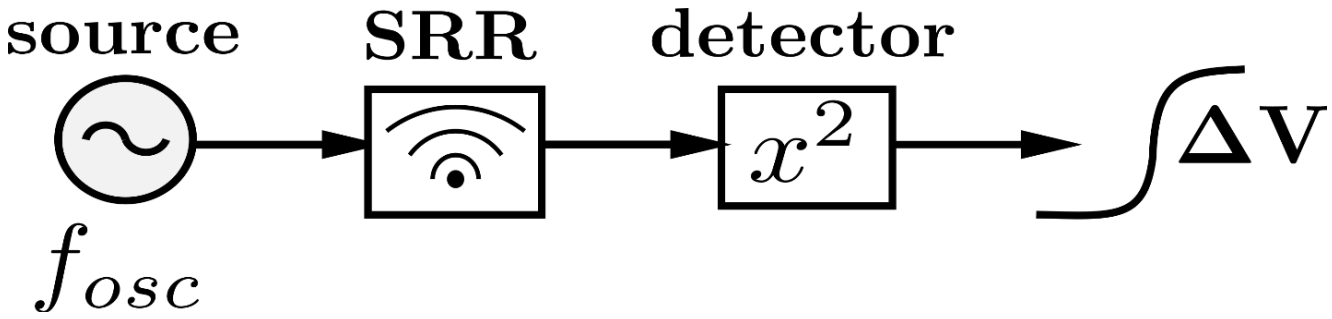
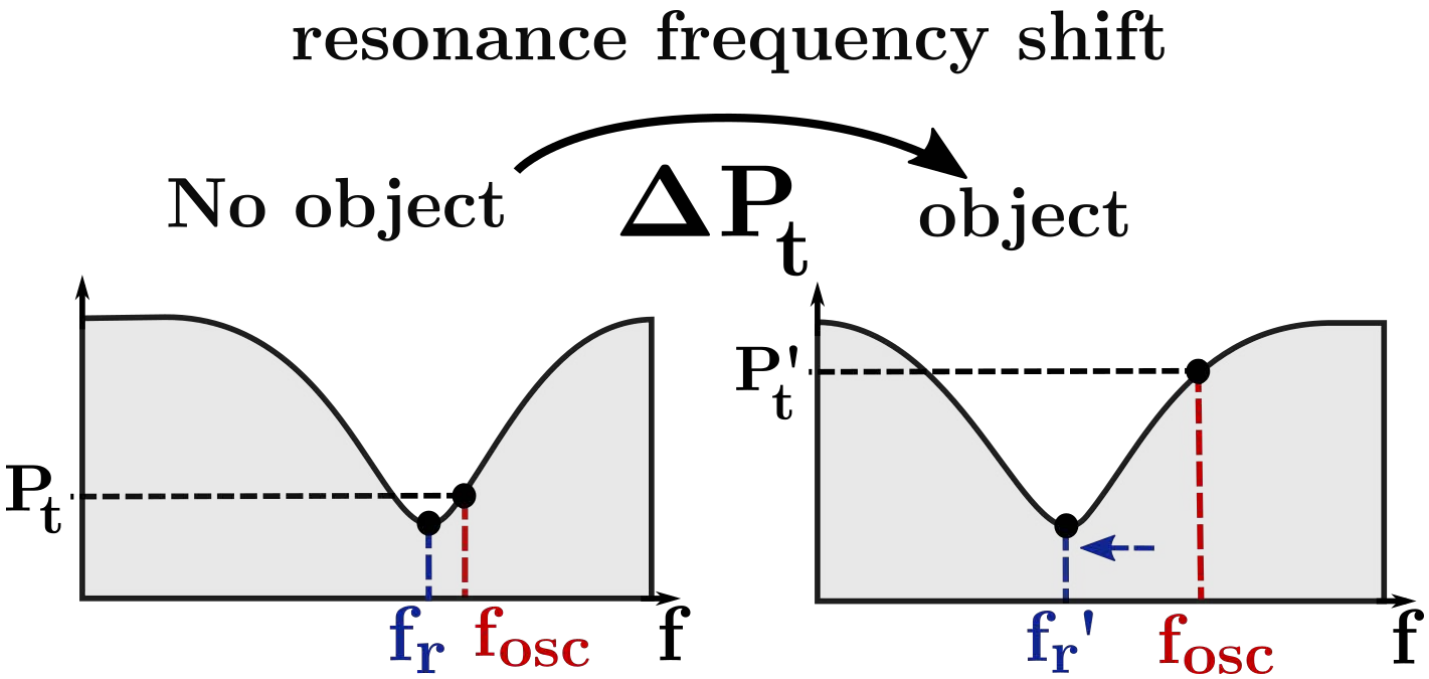
Sensing Concept



3-D SRR inserted between source and detector

- Stop-band characteristics as an object-tunable transmission



Difference in transmitted power between two sensor states: **with and w/o object present**

Free-running oscillator and power detector

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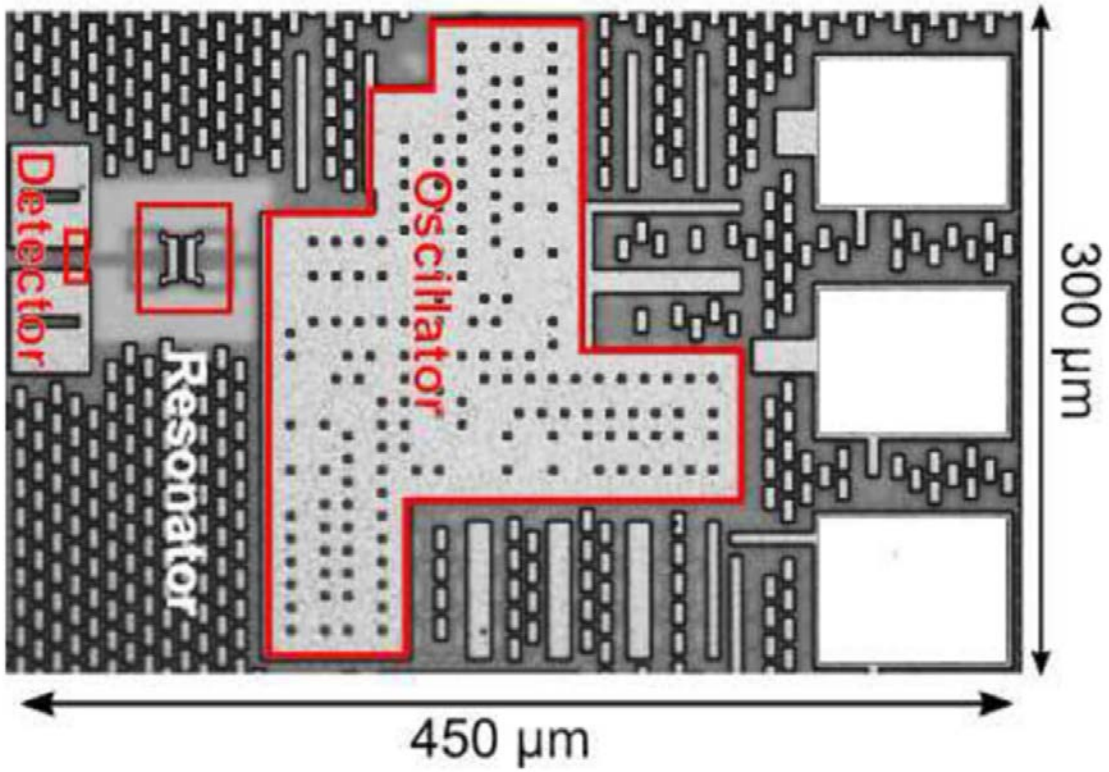
Challenges for Multi-Pixel Integration

1. **Maximize filling-factor**
   - Oscillator footprint **>>** resonator

2. **Response integrity**
   - Pixel-to-pixel coupling
   - Field shielding

3. **Large-scale read-out scheme**
   - Real-time
   - High-sensitivity
   - Low power consumption



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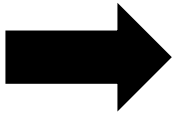
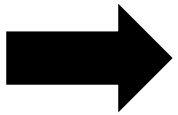
Challenges for Multi-Pixel Integration

1. **Maximize filling-factor**
   - Oscillator footprint **>>** resonator



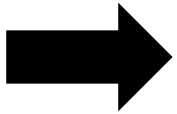
High-density 1-D strip, power divider network, vertically mirrored

2. **Response integrity**
   - Pixel-to-pixel coupling
   - Field shielding



Striplines, High-isolation Wilkinson power splitters

3. **Large-scale read-out scheme**
   - Real-time
   - High-sensitivity
   - Low power consumption



Oscillator chopping, Fully integrated analog/ digital read-out scheme

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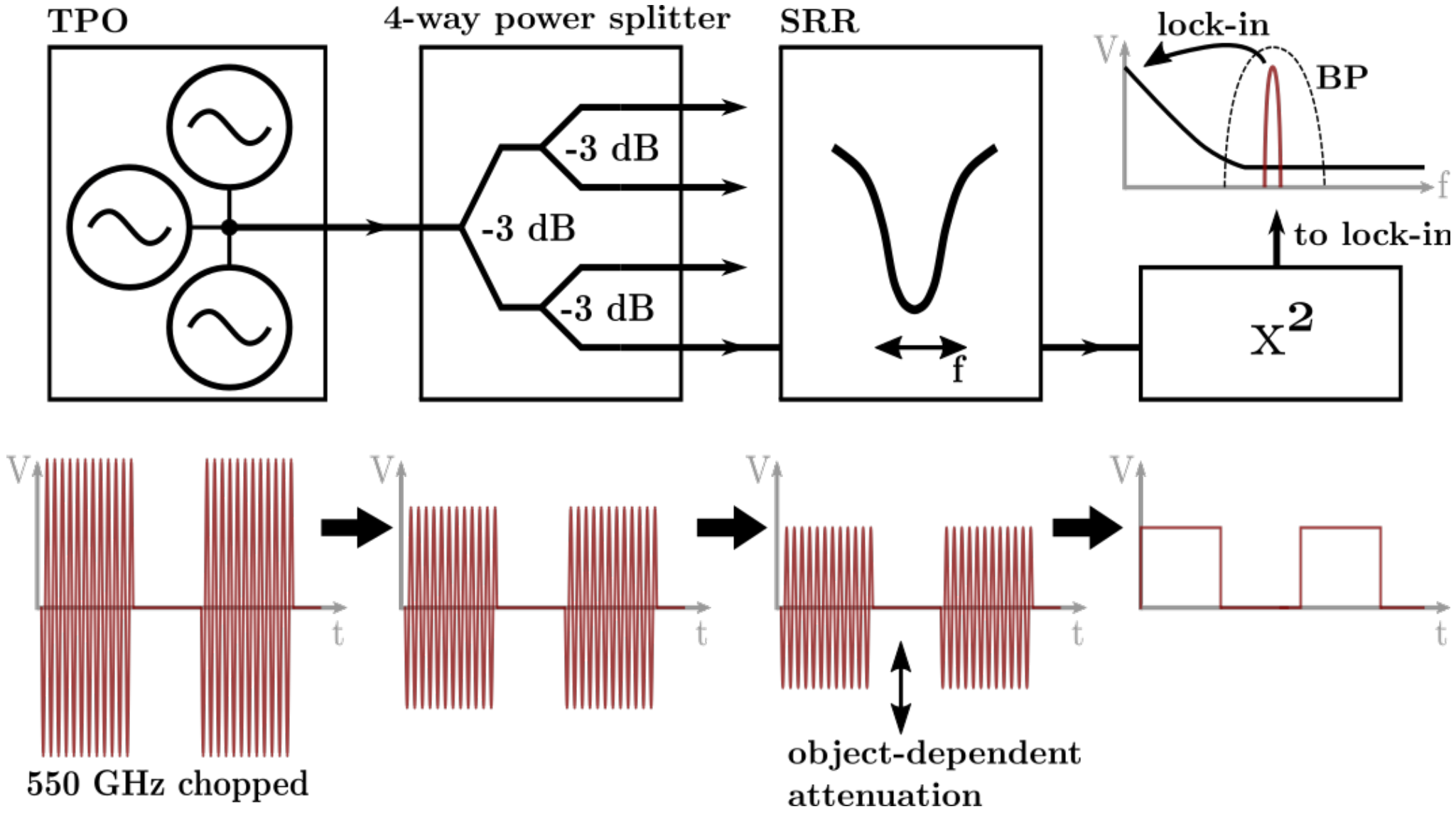
Sub-array Signal Processing



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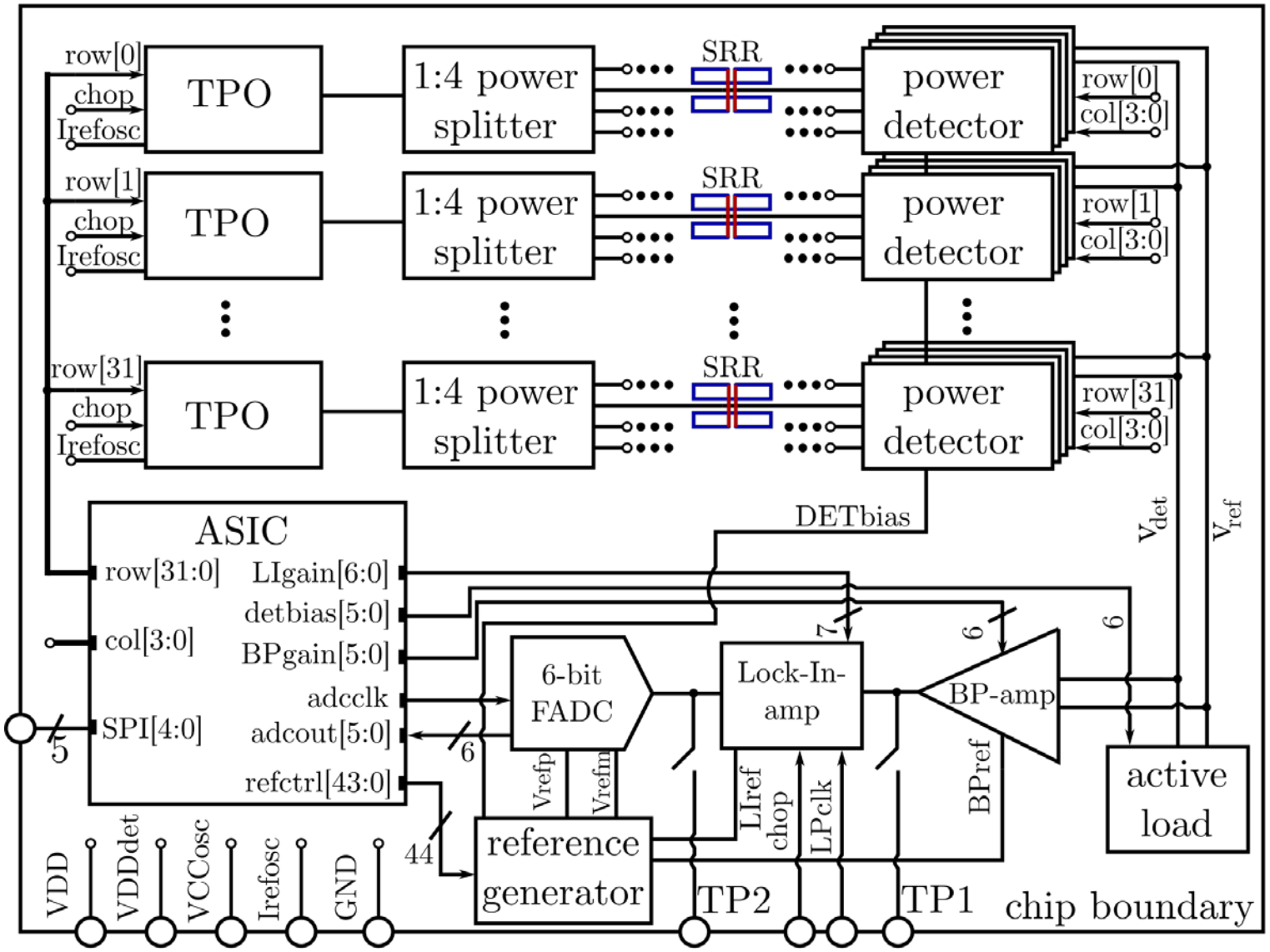
SoC Block Diagram



- IHP 0.13µm SiGe-BiCMOS (f_T/f_{max}=300/450GHz)
- Two vertically mirrored 64 pixel long rows of SRRs/ power detectors
- Each row divided into 16 subarrays of 4 pixels
  - Driven from single triple-push oscillator
  - Connected by 4-way power splitter

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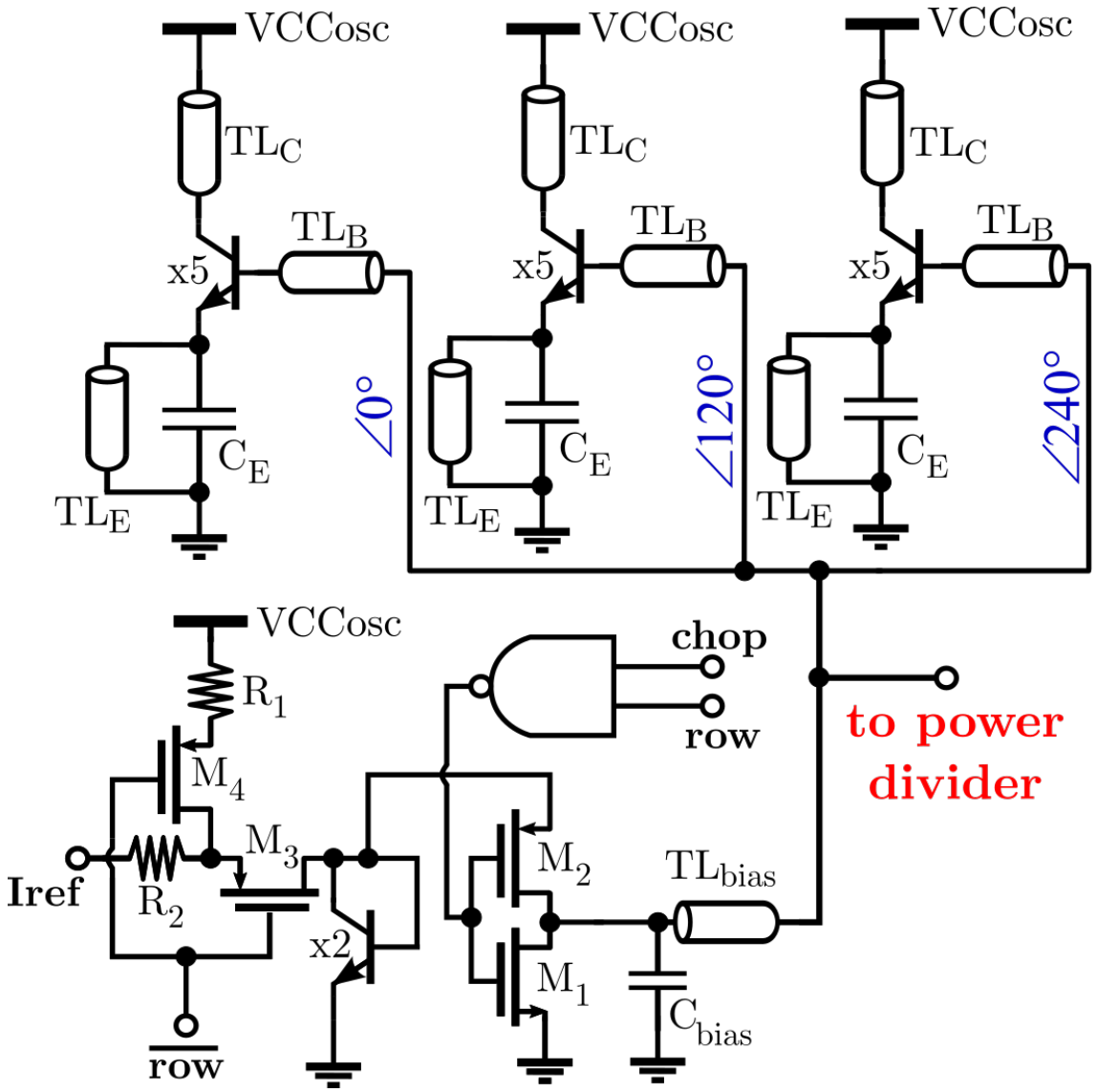
Illumination Source



- Single-ended 3-push Colpitts oscillator in CC configuration
  - ➢ Common virtual AC-ground prevents potential frequency pulling
- Current-mirror biasing scheme with base pull-down logic for chopping (chop) and oscillator selection (row)
- Simulations: **530 GHz, 50 µW**
  Measurement (break-out with antenna*): **534-562 GHz, 28 µW**

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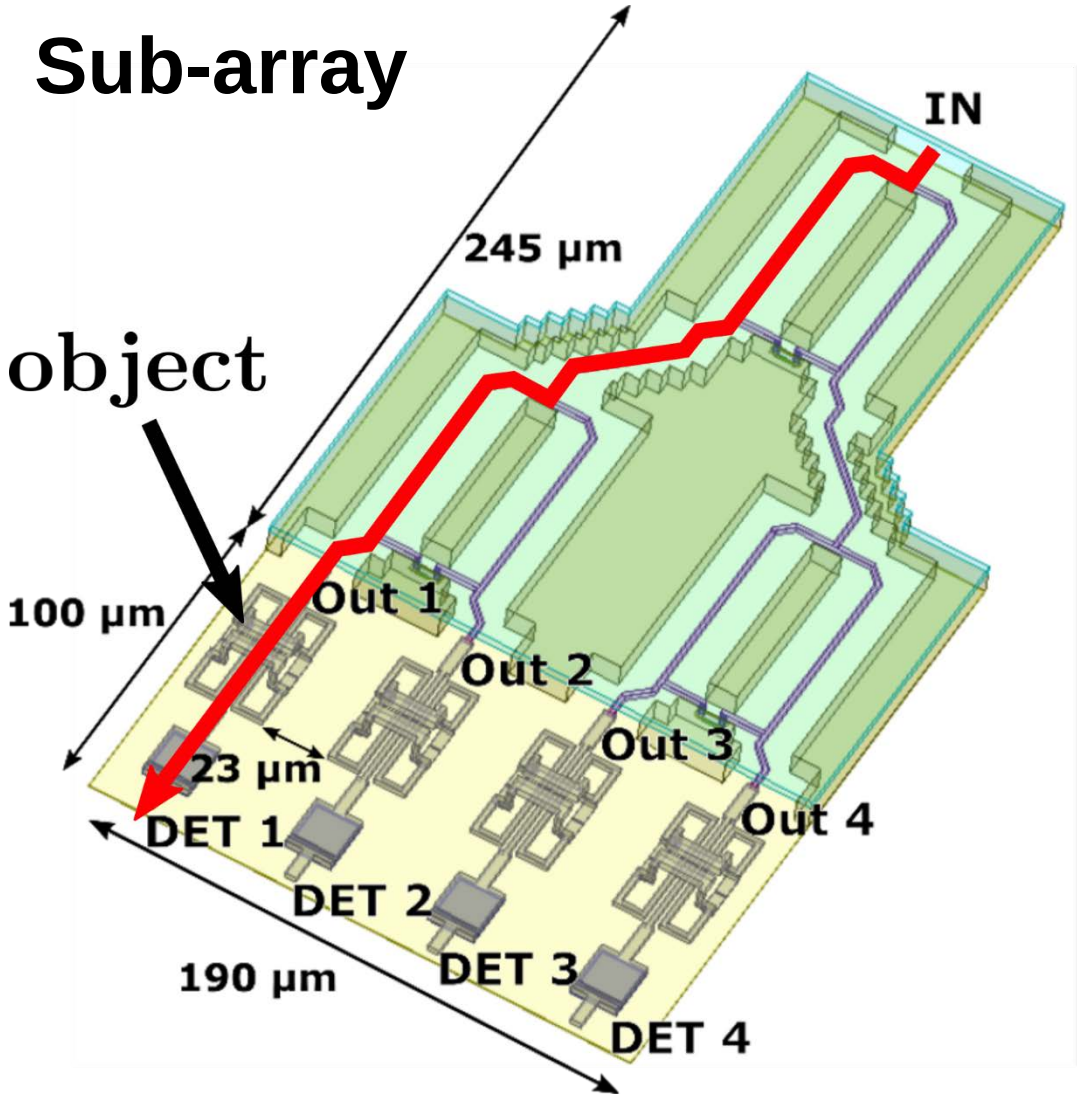
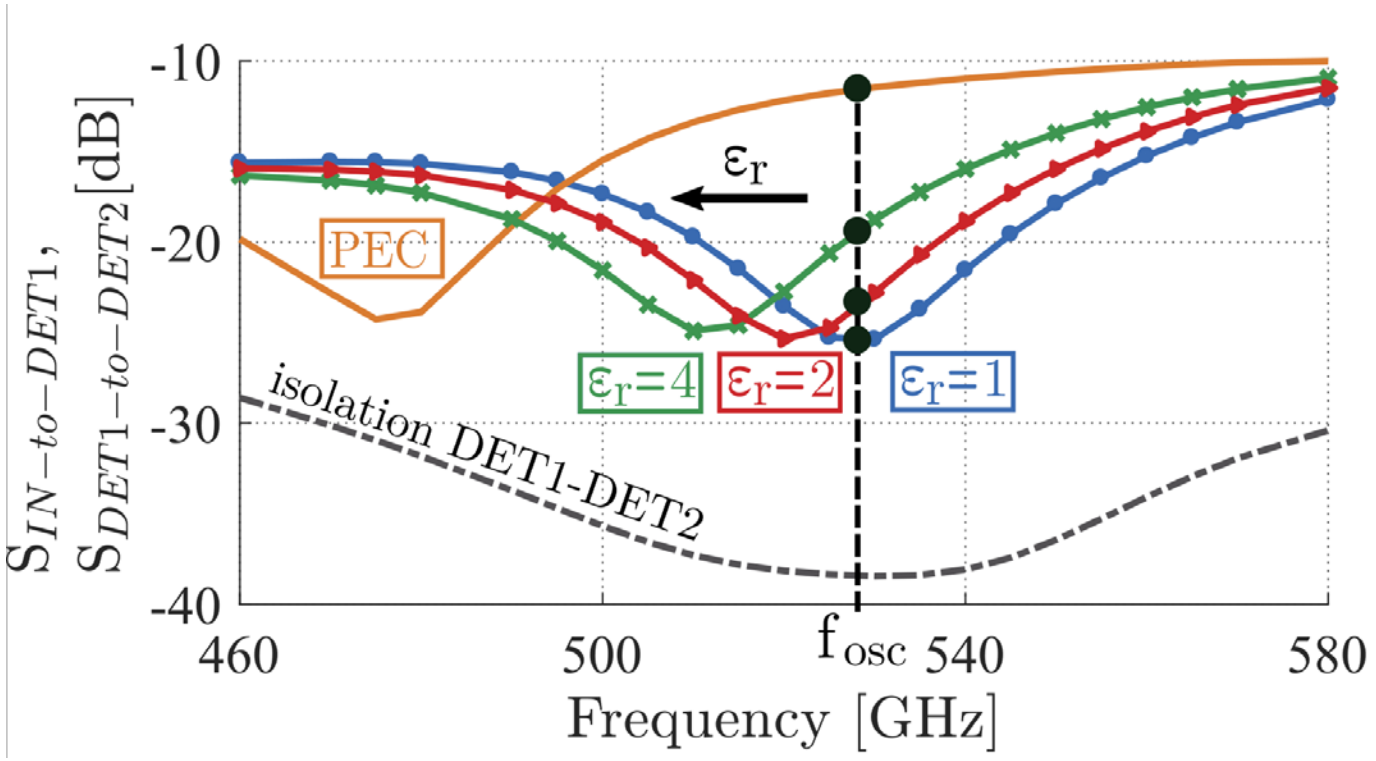
Simulated Sensor Operation

Sub-array



Object dependent insertion loss



- 7.8 dB power-splitter insertion loss
- 15 dB modulation depth
- >30 dB DET-to-DET isolation

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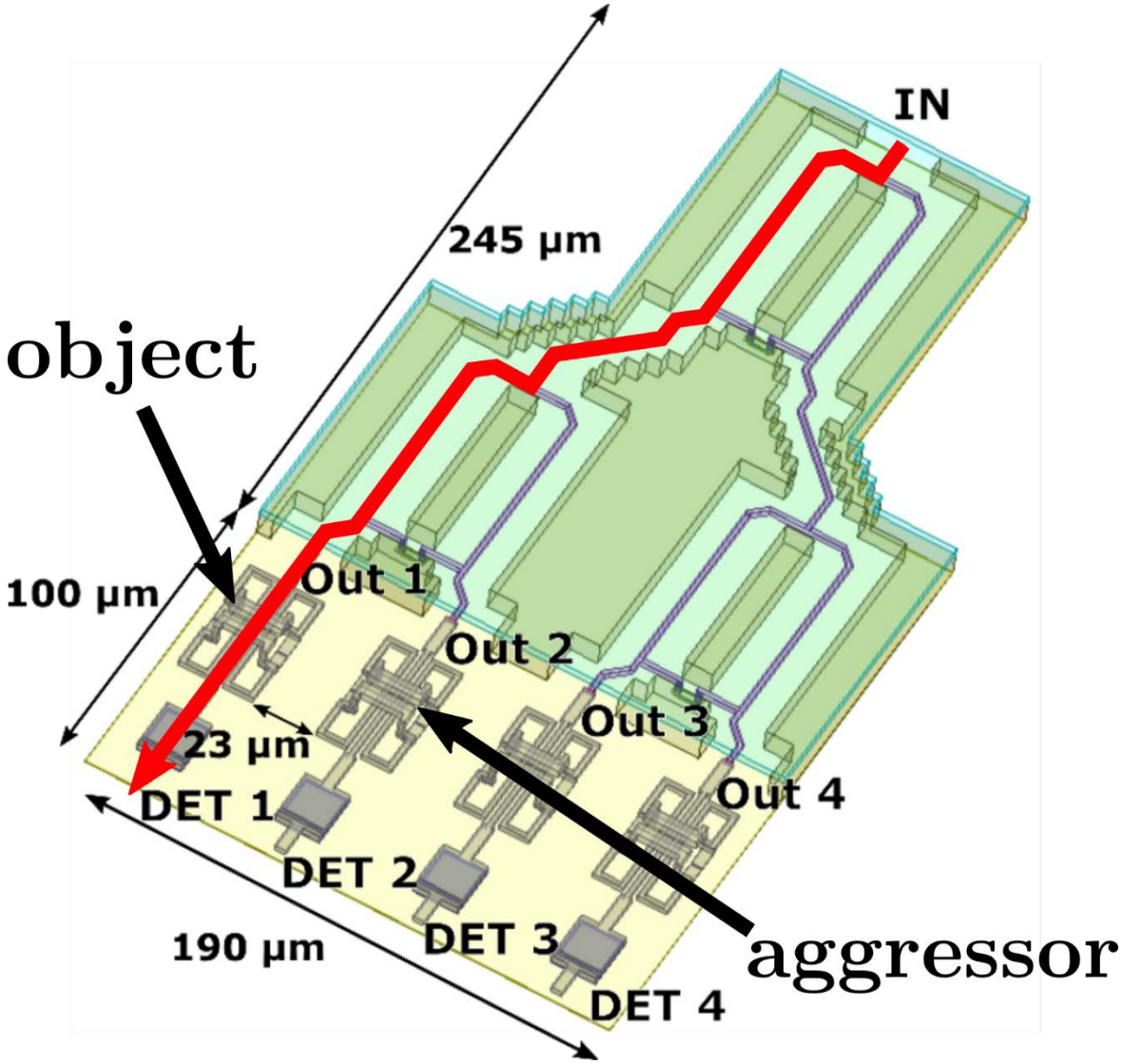
Pixel-to-pixel Coupling



Resonator impedance is strongly object dependent

Reflections and impedance imbalance in the splitter network

Parasitic response

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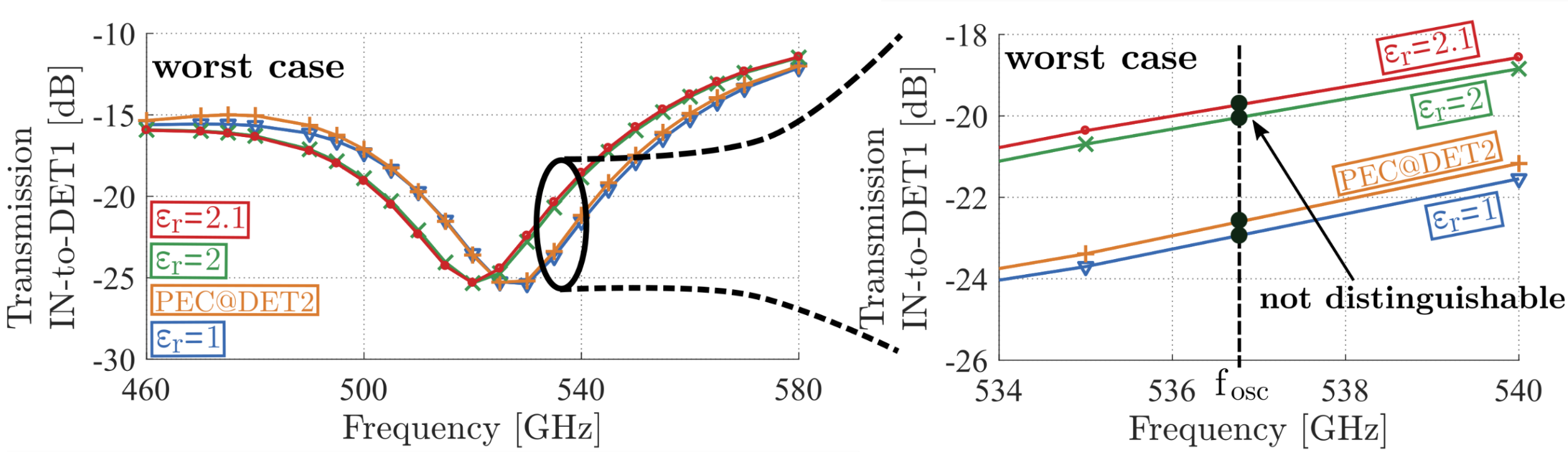
Pixel-to-pixel Coupling



Desensitization caused by network coupling

→ worst case: ε_r uncertainty 0.1

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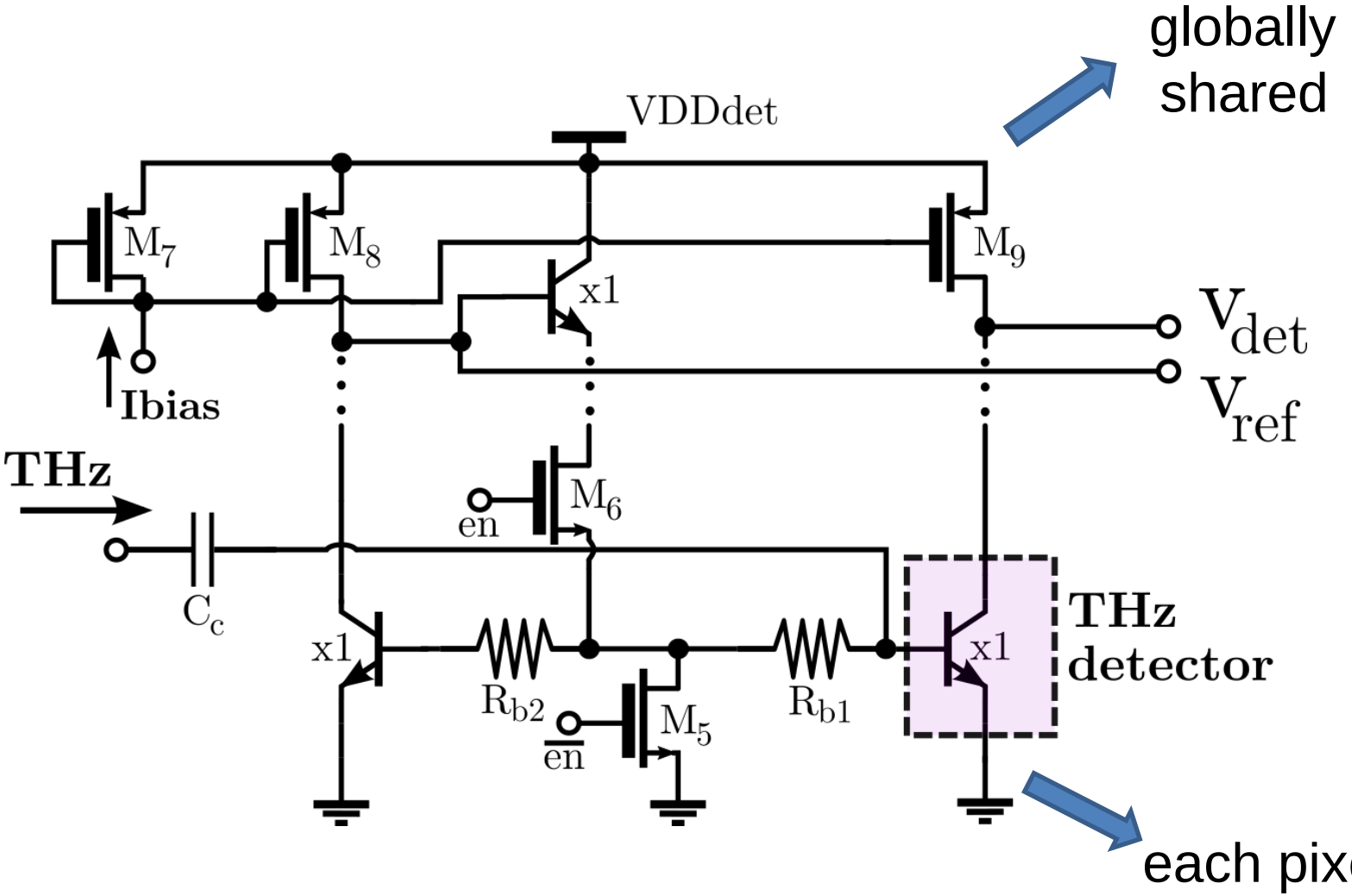
Power Detector Design



- THz-to-DC rectification with BE-junction non-linearity of SiGe-HBT ($\mathbf{R_I \approx 0.48\ ^{A}/_{W}}$)
- DAC controlled, selectable current mirror biasing scheme (3.3V logic)
- Globally shared active load for detector current to voltage conversion

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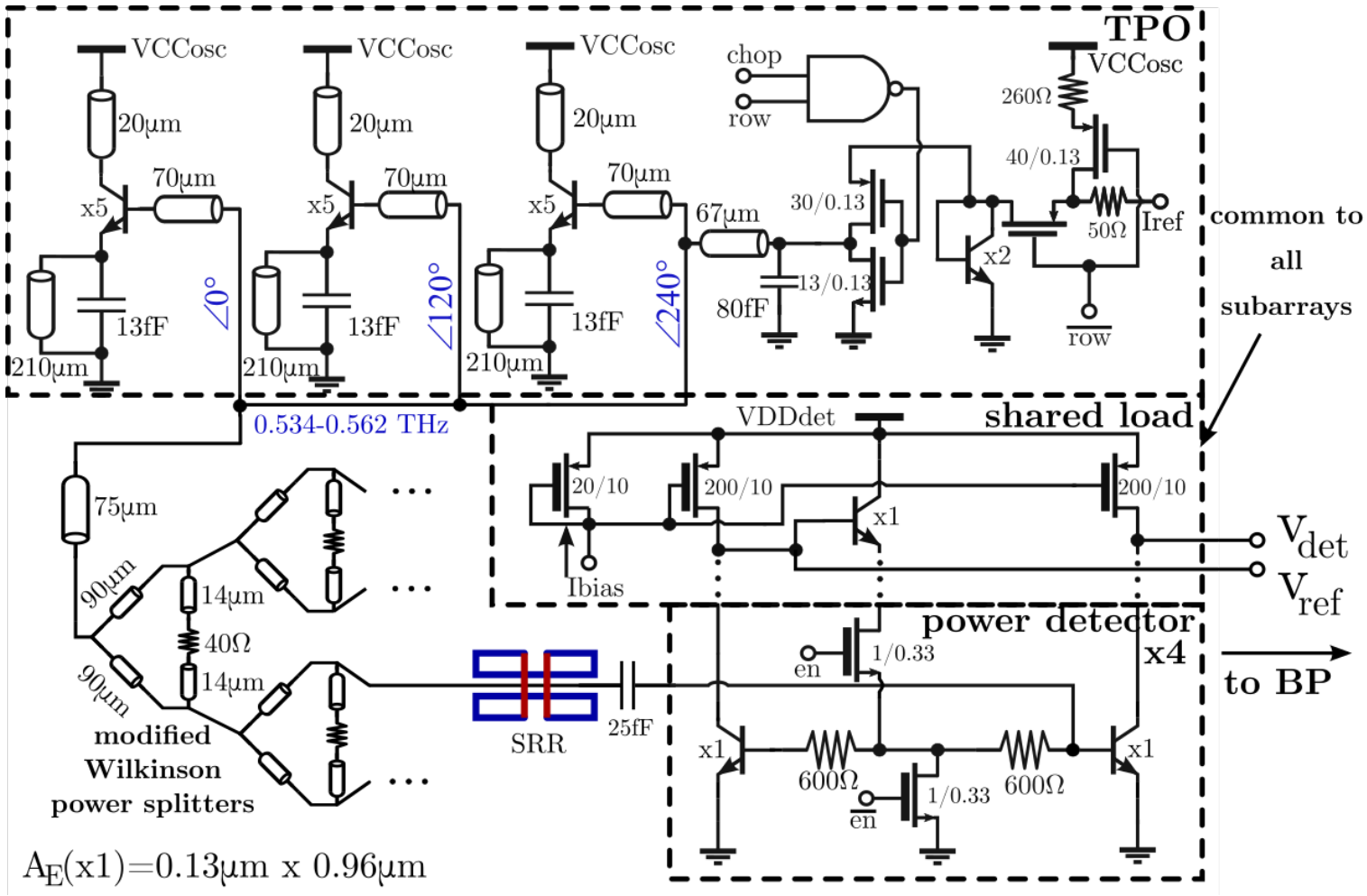
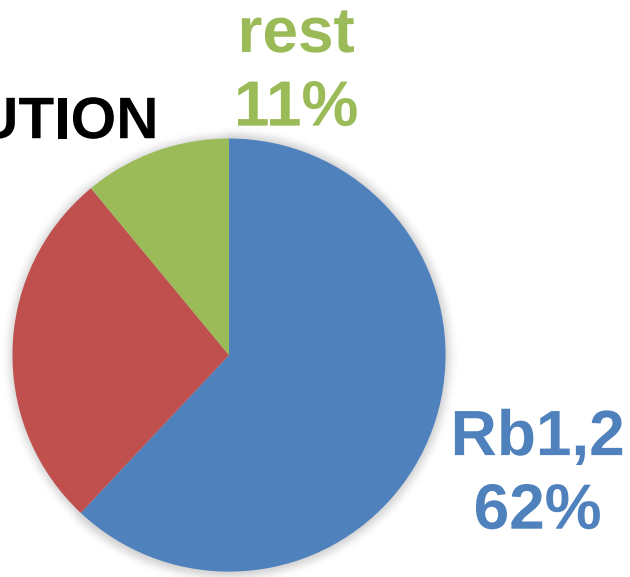
Sub-array Schematic



NOISE CONTRIBUTION @ 200 KHZ



Simulations:

- BW = 350 kHz
- Transimpedance = 60 kV/A
- V_{noise} @ 200 kHz = 1.8 $\mu V/\sqrt{Hz}$

With $\Delta P_{det,metal} = 2.5\ \mu W$
and $R_I = 0.48\ A/W$
→ **DR ≈ 91 dB**

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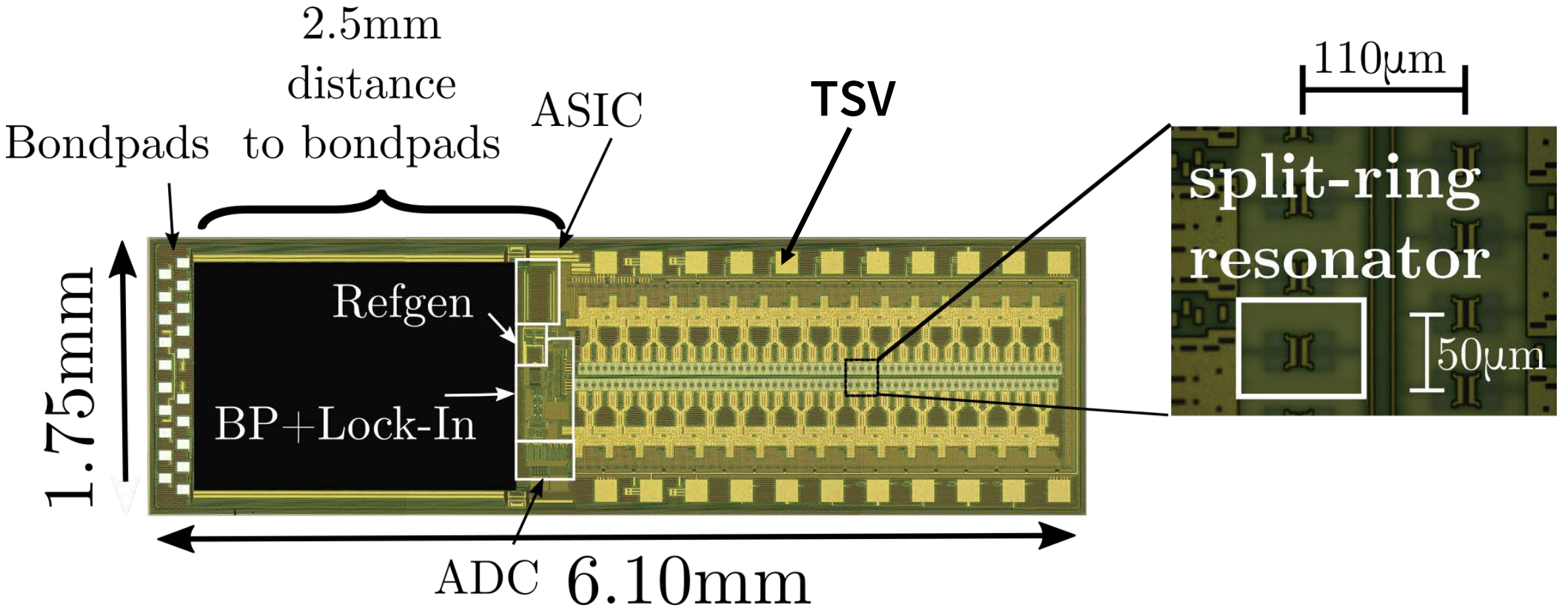
Chip Micrograph



Total power consumption 78 mW

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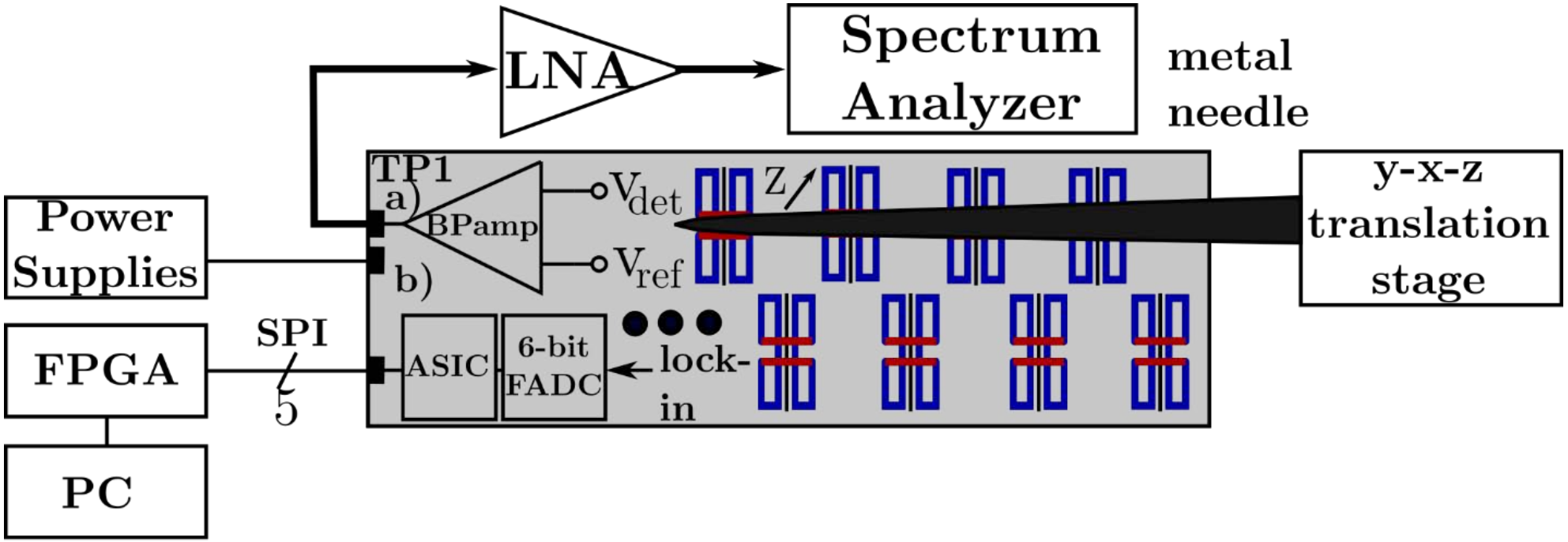
Characterization Setup



$$DR = 20 \cdot log_{10}\left(\frac{V_{metal} - V_{noObj}}{V_{noise}}\right) \rightarrow \Delta V$$

Dynamic range:

1) No Object → V_{noObj}
2) Completely covered (metal) → V_{metal}

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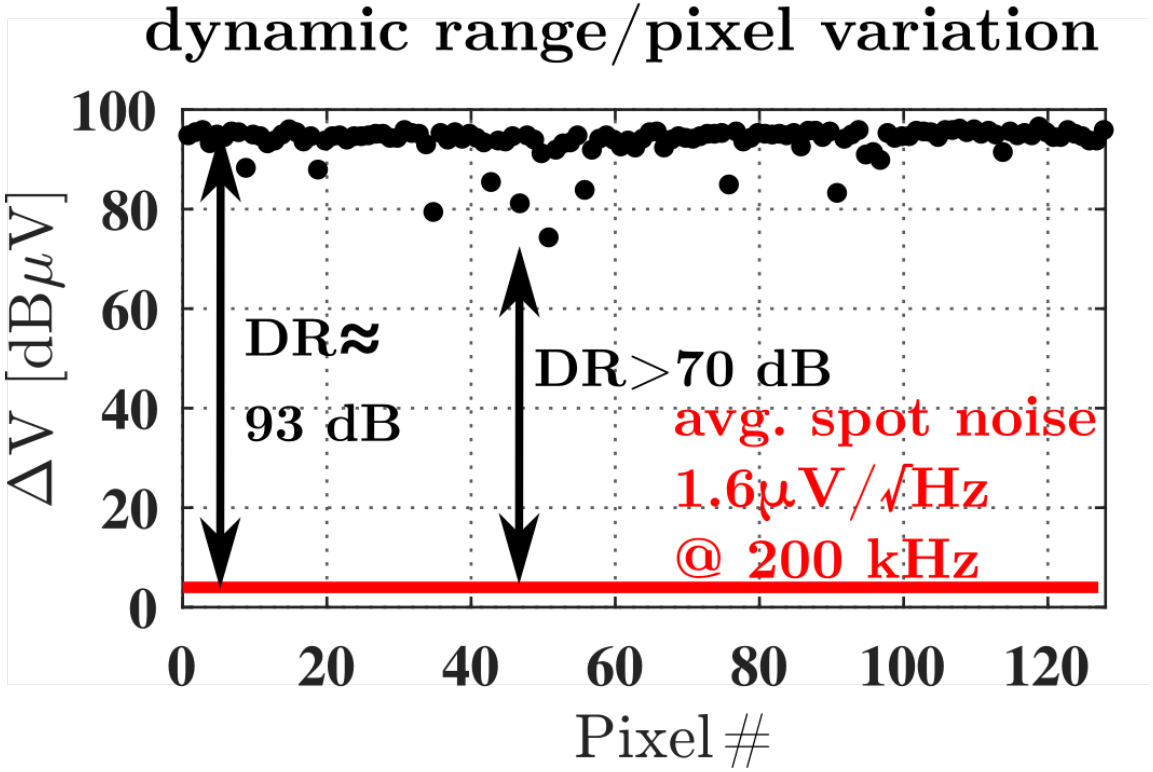
Read-Out Characterization

Analog:

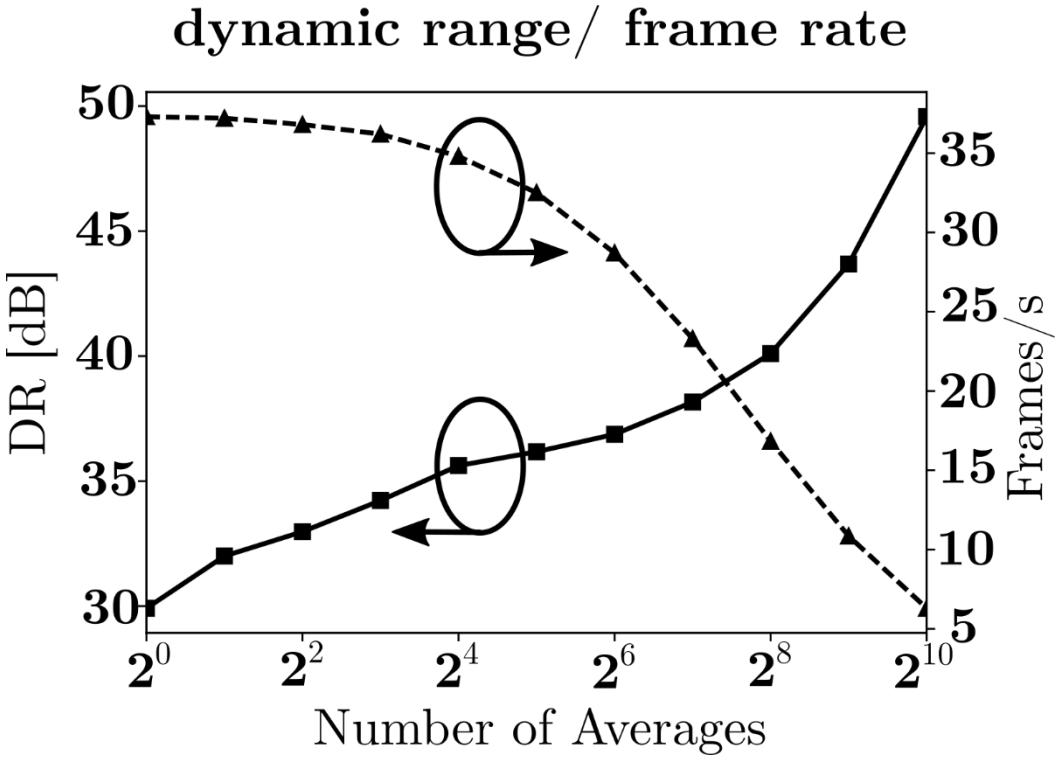


Typical:

DR = 93 dB (1 Hz BW)

57 dB (2.4 kHz BW)

Digital:



f_s=1 MHz, f_{chop}=200 kHz, $f_{C,LP}$=2.4 kHz

N_{avg}= 64:

DR = 37 dB, frame rate = 28fps

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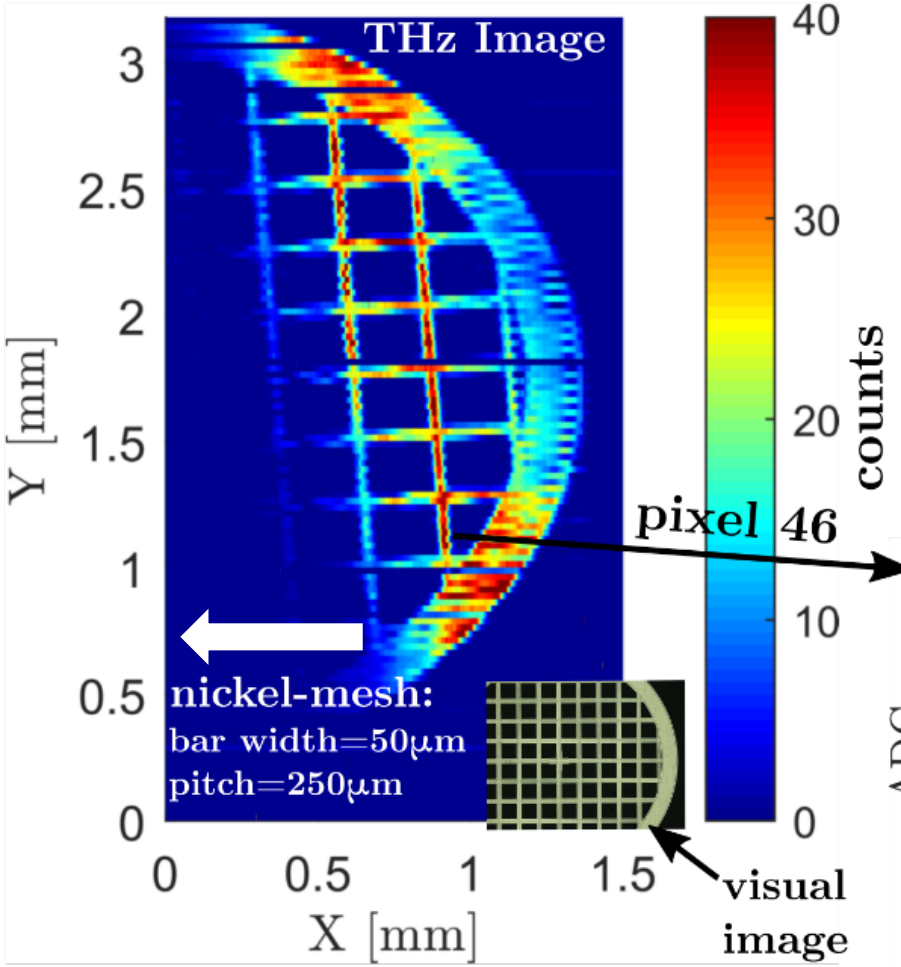
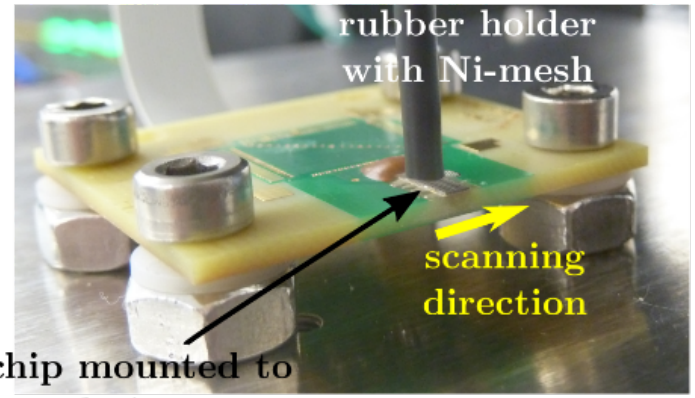
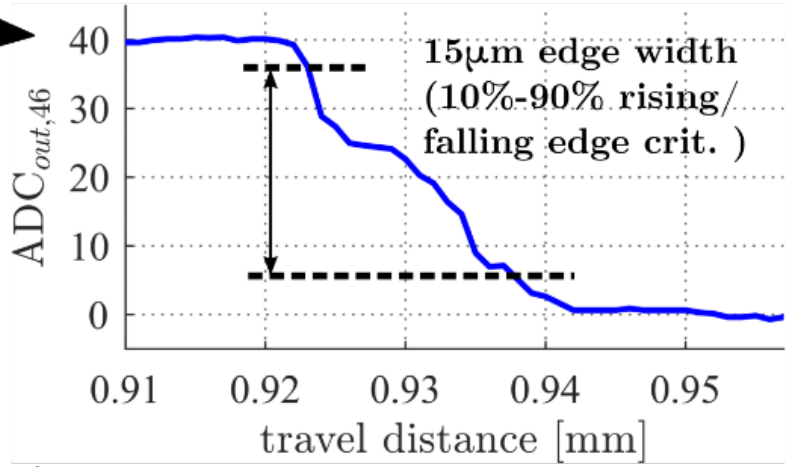
Imaging Results







Pixels=128x1500 (1D,1um step size)
Tscan=6min 45sec

1-D scan:
X-step - 1 µm
Size - 1.5 x 3.2 mm²
Time - 6min 45 sec

- Small distance to sensor surface (< 10µm)
- Bar edges resolved with **15µm resolution** (10-12µm with single resonator / needle *)

max. speed: 312.5 µs/pixel

SoA NSOM ≈ 10 ms/pixel

***J. Grzyb et al., JSSC 2017**

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State-of-the-art Comparison

Technology	Resolution	Frequency	Dynamic Range	Integration Level	No. of Pixels	Ref.
NSOM	typ.: 3.3-40µm	0.2-2.5THz	low (typ.<20dB)	ext. decetctor/source	1	[1]
0.13µm SiGe	est. 10-12µm	0.534-0.562THz	42dB	detector/source	1	[2]
0.13µm SiGe	est. 8-10µm	0.533-0.555THz	20dB	detector/source	1	[3]
0.13µm SiGe	**est. 10-12µm**	**0.534-0.562THz**	**93dB / 37dB@28fps**	**fully integrated**	**128**	**This work**

[1] A. Adam, J. Infrared, Millimeter and Terahertz Waves, 2011
[2] J. Grzyb, IEEE Trans. on Microwave Theory and Techniques, 2017
[3] J. Grzyb, ISSCC Dig. Tech. Papers, 2016

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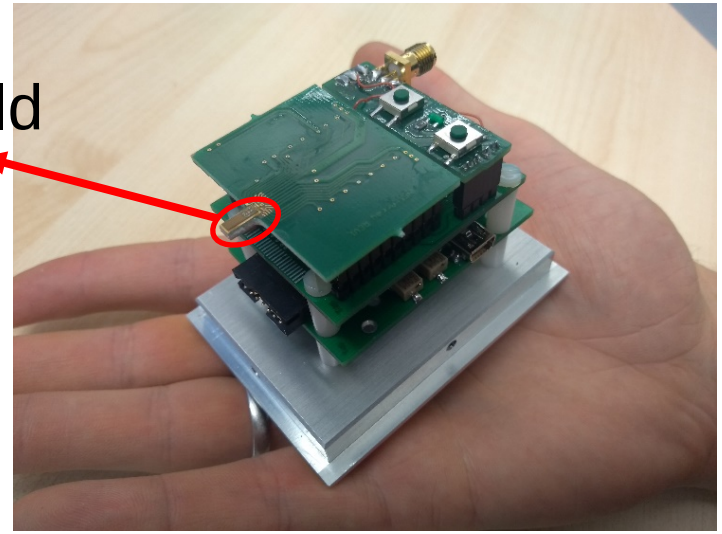
Summary and Outlook

World's first super-resolution THz near-field imaging SoC

Key features:

- 128 pixels, filling factor ≈ 0.5
- 10-12 um resolution @ 550 GHz (λ/55)
- Fully integrated mixed-signal design
  - ➢ Video-rate read-out (up to 35 fps)
  - ➢ DR = 57 dB (analog), 37 dB (digital) @ video-rate
- Scanning speed up to 312.5µs/pixel
- P_{DC}= 78mW → 610 uW/pixel
- Stand-alone, USB, battery operated

Portable prototype (demo session DS2)



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