Session 28 Overview: *Wireless Connectivity*

**WIRELESS SUBCOMMITTEE**

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Connecting things wirelessly requires optimization from multidisciplinary areas. This session will introduce state-of-the-art wireless transceivers supporting ultra-lower-power IoT and connectivity solutions. In this session, a high-performance WLAN SoC supporting up to 802.11ax 1024QAM will be presented. Then, two-blockers-tolerant high-sensitivity Bluetooth Low-Energy (BLE) transceivers in 65nm and 40nm CMOS will be presented followed by a best-in-class performance all-digital PLL for BLE in 16nm FinFET technology, and an energy-harvesting BLE transmitter in 28nm CMOS. An ultra-low-power wakeup receiver enabling event-driven sensor nodes and an ultrasonic wake-up receiver using a precharged capacitive micro-machined ultrasound transducer will be shown. Finally, a 5.8GHz near-field radio achieving the smallest die size of 116μm×116μm will be presented in this session.

**1:30 PM**

**28.1** An 802.11ax 4×4 Spectrum-Efficient WLAN AP Transceiver SoC Supporting 1024QAM with Frequency-Dependent IQ Calibration and Integrated Interference Analyzer  
*S. Kawai*, Toshiba, Kawasaki, Japan  
In Paper 28.1, Toshiba presents a fully integrated 4×4 AP WLAN SoC in 28nm CMOS supporting up to 802.11ax and equipped with frequency-dependent IQ calibration for 1024QAM and an interference analyzer for reliable connection.

**2:00 PM**

**28.2** An ADPLL-Centric Bluetooth Low-Energy Transceiver with 2.3mW Interference-Tolerant Hybrid-Loop Receiver and 2.9mW Single-Point Polar Transmitter in 65nm CMOS  
*H. Liu*, Tokyo Institute of Technology, Tokyo, Japan  
In Paper 28.2, the Tokyo Institute of Technology reports a Bluetooth Low-Energy (BLE) transceiver in 65nm CMOS. The RX consumes 2.3mW with a sensitivity of -94dBm and high blocker tolerance owing to the proposed single-channel demodulation and dynamic-range enhancement technique. The single-point polar TX consumes 2.9mW with a 1.89% FSK error.
3:15 PM

28.4 A 0.45V Sub-mW All-Digital PLL in 16nm FinFET for Bluetooth Low-Energy (BLE) Modulation and Instantaneous Channel Hopping Using 32.768kHz Reference

M.-S. Yuan, TSMC, Hsinchu, Taiwan
In Paper 28.4, TSMC, and University College Dublin present a 0.45V sub-mW all-digital PLL for BLE modulation and <100ns instantaneous channel hopping using a 32.768kHz reference in 16nm FinFET technology. It performs channel hopping and GFSK modulation in a 2-point manner with extensive DCO calibrations after locking to the center band upon system power-up.

3:45 PM

28.5 A 0.2V Energy-Harvesting BLE Transmitter with a Micropower Manager Achieving 25% System Efficiency at 0dBm Output and 5.2nW Sleep Power in 28nm CMOS

J. Yin, University of Macau, Macau, China
In Paper 28.5, the University of Macau and Instituto Superior Technico/University of Lisboa describe the implementation of a 0.2V energy-harvesting BLE transmitter in 28nm CMOS with a micropower manager exhibiting 25% system efficiency at 0dBm output. An ultra-low-voltage VCO with a 5.6:1 transformer and Class-E/F2 PA with an HD-3-notching transformer is presented with a passive-intensive type-I PLL with a 5% duty cycle to improve the reference spurs to -47dBc.

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28.6 A -76dBm 7.4nW Wakeup Radio with Automatic Offset Compensation

J. Moody, University of Virginia, Charlottesville, VA
In Paper 28.6, the University of Virginia reports an ultra-low-power wakeup receiver in 0.13μm CMOS, enabling event-driven sensor nodes with automatic offset compensation spending the majority of their time in an “asleep-yet-alert” state. The receiver consumes 7.4nW with a measured sensitivity of -76dBm and -71dBm at the 151.8MHz MURS and 433MHz ISM bands respectively.

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28.7 A 14.5mm² 8nW -59.7dBm-Sensitivity Ultrasonic Wake-Up Receiver for Power-, Area-, and Interference-Constrained Applications

A. S. Rekhi, Stanford University, Stanford, CA
In Paper 28.7, Stanford University implements an ultrasonic wake-up receiver in 65nm CMOS using a precharged capacitive micro-machined ultrasonic transducer. Realized in an area of 14.5mm², it achieves -59.7dBm sensitivity with 8nW power consumption.

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28.8 A 5.8GHz Power-Harvesting 116μm×116μm "Dielet" Near-Field Radio with On-Chip Coil Antenna

B. Zhao, University of California, Berkeley, Berkeley, CA
In Paper 28.8, the University of California at Berkeley presents a 5.8GHz power-harvesting 116μm×116μm “Dielet” near-field radio in 65nm CMOS with on-chip coil antenna. A hybrid two-tone IM2-IM3 technique is proposed to lock the on-chip oscillator, simultaneously improving the uplink SNR to 42dB and uplink signal-to-transmitter ratio to -28.9dBc at 20MHz.
An 802.11ax 4×4 Spectrum-Efficient WLAN AP Transceiver SoC Supporting 1024QAM with Frequency-Dependent IQ Calibration and Integrated Interference Analyzer

Shusuke Kawa1, Hirotomo Aoyama2, Rui Ito1, Yutaka Shimizu1, Mitsuyuki Ashida1, Asuka Maki1, Tomohiko Takeuchi2, Hiroyuki Kobayashi3, Go Urakawa3, Hiroaki Hoshino1, Shigehito Saigusa4, Kazushiru Koyama1, Makoto Morita5, Ryuchi Niihara2, Daisuke Goto2, Motoki Nagata1, Kengo Nakata1, Katsumi Ikeuchi1, Kentaro Yoshihara2, Ryoichi Tachibana3, Makoto Arai1, Chen-Kong Teh2, Atsushi Suzuki3, Hiroshi Yoshida3, Yosuke Hagiwara3, Takayuki Kato1, Ichiro Seto1, Tomoya Horiguchi2, Koichiro Ban1, Kyosuke Takahashi2, Hitotsubashi Kajihara2, Toshiyuki Yamagishi3, Yuji Fujimura3, Kazuhisa Horiuchi3, Katsuya Nonin1, Toshiya Mitomo1

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An exponentially increasing number of wireless-LAN (WLAN) devices in a dense environment causes a decrease in throughput owing to collisions among the devices and the lack of contiguous bandwidth. The next-generation standard of 802.11ax improves spectrum efficiency by additionally supporting 1024 (1QAM, OFDMA with 80-80MHz), these impose several challenges to silicon design. 1QAM demands extremely low TX EVM, which is better than 50dB for TXBB to achieve a frequency range up to 80MHz to achieve at least ~35dB RX EVM or less. Non-contiguous characteristics better than ~44dBc LO integrated phase noise as well as 50dB isolation between each TRX chain are mandatory. To manage these issues the proposed 1QAM 80MHz+80MHz signal was employed to enable an optimum transmission strategy. For example, if 802.11ax WLAN is deployed, it is operated simultaneously through switching to one of the different channels or by adjusting the packet transmission timing so that it has an on-off cycle corresponding to an alternating power-supply frequency. As fast as 10μs of identification latency clearly improves the throughput, but an approximately 10-10MHz manufacture-dependent bandwidth limitation is taked into consideration to achieve an optimum transmission strategy. For example, when 80MHz WLAN is deployed, it is operated simultaneously through switching to one of the different channels or by adjusting the packet transmission timing so that it has an on-off cycle corresponding to an alternating power-supply frequency. As fast as 10μs of identification latency clearly improves the throughput, but an approximately 10-10MHz manufacture-dependent bandwidth limitation is taked into consideration to achieve an optimum transmission strategy.

References:
Figure 28.1.1: Block diagram of proposed SoC.

Figure 28.1.2: Frequency-dependent IQ amplitude and phase compensator.

Figure 28.1.3: Current-mode TX baseband and programmable-gain QMOD schematics.

Figure 28.1.4: LO distribution schematic, measured phase noise, measured EVM in non-contiguous (80+80).

Figure 28.1.5: Block diagram of integrated interference analyzer and measured power interference density with detection result.

Figure 28.1.6: Measured EVM with calibration, TX OFDMA downlink interference, RX OFDMA EVM.
Figure 28.1.7: Performance comparison with previous works and die micrograph.
28.2 An ADPLL-Centric Bluetooth Low-Energy Transceiver with 2.3mW Interference-Tolerant Hybrid-Loop Receiver and 2.9mW Single-Point Polar Transmitter in 65nm CMOS

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This paper demonstrates a Bluetooth Low-Energy (BLE) transceiver (TXR) achieving ultra-low-power (ULP) operation for Internet-of-Things (IoT) applications. As more and more devices will be connected and accessed to the Internet, their power consumption must be extremely constrained in the 2.4GHz ISM band. To coexist with all the wireless devices without being interfered by co-channel and out-of-band (OB) signals, a BLE receiver (RX) should have very high adjacent-channel rejection and very high blocker tolerance. At the same time, the total power consumption should be minimized for longer battery life. In this work, the TXR utilizes a wide-loop-bandwidth All-Digital PLL (ADPLL) as a central component for transmitting (TX) modulation, RX analog data digitization, and phase synchronization. The single-channel demodulation method is adopted for cutting half of the analog baseband circuit to further reduce the power consumption while maintaining a high interference rejection. This BLE TXR achieves the lowest energy consumption among the state-of-the-art works in the comparison table [1-5] while satisfying all the interference requirements with sufficient margins.

A hybrid-loop RX is proposed in [1] targeting adjacent-channel rejection while eliminating two ADCs and Q-channel to reduce power. However, the reuse of the ADPLL as an ADC consumes large power, which makes it less attractive. Furthermore, the RX suffers from carrier frequency mismatch between TX and RX, and non-coherent demodulation by only the I-channel drops Q-channel information [1]. Figure 28.2.1 shows the BLE TXR block diagram. The hybrid-loop RX architecture is adopted for eliminating the ADCs and a Q-path for demodulation. The ADPLL is capable of 5MHz wide-loop-bandwidth operation using a 26MHz reference thanks to the integrated reference doubler and loop latency compensation technique. Less than 0.5 reference-period loop latency is achieved, which realizes over 70-degree phase margin at 5MHz loop-bandwidth. The wide-loop-bandwidth operation of the ADPLL stabilizes the oscillator frequency while being used as an ADC, hence it can also be used as the local oscillator (LO) for downconversion at the mixer side. The power consumption of the ADPLL is only 1.1mW in RX mode. The Digitalized data Dout from the ADPLL is filtered by a 27-tap FIR filter for further noise and interference rejection. The phase and frequency information is estimated from Dout and feedback to LO frequency directly though the ADPLL frequency control word (FCW). The synchronization loop mitigates the phase rotation of I and Q channels caused by frequency and phase offset, which improves the RX sensitivity. Finally, the symbol timing will be recovered and demodulated by the integrated data decoder. To further take the advantage of the wide-loop-bandwidth operation of the ADPLL, a 1Mb/s GFSK signal is modulated through FCW, which forms a single-point modulator. It can make the TX simplified without any calibration such as DCO gain and linearity calibration in the conventional two-point polar modulators. Furthermore, the wide-loop-bandwidth operation also relaxes the PA pulling effect in TX mode, which is a problem in the conventional two-point modulator when DCO and PA share the same frequency.

Figure 28.2.2 shows the low-IF receiver [5] as one of the most common receiver architectures for ULP applications. It achieves good in-band and OB blocker performance. However, it requires both I and Q channels which consumes significant power. To take advantage of the single-channel receiving method, where the incoming BLE signal is downconverted to a very low IF signal (250kHz) in order to transfer the constellation into DPSK from GFSK modulation [1] and can be demodulated using only the I-channel. The very-low-IF architecture helps to solve the image rejection issues, which will degrade the OB blocker performance in the sliding-IF architecture [3]. Furthermore, thanks to the lowpass filter and the lowpass transfer characteristics of the ADPLL, the entire RX system will be able to filter an over 55dB blocker rejection over 3MHz offset. The ADPLL is reused as an ADC which transfers the analog signal to its digital version. The I and Q channels are derived and filtered using a Timing Error Detector (TED) in the single receiving channel. The phase error is filtered by a digital loop filter and added to the ADPLL FCW. Owing to the wide loop-bandwidth ADPLL operation, it can instantaneously synchronize both the phase and small frequency error of the incoming signal with the LO signal. As compared with the power budget, the conventional I/Q low-IF RX, a total of around 54% energy can be saved thanks to the single-channel demodulation architecture and elimination of ADCs.

In order to reuse the ADPLL as an ADC, the analog input signal is first converted into a frequency offset through a varactor in an LC-VCO, and it is integrated as a phase offset. As shown in Fig. 28.2.3, in the conventional circuit the analog input signal VREF(t) is directly fed to the varactor, and the converted phase information is linearly represented by a Time-to-Digital Converter (TDC). The conversion digital phase error will be filtered and fed back as a digital control code Dout(n) of the DCO to keep constant frequency and phase. Thus, the digital control code Dout(n) always keeps canceling the frequency drift by the input signal VREF(t) as shown in Fig. 28.2.3, i.e., VREF(t) is digitized to -Dout(n). However, the varactor is a nonlinear component, and it introduces significant SNDR degradation in this A-to-D conversion. Even if a small-amplitude signal is an input to the varactor, the conversion still suffers from the noise and distortion trade-off and results in a poor SNDR performance. In this work, a feedback DAC is introduced to mitigate the nonlinearity issue in the varactor as shown in Fig. 28.2.3. The feedback DAC generates a cancellation signal to be subtracted from the incoming signal VREF(t), and only the small-amplitude residue signal VRES(t) is input to the varactor. Furthermore, the DAC feedback path will also be used as the phase-lock path for the ADPLL. The narrow-bandwidth frequency-lock path is used for centering the DC level of the feedback DAC in RX mode. This closed-loop operation can significantly improve the SNDR performance. An SNDR of 45dB is achieved in the measurement result, which is 18dB better than without the feedback DAC. In addition, the power consumption of the TDC can be saved due to a narrower TDC range. The required TDC range can be reduced because of the small amplitude of VRES(t), and the total power consumption of the PLL could be reduced to 1.1mW in this design.

Figure 28.2.4 shows the RF front-end design of the BLE TXR. A single-ended LNA is employed for lower power consumption, and the output is converted to a differential signal by a custom-designed on-chip balun. To reduce LNA power consumption, an additional lower-voltage supply is sometimes utilized [1,2]. To realize the entire 1V-supply operation while maintaining sufficient LNA current efficiency, a gm-cell is stacked on the top of the LNA transistor and the LNA output is coupled to a differential input of the gm-cell by the balun. The LNA bias feeds back from the gm-cell common-mode voltage, which stabilizes the LNA VDD voltage. The measured noise figure of the whole RX chain is around 6dB at the maximum gain of 68dB.

Figure 28.2.5 shows the measurement results of both TX and RX. The single-point modulation TX fully satisfies the BLE spectrum mask requirement. The measured FSK error is only 1.89%, which is the best among all the state-of-the-art BLE TX in Fig. 28.2.6. The modulator consumes 1.2mW for all BLE channels, and the PA consumes 1.9mW at -3dB output and 3.7mW at 0dBm. The RX consumes 2.3mW for RX front-end and ADPLL, which is the lowest among all the works listed in Fig. 28.2.6. The sensitivity level is -94dBm for a bit-error-rate (BER) of 0.1%. The adjacent-channel rejections are measured by setting the desired signal to -67dBm and increase the adjacent channel signal power until the BER reaches 0.1%. The adjacent-channel rejection is greatly improved by enabling the DAC feedback path. For the conventional design [1], the -3MHz point does not satisfy the BLE requirement while a 10dB improvement is achieved by the dynamic range enhancement technique. Figure 28.2.7 shows the measured adjacent-channel rejection by adopting the single-channel architecture and the dynamic-range enhancement technique, the proposed BLE TXR achieves the lowest power consumption while obtaining -94dBm sensitivity and satisfying all the interference requirements with a sufficient margin.

Acknowledgments:
This paper is based on results obtained from a project commissioned by the New Energy and Industrial Technology Development Organization (NEDO).

References:
Figure 28.2.1: Block diagram of the proposed BLE transceiver.

Conventional (Open-loop) [1]:

Proposed (Closed-loop):

Figure 28.2.3: Conceptual diagram of reusing ADPLL as ADC with enhanced dynamic range and measured SNDR performance.

TX Spectrum

RX ACR Performance

Figure 28.2.5: Measurement results of proposed BLE transceiver.

Figure 28.2.2: Conceptual diagram of ADPLL-centric RX architecture with phase and frequency synchronization and ADPLL reused as ADC.

Proposed Single-Channel RX

Conventional i/Q RX

Power Budget (mW)

Figure 28.2.4: RX front-end and analog baseband circuits capable of 1V power supply operation.

Figure 28.2.6: Performance comparison table.
Figure 28.2.7: Die Micrograph.
28.3 A 0.8V 0.8mm² Bluetooth 5/BLE Digital-Intensive Transceiver with a 2.3mW Phase-Tracking RX Utilizing a Hybrid Loop Filter for Interference Resilience in 40nm CMOS

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This paper presents a low-voltage (0.8V) ultra-low-power Bluetooth 5(BTS)/Bluetooth Low Energy(BLE) digitally-intensive transceiver for IoT applications. In comparison to BLE, BTS has a 2x higher data-rate and 4x longer range, while having >8x longer packet. The BLE prior arts [1-5] have made significant efforts to minimize the power consumption for longer battery life, as well as the chip area. However, the prior-art Cartesian BLE radios consume namely 6 to 10mW [1-3] to achieve a <−94dBm sensitivity but with a relatively high supply voltage ($V_{DD}$) (~1.8V). Operating a BLE RF transceiver at a lower $V_{DD}$ (e.g., <0.85V) not only extends the battery life by up to 50% [3], and reduces the Power-Management Unit complexity, but also can accommodate a wider range of energy sources (e.g., harvesters). A recent single-channel phase-tracking RX [5] demonstrated a potential to reduce the chip area and the power consumption at a $V_{DD}$ down to 0.85V. However, it suffers from a degraded sensitivity due to a poor deviation frequency control and an excessive loop delay, limited ACR (Adjacent-Channel-Depression) due to the digitally-controlled-oscillator (DCO) side-lobe energy, and an undefined initial carrier frequency due to the lack of a PLL/PLL interface, which could have a risk of tracking to an interference. This work presents a fully-integrated 0.8V phase-domain BTS/BLE-combo transceiver, including a PHY-layer digital baseband (DBB), and addresses the above-mentioned issues by employing two key techniques: 1) a hybrid loop filter with a loop-delay compensation for BTS side-lobe suppression to enhance interference tolerance, and 2) an all-digital PLL(ADPLL)-based digital FM interface shared between RX and TX is employed, including a deviation frequency calibration, and it also precisely defines the initial frequency. Moreover, the PHY-layer DBB that supports a packet-mode phase-tracking RX operation is also demonstrated.

Figure 28.3.1 shows the block diagram of the transceiver, illustrating a phase-tracking RX, a direct frequency-modulation digital TX, an ADPLL-based digital FM interface, and a PHY-layer DBB. The single-channel zero-IF RX together with the DCO forms a phase-tracking loop, allowing direct frequency demodulation with a simple 1b comparator (CMP) at low $V_{DD}$. The digital TX consists of a DCO modulated by the digital FM interface and an energy-efficient (30%) Class-D PA with an on-chip matching. The ultra-low-power dividerless snapshot ADPLL [6] avoids high-speed logic, allowing it to operate at 0.8V operation and consume only 415µW (excluding DCO). During the RX mode, the ADPLL is only needed at the start-up of the RX due to the presence of interference. The goal of the ADPLL is to suppress the DCO side-lobe energy by 2dB and 6dB at the 2nd and 3rd channel to meet the ACR target in BLE/BTS. In addition, the loop-delay compensation is implemented, which consists of three paths: Proportional, Integral, and Derivative (PID). These three paths form a highpass profile, which intrinsically provides a negative delay, compensating the delay of the following digital filter (~4τ_{DLO}). Thanks to the loop-delay compensation, a 4th-order Chebyshev II digital filter is implemented, suppressing the DCO side-lobe energy by 3 to 6dB at the adjacent channels.

The chip was implemented in 40nm CMOS, with a core area of only 0.8mm² (Fig. 28.3.7), including the on-chip matching. The chip was measured with standard BLE/BTS (1Mb/s / 2Mb/s) GFSK signals with PRBS9 pattern. Thanks to the proposed hybrid loop filter, the RX shows 2-to-7 dB improvement in ACR compared to [5], and does not suffer from the adjacent channel image issue as in [4] (Fig. 28.3.4). Despite the lower $V_{DD}$, the RX has a worst-case OOB blocker of ~17dBm, and does not have any OOB image as in [2,3]. To ensure that the demodulation performance is not degraded by any large DC offset during phase tracking, it is calibrated to within ±10mV before packets. As shown in Fig. 28.3.5, the PHY DBB performs this DC offset calibration and assists the phase-tracking RX to detect BLE/BTS packets. The $K_{dco}$ error can be calibrated well within ±3% thanks to the ADPLL-facilitated frequency-deviation calibration, which leads to an excellent −95 and −92dBm sensitivity in BLE and BTS, respectively. The RX, including the digital FM interface and DLF, consumes 2.3 and 2.9mW in BLE and BTS modes, respectively, where the digital power consumption (35%) and area (15%) can be further scaled in advance technologies. The TX exhibits a modulation quality of 2% (BLE) and 1.4% (BTS). The PA delivers maximum 1.8dBm power with 30% efficiency, and the 2nd and 3rd harmonics are −56dBm and −64dBm respectively, which are significant below FCC regulation. Figure 28.3.6 shows the benchmark of the state-of-the-art phase-tracking RX and BLE radios. This chip presents a BTS/BLE-combo fully integrated transceiver with a best RX figure-of-merit (FoM) and a lowest supply voltage among the state-of-the-arts in the table.

References:
Figure 28.3.1: Simplified block diagram of the transceiver.

Figure 28.3.2: Illustration of the phase-domain RX with interference resilience.

Figure 28.3.3: RX implementation with the hybrid loop filter and the loop-delay compensation.

Figure 28.3.4: Measured RX performance (Adjacent-Channel-Rejection, out-of-band performance, power consumption).

Figure 28.3.5: Measured RX sensitivity with $K_{DO}$ calibration and DC offset calibration, and packet detection in real time.

Figure 28.3.6: Performance summary and comparison with the state-of-the-art.
Figure 28.3.7: Die micrograph in 40nm CMOS.
28.4 A 0.45V Sub-mW All-Digital PLL in 16nm FinFET for Bluetooth Low-Energy (BLE) Modulation and Instantaneous Channel Hopping Using 32.768kHz

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The current paradigm of frequency synthesis for short-range wireless transceivers, such as BLE, is to use a crystal oscillator (XO) in the tens of-MHz range as a frequency reference (REF) to phase lock an RF oscillator [1-4]. This ensures a sufficiently wide PLL bandwidth of tens to hundreds of kHz to quickly acquire a new channel and to suppress lower-frequency phase noise (PN) of the RF oscillator. The latter requirement can be alleviated by substantially lowering the flicker PN of a digitally controlled oscillator (DCO) thus allowing to freeze its tuning word updates during receive (RX) packets and further directly FM-modulating the DCO during transmit (TX) packets [1]. However, an all-digital PLL (ADPLL) is still needed just to quickly settle the DCO to each new channel.

Eliminating the XO would significantly cut the total consumed IoT energy since it drains ~100uW just to sustain itself. Hence, for low-duty-cycle operations, the XO must be powered down. In this case, each restart is energy intensive (~1mW over ~1ms) so only XO shutdowns >10ms make sense [5]. In such systems, the energy drained by the XO can now be actually higher than in an RF PLL (~1mW over ~0.5ms) [1,2]. Only very recently, there was an effort embarked by the authors of [7] to reduce the XO startup energy by dynamically adjusting load capacitance of its Pierce oscillator.

In this work, we demonstrate the elimination of XO and regular-bandwidth PLL for BLE by resorting to a 32.768kHz real-time clock (RTC) that is ubiquitous in IoT hosts for RX/RX scheduling (<200ppm frequency accuracy is now widely available in RTC). As the resulting max PLL bandwidth is 1kHz or so, settling-time response to hopping channels would be comparable to the packet length of ~0.5ms, thus making it impractical. We choose to replace the conventional channel settling with a band settling (see Figure 28.4.1 top) that would be carried out only once per global device power up. The ADPLL would always stay tuned to the center channel (CH=20 @2440MHz) and perform the combined channel hopping and FM modulation by instantaneously offsetting the DCO resonance from the center channel via a 2-point modulation [6]. During periodical sleeps, the oscillator tuning word (OTW) registers will be saved in order to restore the same center-channel frequency at wakeups. Since the bandwidth (ΔfR/KDCO) of typical BLE is 1kHz or so, the channel span of ±250kHz will be compensated. The ADPLL bandwidth in all measurements is 1.3kHz.

Figure 28.4.5 further shows the measured PN. As the ADPLL bandwidth is 32.768kHz/(2·2^n) = 1.3kHz, its effect cannot be visible at the minimum measured offset of 10kHz. However, the low 1Md° corner of 140kHz is clearly discernable. The measured jitter within 100kHz to 1GHz is 1.3ps. The TDC resolution is 8.6ps at 0.4V supply to the doubler and rises to 16.6ps at 0.3V. The total ADPLL power consumption PdC = 0.923mW at 0.45V, the 2.1-to-2.5GHz, -104dBc/Hz (@1MHz offset) DCO dominates 70% of PdC. The entire digital logic is clocked at 32.768kHz and draws only 6% of PdC.

Figure 28.4.6 summarizes the performance and compares it to state-of-the-art BLE PLLs. The key breakthroughs here are: 1) ultra-low-voltage operation at ±0.45V; 2) the elimination of conventional XO as REF in favor of a 32kHz RTC; and 3) near-instantaneous channel hopping, while maintaining the best-in-class performance compared to the those in Fig. 28.4.6 at sub-mW power consumption. The die photo is shown in Figure 28.4.7.

Acknowledgments

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References

Figure 28.4.1: Mechanisms of instantaneous channel hopping, DCO gain calibration through hopping perturbation, and GFSK data modulation.

Figure 28.4.2: Block diagram of the proposed ADPLL. (In bold are the newly introduced blocks w.r.t. conventional ADPLL, e.g., [1].)

Figure 28.4.3: The DCO schematic and non-linearity compensation schemes.

Figure 28.4.4: Measured spectral GFSK frequency modulation (top-left), full-band hopping (top-right), three-channel hopping (bottom-left), and settling w/i & w/o DCO compensation (bottom-right).

Figure 28.4.5: Measured hopping settling time, phase jitter, TDC resolution and power consumption.

Figure 28.4.6: Performance summary and comparison with state-of-the-art.
Figure 28.4.7: Die micrograph of the ADPLL. The core size is 0.24mm².
28.5 A 0.2V Energy-Harvesting BLE Transmitter with a Micropower Manager Achieving 25% System Efficiency at 0dBm Output and 5.2nW Sleep Power in 28nm CMOS

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Massive deployment of wireless sensor tags (e.g., iBeacon) will only happen if batteries and their replacement effort are avoided. Self-powering by harvesting the ambient energies like indoor solar and thermal gradient is prospective[1], but their inconstant sub-0.5V output hinders their utility. Adding boost converters and regulators inevitably worsens the system efficiency and integration level. This paper reports an energy-harvesting Bluetooth Low-Energy (BLE) transmitter (TX) (Fig. 28.5.1). It features a fully integrated micropower manager (µPM) to limit the sleep power and tolerate variation of the energy-source voltage (VDD,down) down to 0.2V. U-An ultra-low-voltage (ULV) VCO and PA, and a passive-intensive type-I PLL are proposed. Fabricated in 28nm CMOS, the TX exhibits a 25% system efficiency at 0dBm output (Pout).

The TX (Fig. 28.5.1) tailors a µPM with 4 specific charge pumps (CP1-4) to deliver 3. Since the VCO plus PA dominate 99% active power, ULV designs allow them to calls for a big C de compromising the area and startup time. The ring-VCO, using voltage VD of M1,2 set by VDD,EH. Differential-mode oscillation is achieved by source-ULV VCO (Fig. 28.5.3-left) removes the drain-to-gate feedback for a constant drain VCO has out-phased VGS and VDS, its cross-coupled pair is pushed into the triode transformer.. The transformer has a primary coil (LA11,12) stacked atop its secondary coil (LB21,22) to enlarge both the coupling factor (kA≈0.76) and turns ratio (N1,2=5.6×N3,4). The VCO hence shows a large passive loop gain proportional to kN2,4 even in the presence of source degeneration. In active mode, M1,2 has a gate bias Vbias (0.39V) given by the BGR that further facilitates startup of the crystal oscillator [1].

The trifilar-coil VCO [2] features a large passive loop gain to facilitate startup at ULV. Yet, the VCO steady-state power consumption is decided by both the loss of the LC tank and transistor channel conductance (Gm). Since the trifilar-coil VCO has out-phased Vctrl and Vout, its cross-coupled pair is pushed into the triode region, resulting in large Gm and power consumption especially at ULV. Here, our ULV VCO (Fig. 28.5.3-left) removes the drain-to-gate feedback for a constant drain voltage VD of M1,2 set by VDD,EH. Differential-mode oscillation is achieved by source-to-gate magnetic cross-coupling (Vctrl to Vout and Vctrl to Vctrl). Unlike [3], an auxiliary cross-coupled pair is not entailed at the gate, which otherwise penalizes the phase noise (PN) by ~2dB in the 1/f region (even with a size of one-tenth of W/L). Since Vctrl and Vout (Vctrl and Vctrl) are in-phase, they lead to a large Vctrl (−0.78Vctrl) improving the PN, and can serve as the VCO outputs. The reduced Vctrl (−0.51Vctrl) helps M1,2 to stay in the saturation region, avoiding Q degradation of the transformer. The transformer has a primary coil (L11,12,13,14) stacked atop its secondary coil (L21,22) to enlarge both the coupling factor (kV=0.76) and turns ratio (N1,2=5.6×N3,4). The VCO hence shows a large passive loop gain proportional to kN2,4 even in the presence of source degeneration. In active mode, M1,2 has a gate bias Vbias (0.39V) given by the BGR that further facilitates startup at ULV. DC isolation between Vctrl and VDD,EH improves the frequency pushing (measured 29.7MHz).

The 2.4GHz VCO outputs (Vctrl) directly drive the ULV PA (Fig. 28.5.3-right) that operates in the Class-E/F mode to enhance the power efficiency. To meet a 0-dBm Pout at 0.2V, we exploit a step-down transformer (L13,14) to reduce the drain-node swing of M1,2 while rejecting the even-order harmonics at Vout. To suppress the HD2 without adding an explicit LC filter, C1 (0.70pF) is embedded into the secondary coil (L21,22) to resonate with a part of its inductance (L21,22) at 3× of the 2.4GHz ISM band: 3ω = 1/(2×C1). As such, [3] of the PA will present a high impedance at 3ω to boost the 3×harmonic current. L2 is routed as the most inner 2 turns of L21,22 (Fig. 28.5.7), with its dimension (D1,2) being designed to balance the HD2 and PA efficiency. Simulations suggest that D1=100μm aids balancing HD2 (−47dBm) and PA efficiency (30.6%) at Pout=0dBm. Comparing with no L1,2, HD3 is rejected by 19dB more (Fig. 28.5.3-right). The passband loss rises only 0.5dB, since the magnetic coupling between L1,2 and L2 is dominated by their outer turns. In sleep mode, the shared gate bias (Vbias) of the VCO (M1,2) and PA (M3,4) is switched to VR (−0.17V) optimized for leakage power reduction (measured 3.9μW). The VCO can be switched to the receiver mode by shutting down the PA via SSW.

The VCO is locked by a type-I integer-N PLL with VR=0.55V and f30=1MHz to support channel selection (Fig. 28.5.4). With a passive XOR gate + an inverter-based buffer, VCTRL is rail-to-rail pulses and hence a 0- to 0.55V VCTRL range for frequency tuning is realized. Unlike [4] that uses 50% duty-cycle φ1 to drive the master-slave sampling filter (MSF), here φ2 utilizes a 10× less duty cycle (i.e. 5%) to reduce the ripple of VCTRL, mainly induced by the clock feedthrough from VCTRL which aids in suppressing the reference spur. It can be quantified by analyzing the 1st-harmonic Fourier coefficient of VCTRL. Meanwhile, the XOR gain varies with VCTRL, and has a simulated minimum gain improved from ~0.03 (50% φ1) to 1.21V/1rad (5% φ2), which expands the loop bandwidth to better suppress the VCO PN. During open-loop FM modulation, S2 is off and S1 is on. Thus, C1,2 are in parallel (26pF) to reduce the VCTRL leakage. The swing of φ2 is bootstrapped to lower the size of S1,2 (transmission gates) The PLL excluding the VCO dissipates 30μW mainly for the divider.

The TX fabricated in 28nm CMOS satisfies the strict minimal density rules. Under open-loop modulation, the TX shows a system efficiency of 25% at Pout=0dBm and VDD,EH=0.2V, and 27% at Pout=3.7dBm and VDD,EH=0.3V (Fig. 28.5.5). A single-tone Pout of 0dBm shows HD2=−49.6dBm and HD3=−47.4dBm. The BLE spectral mask is met and FSK error is just 2.2%. The frequency drift is <5kHz when delivering a 425μs BLE packet. The free-running VCO shows a FOM of 188.4dB when VCTRL is raised. The forward diodes at VDD,PM are for overdrive protection. Self-powering by harvesting the ambient energies like indoor solar and thermal gradient is prospective[1], but batteries and their replacement effort are avoided. The authors thank Macau Science and Technology Development Fund (FDCT) - SKL Fund and University of Macau - MYRG-2015-00097-AMS for financial support.

References:
[6] X. Peng et al., “A 2.4-GHz ZigBee Transmitter Using a Function-Reuse Class-F DCO-PA and an ADPLL Achieving 22.6% (14.5%) System Efficiency at 6-dBm (0-dBm) Pout,” IEEE JSSC, vol. 52, pp. 1495-1508, June 2017.
Figure 28.5.1: Proposed energy-harvesting BLE TX features a fully-integrated μPM to control the active/sleep power and tolerate variation of the energy source (VDD,EH) down to 0.2V.

Figure 28.5.2: Left: CP, of the μPM. Its ring-VCO is locked via tunable delay lines to track VDD,EH variation. Right: Measured internal voltages against VDD,EH and their startup time.

Figure 28.5.3: Left: ULV VCO with M1,2 always in saturation region even at VDD,EH=0.2V. Right: ULV Class-E/F PA, with its transformer-embedded L1,C1 notch to suppress HD3.

Figure 28.5.4: A 2.4GHz integer-N type-I PLL with passive XOR and MSSF. The MSSF uses a 5% duty-cycle \( \Phi \) to aid suppressing the reference spurs. VDD,PLL=0.55V and fref=1MHz.

Figure 28.5.5: Upper: measured \( P_{\text{out}} \), power efficiency and LD3,4. Lower: measured modulated output spectrum, FSK error and frequency drift under open-loop operation.

Figure 28.5.6: Benchmark with the recent art. This work and [5-7] use open-loop modulation.
Figure 28.5.7: Die micrograph of the 28nm CMOS BLE TX and details of transformers. Extra pads are for individual characterization of the pPM, VCO and PA in active and sleep modes.
Event-driven sensor nodes have applications in agriculture, infrastructure, and perimeter monitoring and are characterized by spending the vast majority of their time in an asleep-yet-alert state. In this state, the node must wake to incoming RF wakeup commands from an antenna with minimal dc power, as the total percentage of power in sleep mode dominates if wakeup events are sufficiently infrequent. The RF wakeup receiver (WuRX) is a critical block of the node’s asleep-yet-alert state. It must maximize sensitivity with power consumptions of 10nW or less to maximize battery lifetime or even enable battery-less systems that persist on energy harvesting [1-3]. These WuRXs must reliably detect wakeup signals as well as reject false wakeups caused by external interferer signals or noise. Otherwise, booting the full node into its active state when it is not needed can quickly relinquish power savings created by the wakeup radio in its asleep-yet-alert state.

In this work, we present a WuRX that achieves -76dBm sensitivity in the 151.8MHz MURS band and -71dBm sensitivity in the 433MHz ISM band while consuming 7.4nW dc power. This is enabled by several innovations, including a passive envelope detector (ED) that minimizes the input noise-equivalent power (NEP) of the RF front-end, high-sensitivity amplifier–correlator stages that host a fully automated offset-control algorithm that operates even when the RF channel is quiet, a digital correlator to provide additional discrimination from external interferers or wakeup signals, and a low-frequency bandpass IF path to limit noise into the comparator while providing robustness against external interference. Figure 28.6.1 shows the receiver block diagram.

The CMOS RF front-end is co-designed with a discrete tapped capacitor transformer to maximize the signal-to-noise ratio at the output of the ED (Fig. 28.6.2). The achievable passive voltage gain of the transformer is limited by the inductor’s shunt conductance, so minimizing the input capacitance of the ED by reducing the number of detector stages enables the use of larger, higher-quality-factor inductors with larger shunt conductance for optimal voltage gain. On the other hand, increasing the number of stages in the detector increases its voltage sensitivity ($V_{sensitivity}$), output impedance as well as output noise level. Device voltage threshold also enables a tradeoff between input impedance, voltage sensitivity, and bandwidth [4]. Output thermal noise levels of active envelope detectors such as common-source and common-gate architectures degrade considerably at extremely low bias currents (Fig. 28.6.2). Thus, noise performance of passive (Dicken) detectors becomes superior when currents are restricted to less than several hundred nA. Additionally, passive detectors with zero-bias diode-connected transistors have no flicker noise, erasing the tradeoff between flicker-noise corner frequency and input impedance. This ED was optimized for the 151.8MHz band, where a 45-stage, low-threshold voltage-device ED provided minimum NEP of 170fW/Hz in simulation with an overall measured voltage sensitivity from the 50Ω input to the output of the detector of 15.2mV/nW. To demonstrate the broadband nature of the CMOS chip itself in other bands, a second transformer was designed, implemented, and measured for the 433MHz band, achieving a voltage sensitivity of 6.4mV/nW (Fig. 28.6.2). The 3dB bandwidths of the 151.8MHz and 433MHz transformers are 3MHz and 11MHz respectively.

The IF signal is amplified and digitized through a high-sensitivity ground-referenced baseband amplifier followed by a clocked comparator. The baseband amplifier is a modified cascode amplifier where the input stage is replaced with a common-drain PFET to allow for a ground-referenced amplifier. It takes advantage of ac coupling between the amplifier and comparator as well as a zero-pole pair created by using self-biasing of the gates of the common–gate and load transistors to enable an analog bandpass frequency response with a low-frequency cutoff of <1Hz and a high-frequency cutoff of 0.2Hz, which can be tuned through a digitally controlled capacitor bank ($C_t$) to match the frequency response of the ED while suppressing out-of-band noise (Fig. 28.6.3). One additional benefit of the IF bandpass frequency response is that it suppresses many interferer signals. The amplifier provides high simulated passband gain of 25dB while consuming 2nW.

The clocked-comparator sample consists of a preamplifier with a PFET input stage with one input referenced to ground and the other input driven by the output of the RF front-end (Fig. 28.6.3). The cross-coupled inverter pair provides regenerative feedback. When CLK=0, the comparator is reset. When CLK=1, the comparator enters into evaluation mode where it samples the incoming signal that gets latched during the rising edge of φ. The comparator threshold is controlled through 6b of fine-grained control bits, which are set by the automatic offset-control loop with minimum step size of ~280µV. Three bits of coarse-grained digital control set the range of the comparator threshold. For instance, with a coarse setting of 000, the simulated comparator threshold ranges from -6mV to 35mV.

A fully-integrated automatic offset-control algorithm allows for optimal operation in the presence of on-off keyed (OOK) RF interferer signals, and it supplies self-calibration to overcome PVT variations. One significant challenge for event-driven WuRXs is that the entirety of the offset control must be accomplished in the absence of an RF signal. For receiver power levels below 10nW, an on-chip RF calibration source also is not feasible, so the offset of the comparator must be set from information available in the RF off state. The compensation loop, shown in Fig. 28.6.4, sets the comparator offset to a level that provides a desired false-positive rate (at the output of the comparator) for a trade-off between low false-wake-up rate (at the output of the correlator) and high sensitivity. In this work, the false-positive rate is set to be 1.5% to achieve a false-wake-up event rate of <1/hr.

An 8b shift-register-based correlator with programmable error tolerance was implemented with subthreshold logic to minimize dc power (Fig. 28.6.4). Given the asymmetry of the incoming signal that is zero until a wakeup signal is sent, the error correction tolerates differing levels of false positives and false negatives from the comparator and still issues a wakeup signal. This helps suppress system false wakeups, which otherwise increase at lower threshold offset words. The wakeup signal is two back-to-back 8b OOK codes separated by a half-clock-cycle delay to account for possible phase mismatch between the transmitter and receiver. The on-chip clock consists of a five-stage current-starved ring-oscillator architecture. External voltage biases $V_{cc}$ and $V_{dd}$ control the frequency of the clock source from 0.1kHz to 10kHz and draw <0.1nW.

Wakeup sensitivity of -76dBm, with 10% probability of missed detection and false-wake-up rate <1/hr is achieved using the full wake-up code including the correlator with no synchronization and a symbol bit rate of 0.2kb/s (Fig. 28.6.5). The offset word is fixed to ensure constant voltage threshold throughout this measurement. Receiver false wakeups are observed when -76dBm -68dBm detection threshold at a -30dB carrier to interferer ratio (CIR) constant envelope interference with a 3MHz offset from the signal. The rectified CW signals produce a dc offset at the output of the envelope detector and thus are blocked by the bandpass response of the baseband amplifier before even reaching the comparator. The limitations on the CIR is sufficiently large dc offsets output of the envelope detector to drive the baseband amplifier into a different biasing region where the small wake-up signal on top of the dc offset no longer has enough gain.

A more challenging form of interference to block is from non-constant envelope interferers with similar RF and IF frequencies as the desired wakeup signal that can pass through both the RF input filter as well as the IF baseband amplifier. These types of interferers will be incident on the comparator and must be blocked either through offset control at the comparator or through digital error correction when the envelope interferers with automatic offset control enabled is shown in Fig. 28.6.5. A successful -75dBm wakeup signal is observed in a quiet environment. After a -86dBm 0.1 kb/s OOK signal 3MHz away briefly causes an elevated false-positive rate at the comparator, the offset control automatically raises the threshold. Rather than being unusable, the WuRX remains functional the entire time, though at a lower sensitivity, as the final -72dBm wakeup signal shows, with no false wakeups occurring even under such challenging interference conditions. The DC power of the system is 7.3nW and its performance is compared to state-of-the-art WuRXs in Fig. 28.6.6, showing 7dB improvement over prior sub-10nW WuRXs. Figure 28.6.7 shows die and PCB photos of the WuRX.

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References:
**Figure 28.6.1:** Block diagram of the wakeup receiver showing waveforms from RF input through digital wakeup output.

**Figure 28.6.2:** Comparison between active and passive envelope detectors and measured performance of RF front-end at 151.8MHz and 433MHz.

**Figure 28.6.3:** Schematics of baseband amplifier and comparator and their simulated gain, noise and offset response.

**Figure 28.6.4:** Automatic-offset-control algorithm, measurements showing automated control over comparator false-positive rate and correlator schematic.

**Figure 28.6.5:** Measurements of receiver sensitivity, dc power consumption and automatic-offset response to non-constant envelope interferers.

**Figure 28.6.6:** Summary of performance and comparison with state-of-the-art.
Figure 28.6.7: Die micrograph and PCB photo of the wakeup receiver.
28.7 A 14.5mm² 8nW -59.7dBm-Sensitivity Ultrasonic Wake-Up Receiver for Power-, Area-, and Interference-Constrained Applications

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The mm-sized sensors of the Internet of Things is envisioned to include unobtrusive, distributed mm-sized nodes capable of sensing and communicating information about their surroundings. Wake-up receivers (WuRXs) – ultra-low-power receivers that monitor their environment for a wake-up signature – are an important part of this vision, as they can extend the lifetime of a wireless node by keeping it asleep until interrogated. The state of the art in WuRXs, measured in terms of sensitivity and power, has recently been advanced by streamlining the signal path to include fewer power-hungry gain stages and instead obtaining the gain at the chip-antenna interface [1, 2]. This has led to excellent power-sensitivity performance, but the accompanying increase in size hampers the applicability of these techniques in size-conscious applications, such as surveillance, asset tracking, and ubiquitous sensing. Moreover, size-reduction methods based on RF antenna miniaturization are fundamentally limited by high antenna Qs at low size-to-wavelength ratios [3]; efficiently matching to these antennas requires, in turn, high-Q passives that are generally unavailable at mm-scale.

To overcome this fundamental size-sensitivity tradeoff, this work proposes an ultrasonic (US) WuRX based on a precharged capacitive micromachined US transducer (CMUT), similar to those presented in [4]. Signature detection over US rather than RF allows this work to improve upon prior art by 7.6dB in terms of a combined sensitivity-power-area metric in the following ways: the CMUT-chip interface is naturally high-impedance (~200kΩ), resulting in higher voltage for a given incident power and leading to -59.7dBm sensitivity; the high-impedance, low-frequency environment obviates the need for active gain at RF, allowing for 8nW power consumption; and the small CMUT size (on the order of the US wavelength) and absence of off-chip matching allow the WuRX to be implemented in 14.5mm², which is significantly smaller than the active area (chip + antenna/transducer) of prior RF- and US-based works [5, 6]. Using US also makes the system insensitive to RF interference, while the narrowband (NB) CMUT and on-chip signature detector reject acoustic noise and interferers, as shown by measurements. Multiple, partially-overlapping signatures allow hierarchical classes of wake-up, leading to greater flexibility in a network tree protocol. At the system level, unlike RF, US has no EIRP limit in air, enabling greater range at the same intensity by increasing transmitter aperture (ultimately limited by intensity regulations at the WuRX).

Figure 28.7.1 shows the chip block diagram. The CMUT output connects directly to a ripple-canceling envelope detector (ED), whose DC output is compared to a pseudoresistor ladder-based reference voltage by a low-noise comparator clocked by a relaxation oscillator (fclk = 1.344kHz). The comparator output is clocked into a variable-length detector that looks for one of multiple selectable signatures and outputs a 0.5V wake-up pulse upon signature recognition. The reference ladder is calibrated once, upon startup.

To limit power consumption and area, the chip uses neither closed-loop timing recovery nor a crystal. Meanwhile, the CMUT needs ~Q cycles to ring up, during which time the ED output is not necessarily valid. The accompanying timing issues are solved by oversampling the data. By conditioning on the bit arrival time relative to the last clock pulse, the missed-detection rate (MDR) can be derived as a function of timing uncertainty (drift and jitter), signature length, and sampling rate. As shown in Fig. 28.7.1, sampling the incoming data at 4× the bit rate allows almost full use of the CMUT bandwidth for an MDR of 10⁻³, at timing uncertainties realizable without a crystal. The design of the Schmitt trigger-based relaxation oscillator takes advantage of 4× oversampling by being optimized for low power rather than high accuracy; an 8b capacitor bank allows frequency trimming upon startup.

To further reduce power, the CMUT output is directly fed into a low-power ED, shown in Fig. 28.7.2. One of the challenges posed by operating at such a low carrier frequency (57.7kHz) is the high ED output ripple, which limits the WuRX sensitivity if not addressed. A ripple-canceling topology is therefore implemented, in which the outputs of a common-source and common-gate stage are combined before being fed into the comparator. Because the linear gain (A_{fundamental}) of these stages has opposite sign while the conversion gain (A_{conversion}) has the same sign, the carrier amplitude at the output is reduced by ~44dB (simulated) compared to an ED based on a single common-source stage. As shown in Fig. 28.7.2, this improves the frequency-ripple tradeoff to the point that the ripple becomes smaller than the noise of this stage. Ratiometric biasing in the ED mitigates the effect of PMOS pseudoresistor variation on operating point; the one bias point not set ratiometrically is adjusted with one-bit control to result in the correct sign for A_{conversion} over process variations.

The output of the ED is compared to a ladder-based reference by a self-timed comparator based on a double-tail latch, a topology chosen for its low headroom and wide input common-mode range (important due to process variation in ED output bias point). As shown in Fig. 28.7.3, to avoid an incomplete comparison, only once the outputs of the comparator are valid are its tail transistors turned off, and it is reset only at the next clock pulse. Because the comparator spends the majority of each clock cycle idling, leakage power is a potential concern; this is addressed by using thick-oxide tail devices, limiting leakage to 290pW.

The comparator output is clocked into a DFF-based detector that compares sequences of every fourth bit (in accord with 4× oversampling) to one of four hard-coded signatures. To enable hierarchical wake-up networks in which security and privacy settings are built-in at the chip level, these signatures are designed to partially overlap: each child signature contains at least one parent signature, so that child nodes cannot be awaken without also waking up parent nodes within range. Proof-of-concept wireless measurements demonstrating a parent-child wake-up scenario, as well as more detail about signature hierarchy, are shown in Fig. 28.7.4.

The proposed WuRX chip was fabricated in TSMC 65nm CMOS GP technology, runs on 0.5V, and measures 1mm×1.5mm. Figure 28.7.5 shows the wireless test setup and results. For each test, incident pressure was determined by combining the CMUT voltage with sensitivity data previously collected using a calibrated microphone (GRAS 40DP); incident power was then calculated by combining pressure with CMUT area. Synchronized BER tests establish operation at nominal sensitivity; unsynchronized MDR tests show sensitivity within +/-0.5 dB of BER results, indicating that 4× oversampling effectively mitigates detection errors due to timing uncertainty. Bandwidth, carrier-to-interferer (CIR), and carrier-to-noise (CNR) measurements indicate robustness of the US WuRX to close CW interferers and NB noise; slight increases in BER over a short CIR range for some values of Δf likely stem from the probabilistic nature of BER measurement at the chosen data sequence length. Long-range test results show wireless functionality in an outdoor setting with ambient noise and a strong 25kHz interferer. Preliminary variability measurements for 20 chips from a single lot, taken electrically at a lower data-rate (62.5b/s) and slightly higher Vdd (0.6V) than nominal, indicate consistent performance (sensitivity: μ = -58.4dBm, σ = 1.6dBm; power: μ = 7.3nW, σ = 0.9nW).

Figure 28.7.6 shows that the proposed WuRX improves upon the state of the art by 7.6dB, has the smallest active area among works that include an antenna/transducer, and is supported by wireless tests and interferer measurements. This work thus demonstrates that using an ultrasonic wake-up medium enables miniaturized, long-range, low-power WuRXs that are competitive with RF-based solutions. Photos of the chip die and precharged CMUT are shown in Fig. 28.7.7.

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The authors thank Prof. B. T. Khuri-Yakub and M.-C. Ho for fabrication and provision of precharged CMUTs, and Mentor Graphics for the use of the Analog FastSPICE (AFS) Platform. This research was conducted with Government support provision of precharged CMUTs, and Mentor Graphics for the use of the Analog FastSPICE (AFS) Platform. This research was conducted with Government support.

References:
**Figure 28.7.1:** US WuRX block diagram; precharged CMUT electrical properties; choice of data and sampling rates.

**Figure 28.7.2:** Hybrid CS-CG ripple-cancelling ED: schematic, ripple reduction, performance under process variation.

**Figure 28.7.3:** Self-timed comparator is off for most of clock period; thick-oxide tail devices minimize leakage.

**Figure 28.7.4:** Signature detector looks for one of many hierarchical signatures, as wireless tests demonstrate.

**Figure 28.7.5:** Wireless tests show US WuRX functionality across signatures and with noise and interferers present.

**Figure 28.7.6:** Comparison plot and table; latter includes recent works pushing sensitivity, power, and often area.
Figure 28.7.7: Micrograph of proposed chip sitting on a precharged CMUT; simulated chip power-draw breakdown.
A 5.8GHz Power-Harvesting 116μm×116μm “Dielet” Near-FIELD Radio with On-Chip Coil Antenna

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The proliferation of the Internet of Things (IoT) and low-power sensors would benefit greatly from batteryless compact radios that require no external components. Such a radio could be used for future RFID, wearables/implantable devices, and counter-counterfeit electronics. Previous demonstrations have focused primarily on miniaturizing the radio size [1, 2], but relying on off-chip antennas. Two challenges must be overcome to enable sufficiently small radios with on-chip antennas [3]: 1) In most state-of-the-art radios [3-6], the device antenna is connected to both the downlink signal path and the power management unit. Relying on separate signal and power paths incurs an area penalty and degrades antenna matching. In addition, it would be difficult to get a high downlink data-rate since the weak power transfer cannot be disturbed by communication data with a high-index modulation. 2) The ultra-small die area precludes the use of any on-chip energy storage (such as large capacitors or inductors) or a large antenna, so sufficient power must be supplied wirelessly. The wireless power tone acts as a large blocker for the uplink communication signal, resulting in a poor uplink signal-to-noise ratio (SNR) and signal-to-blocker ratio (SBR). In [4], the radio dimension was reduced to 500μm×250μm, but the achieved uplink SNR was only 10dB. To circumvent the blocker issue in the uplink, dual antennas were adopted in [5] and [6] to split the wireless power tone and uplink tone into two frequencies, resulting in a die area larger than 4.4mm².

We have demonstrated an RFID system used to detect counterfeit electronics that addresses the design challenges in several ways: 1) On the downlink, the power-transfer path is reused for data communication, minimizing chip area. The wireless power signal is transmitted as ASK with <4% modulation index, minimally impacting the delivered power. Instead of directly connecting a demodulator to the antenna [3-6], the AC-DC rectifier serves as the demodulator followed by an ASK detector, so it does not load the antenna. 2) For the uplink, we propose a hybrid 2nd-3rd-order intermodulation injection-locking (HIMIL) technique, where a two-tone waveform is generated by a reader for power delivery. A clean uplink carrier is produced by injection-locking the carrier oscillator (CO) on the radio chip to the 2nd-order intermodulation (IM2) of the two tones. Meanwhile, utilizing the 3rd-order intermodulation (IM3) as the uplink provides isolation from the two-tone blockers. As a result, both the uplink SNR and SBR can be significantly improved.

The system architecture is shown in Fig. 28.8.1, where the chip contains an on-chip coil antenna, an AC-DC rectifier, a power-on reset (PoR), a bandgap, LDOs, memory, and communication blocks. When the rectenna outputs a DC voltage VDC>0.85V to power up the chip, the bandgap generates a 0.8V reference voltage and 100mA constant currents IREF for all LDOs and submodules. As the ultra-small die area cannot fit sufficient decaps, separated LDOs are adopted to isolate the supply interferences among the submodules. During downlink, the two tones are set to the same frequency f1–f2=5.76GHz and phase, but f1 is modulated by the authentication data. The CMOS radio’s on-chip antenna picks up the <4% ASK signal, which is then rectified to produce data with an amplitude less than 4% of the VDC, requiring amplification by the subsequent ASK detector. After the radio chip authenticates the reader, the flag signal “TXEN” changes from 0 to 1 to initiate uplink.

The reader periodically enters uplink mode to check whether data is coming from the radio chip. Switching from downlink to uplink, the two tones generated by the reader separate to f1=5.76GHz and f2=5.728GHz. Due to the nonlinearity of the radio chip’s AC-DC rectifier, an IM3 tone 2f1–f2=5.808GHz is generated and transmitted to the reader. Meanwhile, the IM2 component f1–f2=40MHz is passed to the rectifier output VDC and then added to the reference current of the CO, as shown in Fig. 28.8.1. The CO is designed to be injection-locked to the 40MHz IM2, resulting in a low-noise strong carrier f2=20MHz, which improves the uplink SNR. The 4kHz clock generator is used to serially read data from an on-chip 4k-byte embedded memory (FB-written memory) that modulates the CO. The modulated carrier f1 is then mixed with the 5.808GHz IM3 tone. As a result, the uplink signal received by the reader is found at 2f1–f2+f1=5.828GHz, which is far away from the f1 and f2 blockers.

Figure 28.8.2 shows some of the key circuit details. The on-chip coil antenna is designed with patterned ground shield, taking a die area of 116μm×116μm, where all the circuits locate inside the coil. The antenna has an inductance of 4.83nH and a Q-factor of 14, whereas the frequency response of the rectenna indicates that the proposed two-tone technique can be supported with little influence on the power efficiency. The bottom path of the ASK detector (M3–M2 and Decap#2) forms an average filter, while the top path (M1–M0) pass the signal envelope, duplicating M3–M2 as M1–M0 to address PVT variations. Typically, VDD varies between 0.85V and 1.7V versus different powering ranges, so an extra diode M1 is added to support high input voltages. A comparator samples the data by comparing VDC and VREF, and two subsequent amplifiers increase the data amplitude. The 4kb/s data from the memory turns the CO on and off, whereas the CO is injection-locked to IM2 on the reference current. A Manchester data-rate of up to 5Mb/s must be supported during downlink (TXEN=0); therefore, the 1.6pF Decap#1 is isolated from the VDC and only the 1.2pF Decap#2 affects the signal. During uplink, Decap#1 is turned on to filter the switch-induced ripple at the rectifier output, i.e., the VDC node.

The testing platform is shown in Fig. 28.8.3. A probe station holds the radio chip in place to test the ranges and misalignment tolerance. For the downlink, the repeated Manchester serial number “00111010” is applied to the mixer to realize the ASK with a modulation index of 3.8%, and the output power of the PA is 32.406dBm, which only decreases the PA peak power by 0.024dB. Port#1 of the duplexer has a passband of 5.725 to 5.770GHz for downlink, whereas Port#3 has a passband of 5.805 to 5.850GHz for uplink. During the uplink, two wireless powering tones 5.768GHz/5.728GHz and the PA output noise at 5.828GHz can be filtered out at port#3, while the IM3 tone 2f1–f2=5.808GHz becomes the dominant blocker. The reader coil dimension is optimized for 1mm powering range. Given the small size of the “dielet”, even a 1mm distance represents a 9:1 ratio in range-to-dimension. In addition to the padless radio chip, a testing chip with pads was also implemented to check key signals such as TXEN, VDC, bandgap reference, and the CO frequency.

The measured wireless power transfer and the downlink communication results are displayed in Fig. 28.8.4. The harvested power and bandgap reference voltage are measured relative to the reader-to-chip range, and the digital authentication succeeds up to 1mm range. The harvested power at 1mm can reach 9.76μW, resulting in a power efficiency of 5.6x10⁻⁴. The results also show that the power efficiency drops by less than 40% at a misalignment of 0.2mm.

Figure 28.8.5 shows the uplink spectrum tested at Port#3 of the duplexer. At 0.8mm range, the chip’s CO cannot lock to the IM2, so no uplink signal shows up at 5.828GHz. As the range is shortened to 0.7mm, the CO is injection-locked by the 40MHz IM2, and an uplink signal appears at 5.828GHz with an SBR of -29.9dB. Without the two-tone configuration, the CO is free running at 23MHz, and the uplink signal displays a SNR less than 2dB even with downconverting noise cancellation. Using the proposed HIMIL technique, the uplink SNR is improved by 46dB. For the 4kb/s uplink, a 42dB uplink SNR is achieved.

Figure 28.8.6 summarizes this chip performance and compares with previous works. It shows that: 1) The 116μm×116μm radio is the smallest radio, and the die area is less than 11% of the state-of-the-art radios. 2) The chip achieves the best uplink SNR (42dB) by the new uplink concepts. 3) The downlink data-rate is only limited by the speed of previous sub-mm-sized near-field radios. The die micrograph is displayed in Fig. 28.8.7, where all the circuits locate under the patterned ground shield.

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References:
Figure 28.8.1: System architecture of "dielet" radio.

Figure 28.8.2: Detailed description of on-chip antenna, downlink ASK detector, and uplink IM2 injection-lock carrier oscillator.

Figure 28.8.3: Measurement setup and measured reader PA power for both one-tone downlink and two-tone uplink.

Figure 28.8.4: Measured results of wireless power transfer and downlink communication.

Figure 28.8.5: Measured uplink SBR and uplink SNR as well as the comparison with conventional backscattering result.

Figure 28.8.6: Performance comparison.
Figure 28.8.7: Die micrograph.