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SESSION 28

Wireless Connectivity

An 802.11ax 4×4 Spectrum-Efficient WLAN AP Transceiver SoC Supporting 1024QAM with Frequency-Dependent IQ Calibration and Integrated Interference Analyzer

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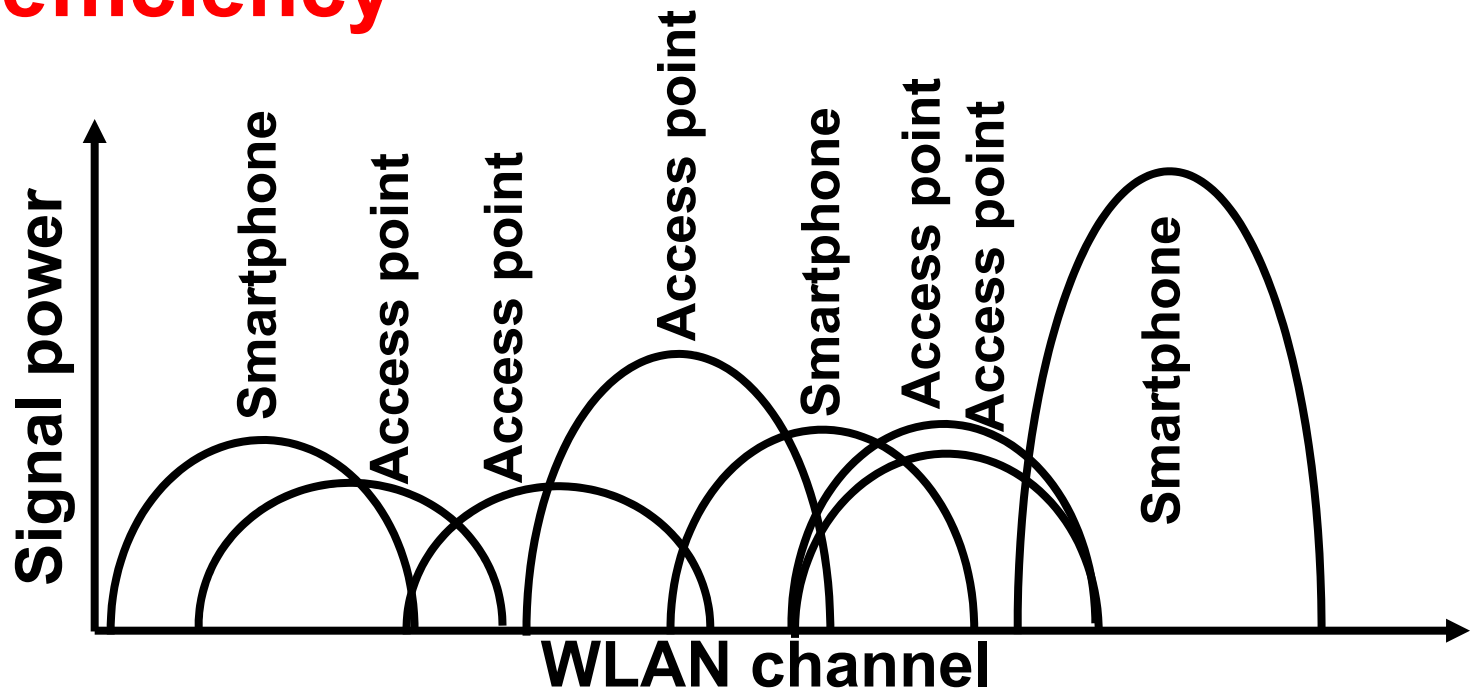
[3]Toshiba Memory, Kawasaki, Japan; [4]Toshiba Microelectronics, Kawasaki, Japan

Background

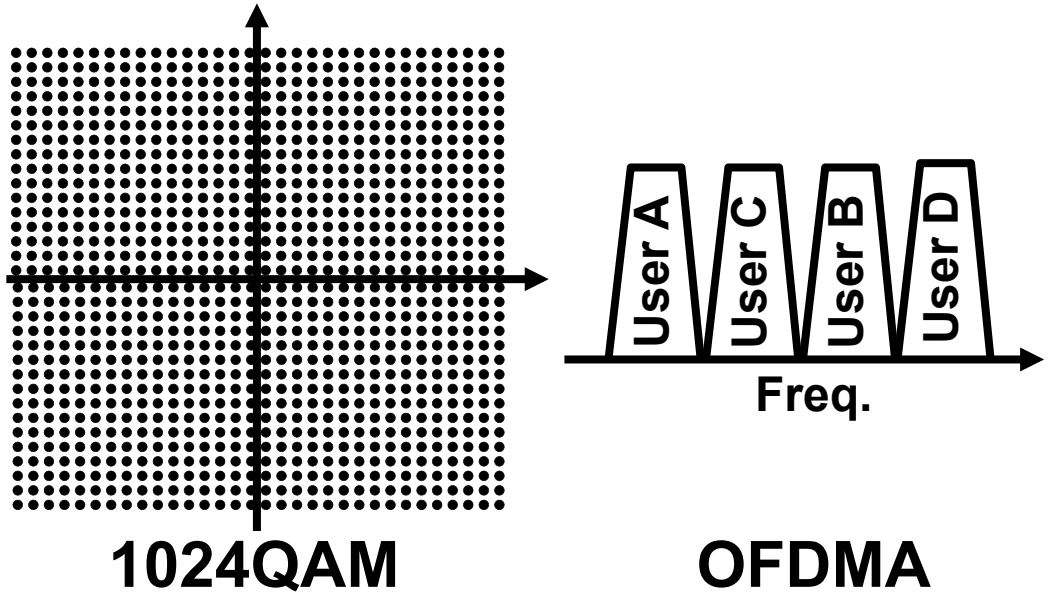
- Available frequency in 2.4GHz and 5GHz is limited
  - # of wireless devices is increasing in a dense environment
- WLAN next generation standard(IEEE802.11ax) improves spectrum efficiency



2.4GHz band's frequency usage in downtown

Features and challenges of 11ax

- **Features of 11ax**
  - **1024 (1K) QAM**
    - **High throughput in narrow band**
  - **OFDMA with non-contiguous CA**
    - **Spectrum efficiency is improved**



- **Challenges (EVM<-37 for 1KQAM)**
  - **Extreme IQ balance over the wide bandwidth (IRR<-50dB)**
  - **Low noise analog circuit (SNR>50)**
  - **Better isolation among TLs (<-50dB)**

Key techniques of proposed 11ax AP SoC

11ax features

- Frequency-dependent IQ amplitude calibration
- Low-noise pure-current-mode TXBB
- Isolated LO distribution circuit among transmission line
  - MIMO TRXs required long transmission line

Unique function of proposed SoC

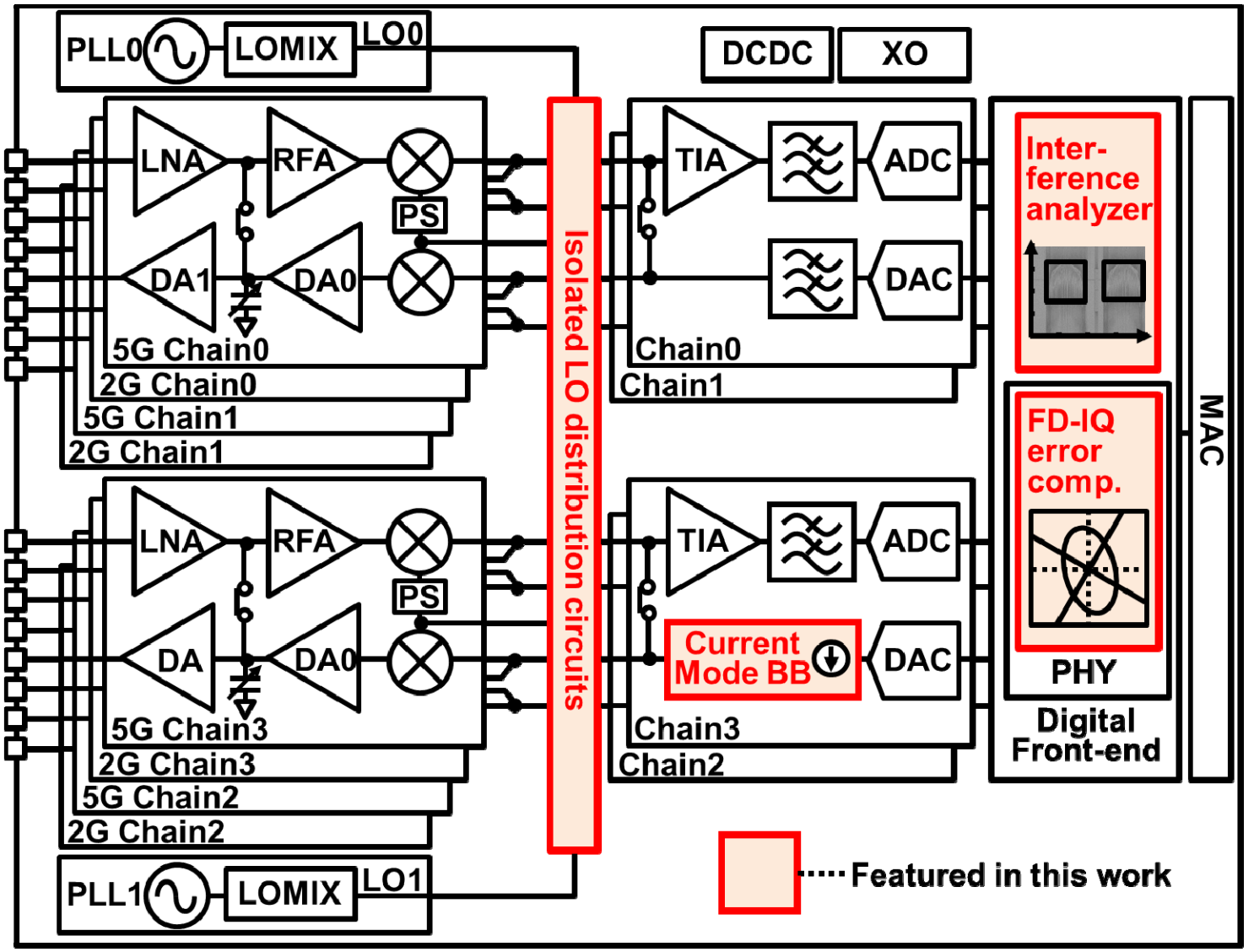
- Interference analyzer
  - Interference identification enables robust communication

Outline

- Background
- **Block diagram of proposed SoC**
- Frequency-dependent IQ error calibration
- Pure current mode TXBB
- Isolated LO distribution circuit
- Interference analyzer
- Measurement results
- Conclusion

Proposed 11ax AP SoC block diagram

- 4 TRX chains, 2 PLL
- IQ error compensator and current modes BB for 1K QAM
- Isolated LO circuit for non-contigiuous CA
- Integrated Interference analyzer to avoid interference



Outline

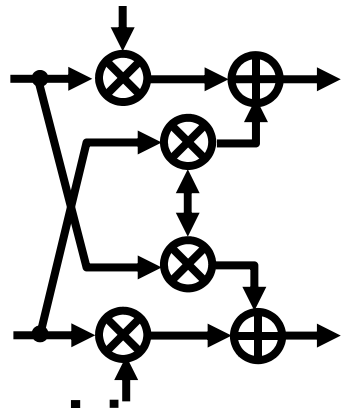
- Background
- Block diagram of proposed SoC
- **Frequency-dependent IQ error calibration**
- Pure current mode TXBB
- Isolated LO distribution circuit
- Interference analyzer
- Measurement results
- Conclusion

Conventional IQ error compensation method

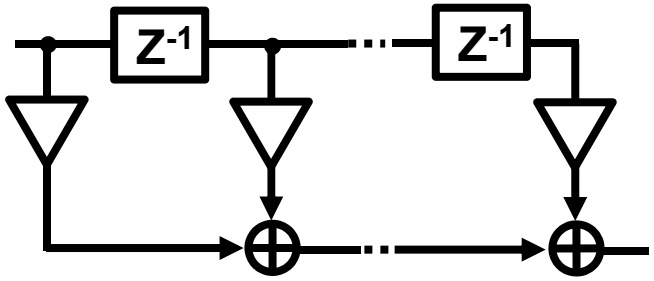
- Linear transformer and FIR filter compensates FI-IQ error and FD-IQ phase error
- Frequency-dependent IQ amplitude error is not compensated by using conventional method

Error compensation method

	Phase	Amplitude
Frequency-independent	Linear(affine) transformer	
Frequency-dependent	FIR filter	None☹



Linear transformer



FIR filter

Simple IQ error compensation matrix

- IQ error compensation matrix
  - α: amplitude error, β: phase error

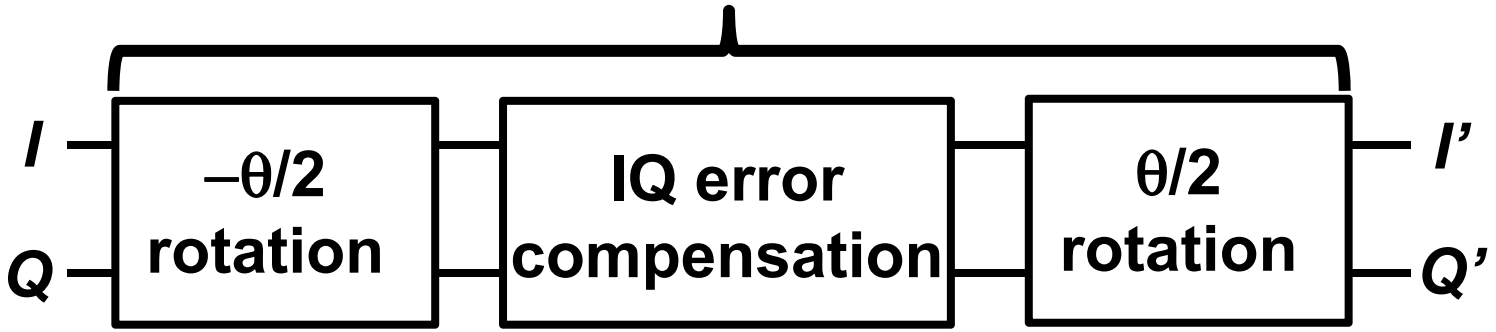
$$\begin{pmatrix} I' \\ Q' \end{pmatrix} = \begin{pmatrix} 1+\alpha & \beta \\ \beta & 1-\alpha \end{pmatrix} \begin{pmatrix} I \\ Q \end{pmatrix}$$

IQ amp./phase error conversion

- **Rotation circuit is sandwiched between compensator**
  - **Amp. error is converted from α to $\alpha\cos\theta - \beta\sin\theta$**
  - **Phase error is converted from β to $\beta\cos\theta + \alpha\sin\theta$**

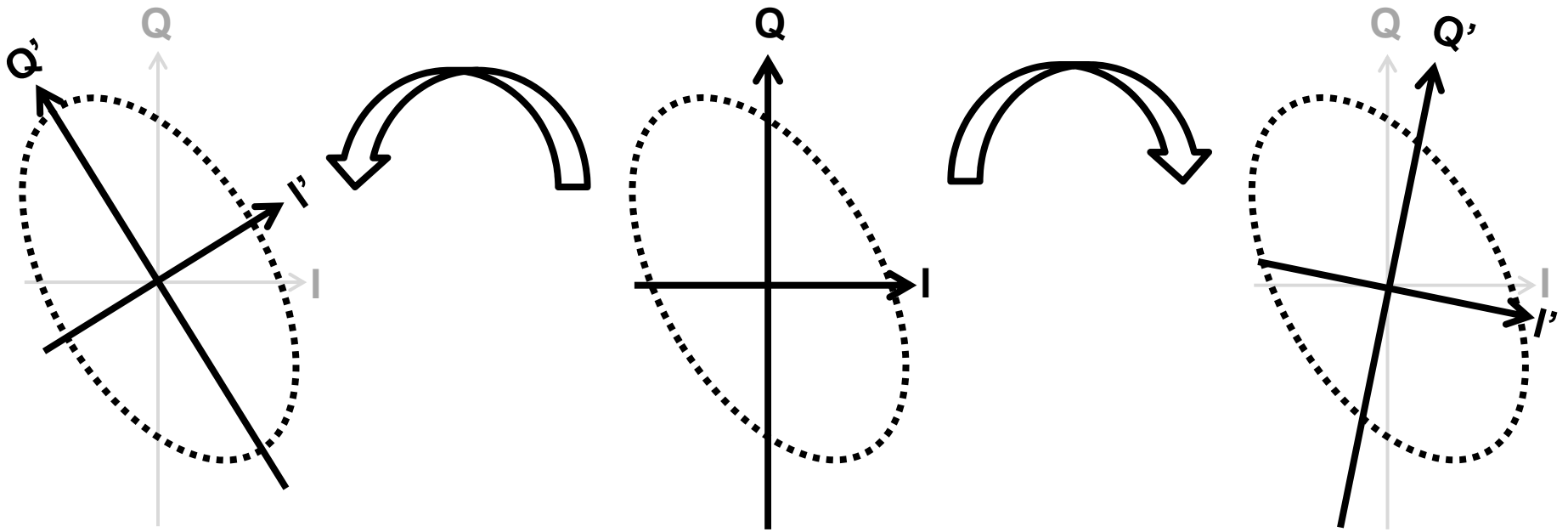
$$\begin{pmatrix} I' \\ Q' \end{pmatrix} = \begin{pmatrix} \cos\frac{\theta}{2} & -\sin\frac{\theta}{2} \\ \sin\frac{\theta}{2} & \cos\frac{\theta}{2} \end{pmatrix} \begin{pmatrix} 1+\alpha & \beta \\ \beta & 1-\alpha \end{pmatrix} \begin{pmatrix} \cos\frac{\theta}{2} & \sin\frac{\theta}{2} \\ -\sin\frac{\theta}{2} & \cos\frac{\theta}{2} \end{pmatrix} \begin{pmatrix} I \\ Q \end{pmatrix}$$

$$= \begin{pmatrix} 1+\alpha\cos\theta - \beta\sin\theta & \beta\cos\theta + \alpha\sin\theta \\ \beta\cos\theta + \alpha\sin\theta & 1-\alpha\cos\theta + \beta\sin\theta \end{pmatrix} \begin{pmatrix} I \\ Q \end{pmatrix}$$



Rotation effects

- IQ amplitude/phase error is converted to phase error only by rotating the optimum angle



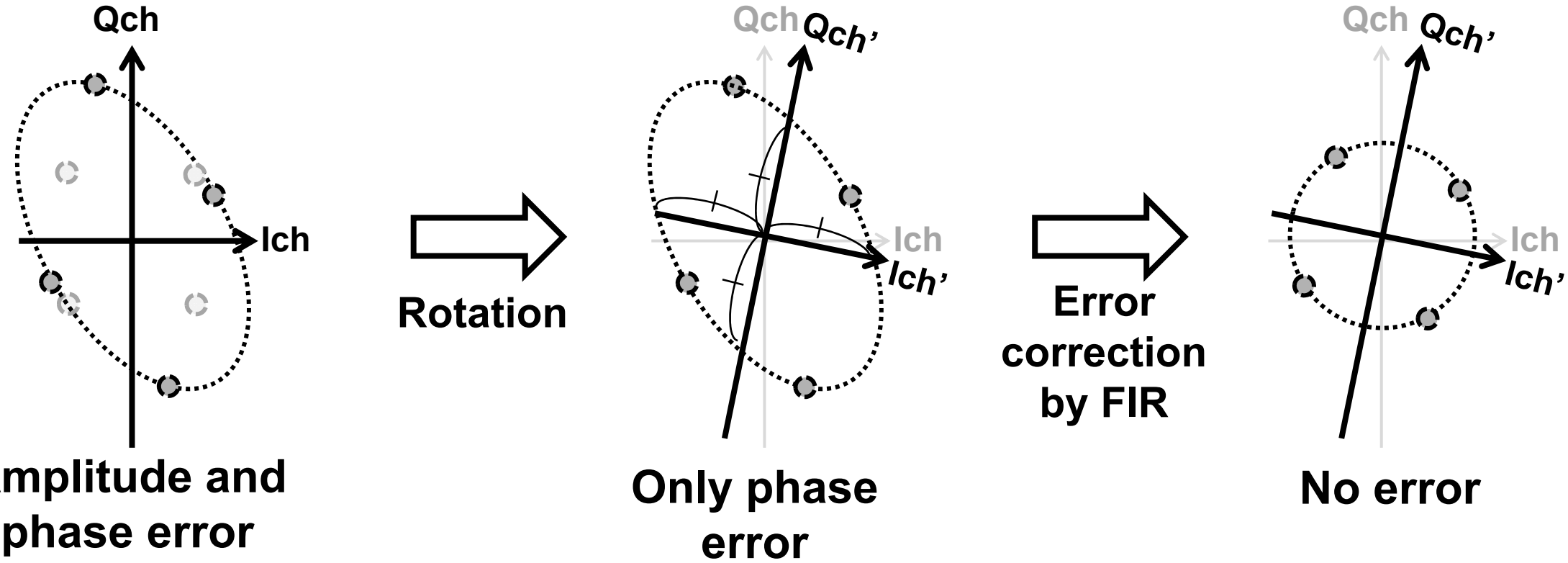
Only amplitude error

Amplitude and phase error

Only phase error

FD-IQ amplitude error correction

- **Cancelling both frequency dependence only in the phase domain**

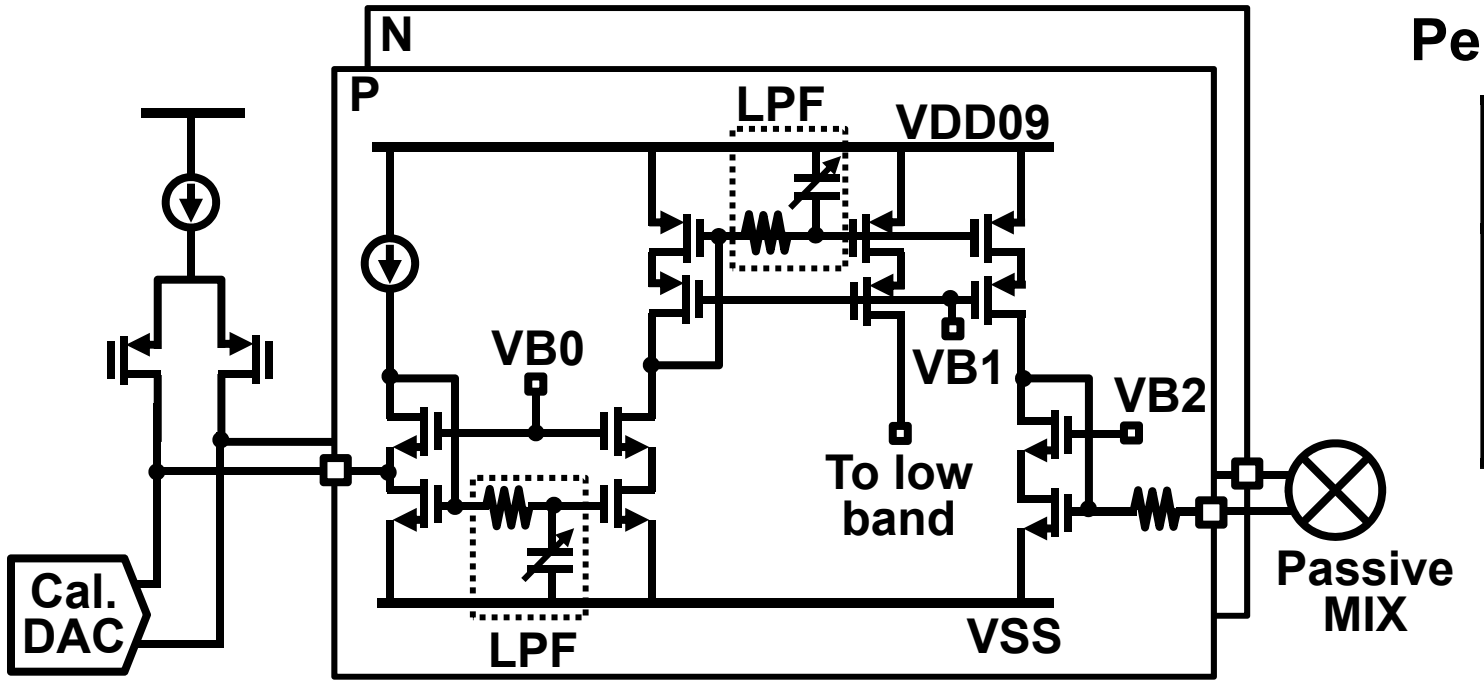


Outline

- Background
- Block diagram of proposed SoC
- Frequency-dependent IQ error calibration
- **Pure current mode TXBB**
- Isolated LO distribution circuit
- Interference analyzer
- Measurement results
- Conclusion

Proposed current mode TXBB

- OPAMP-less design contributes low noise operation SNR is improved to >50dB
- Poor CMRR can be compensated by carrier leak cal.



Current mode TXBB (Qch is not shown)

Performance comparison (simulation)

	Current mode	Voltage mode*
SNR [dB]	52.6	49.3
Suppression** [dB]	33	31.4
Area [um^2]	170	490

*Voltage mode circuit is based on [3] and simulated in a 28nm CMOS

**600MHz suppression

Outline

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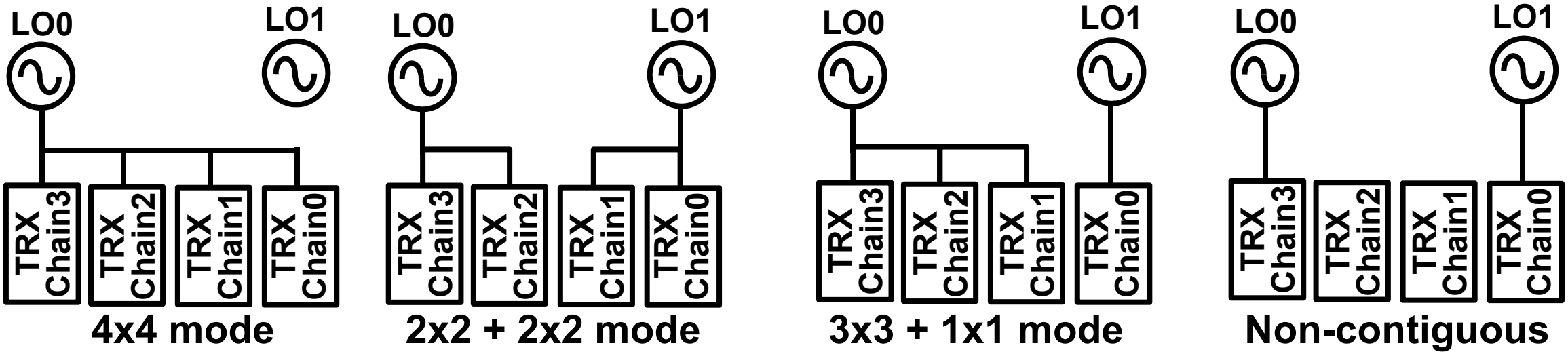
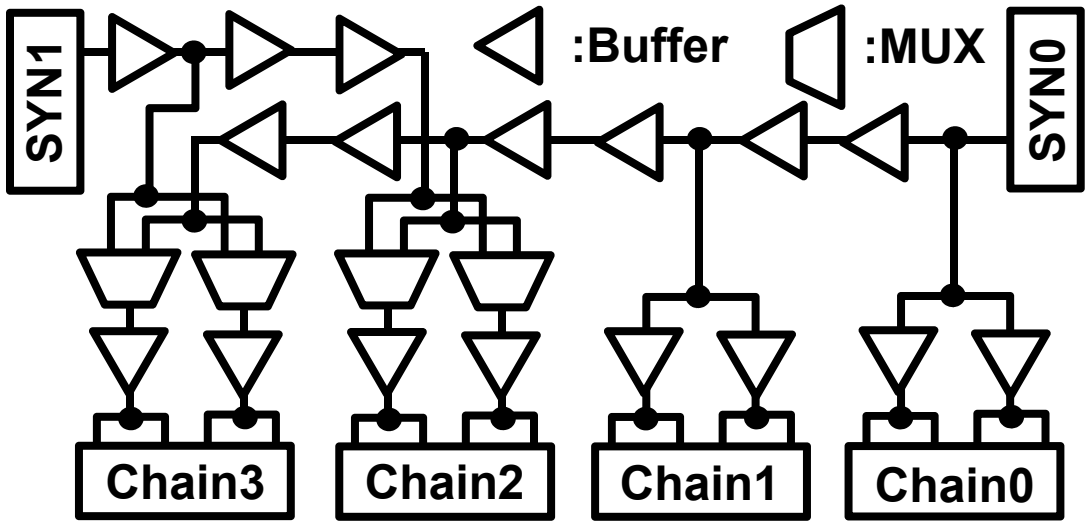
All possible operation modes

- 4x4 transceivers has 4 configuration
- Isolation of -50dB is necessary among each transmission line for EVM of less than -37dB

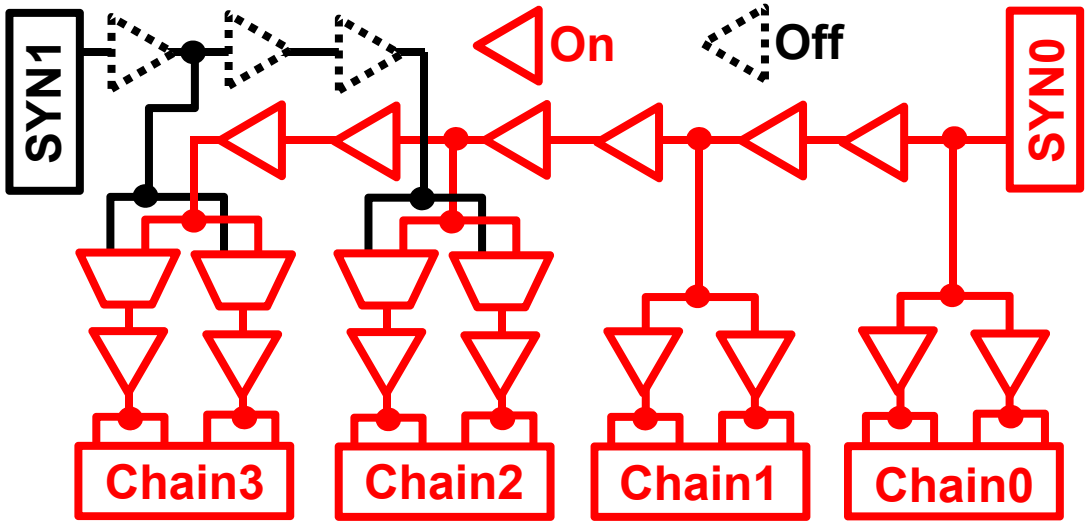


LO distribution schematics

- Proposed schematic supports all configurations
- 2 stages are turned off at each frequency boundary for better Isolation among transmission line



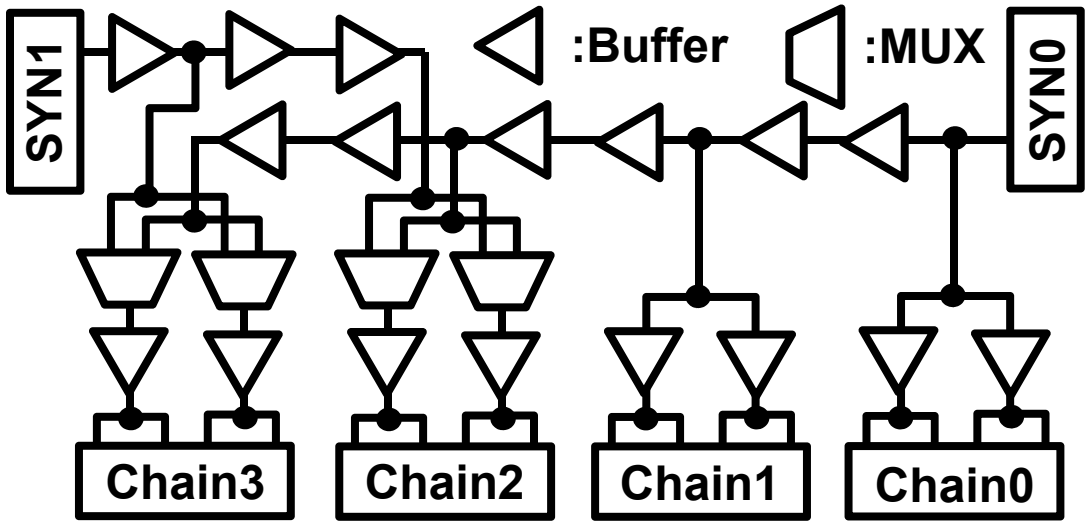
LO distribution schematics



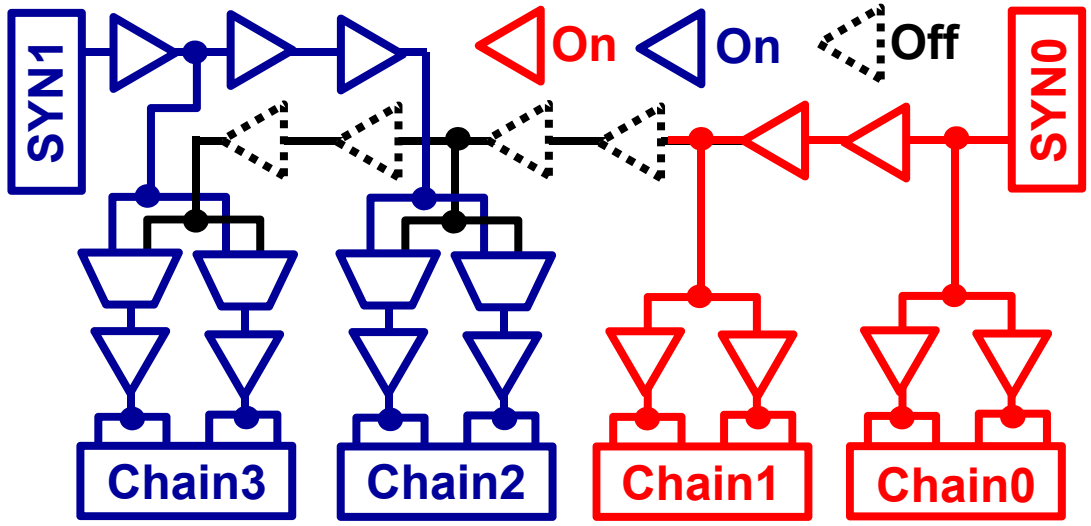
4x4 mode

LO distribution schematics

- Proposed schematics supports all configurations
- 2 stages are turned off at each frequency boundary for better Isolation among transmission line



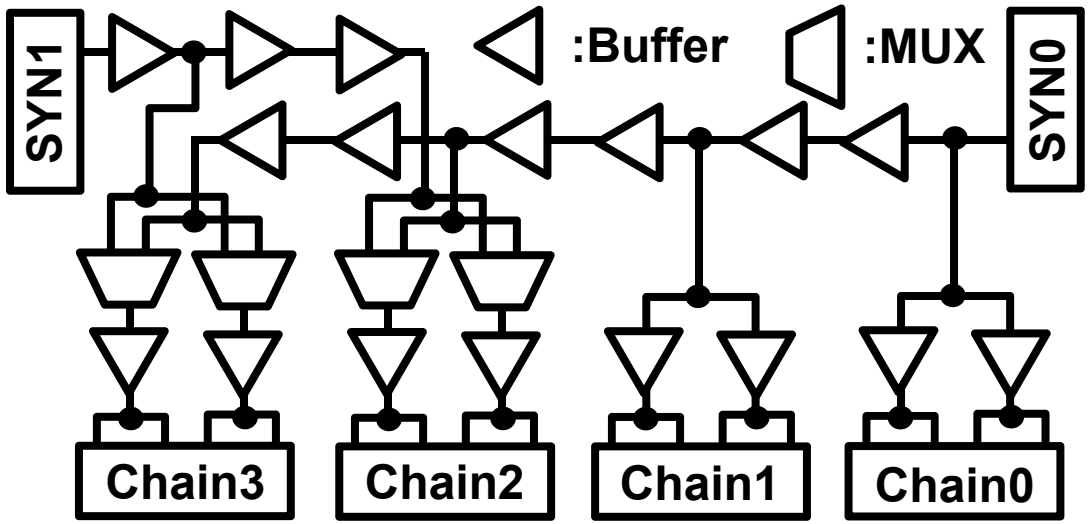
LO distribution schematics



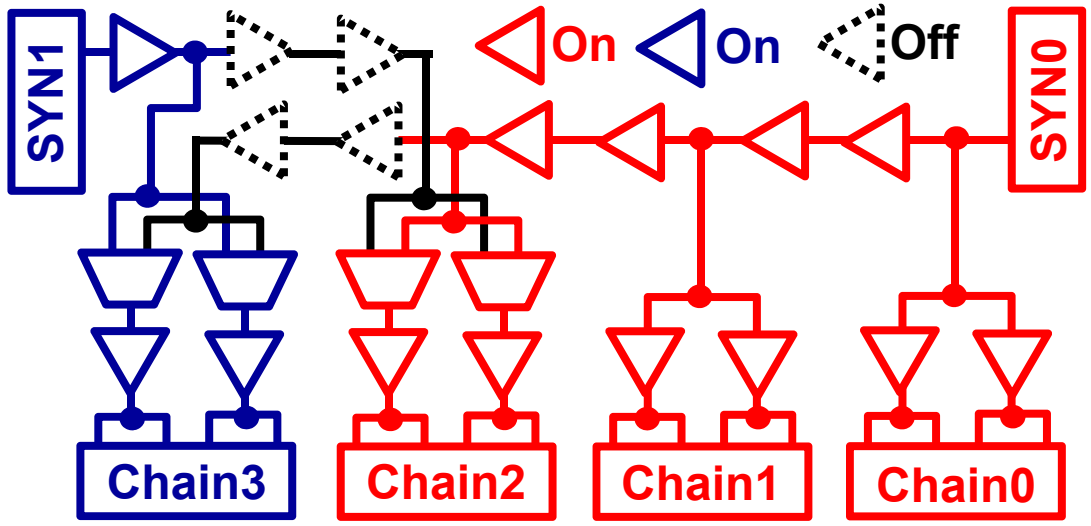
2x2 + 2x2 mode

LO distribution schematics

- Proposed schematics supports all configurations
- 2 stages are turned off at each frequency boundary for better Isolation among transmission line



LO distribution schematics



1x1 + 3x3 mode

Outline

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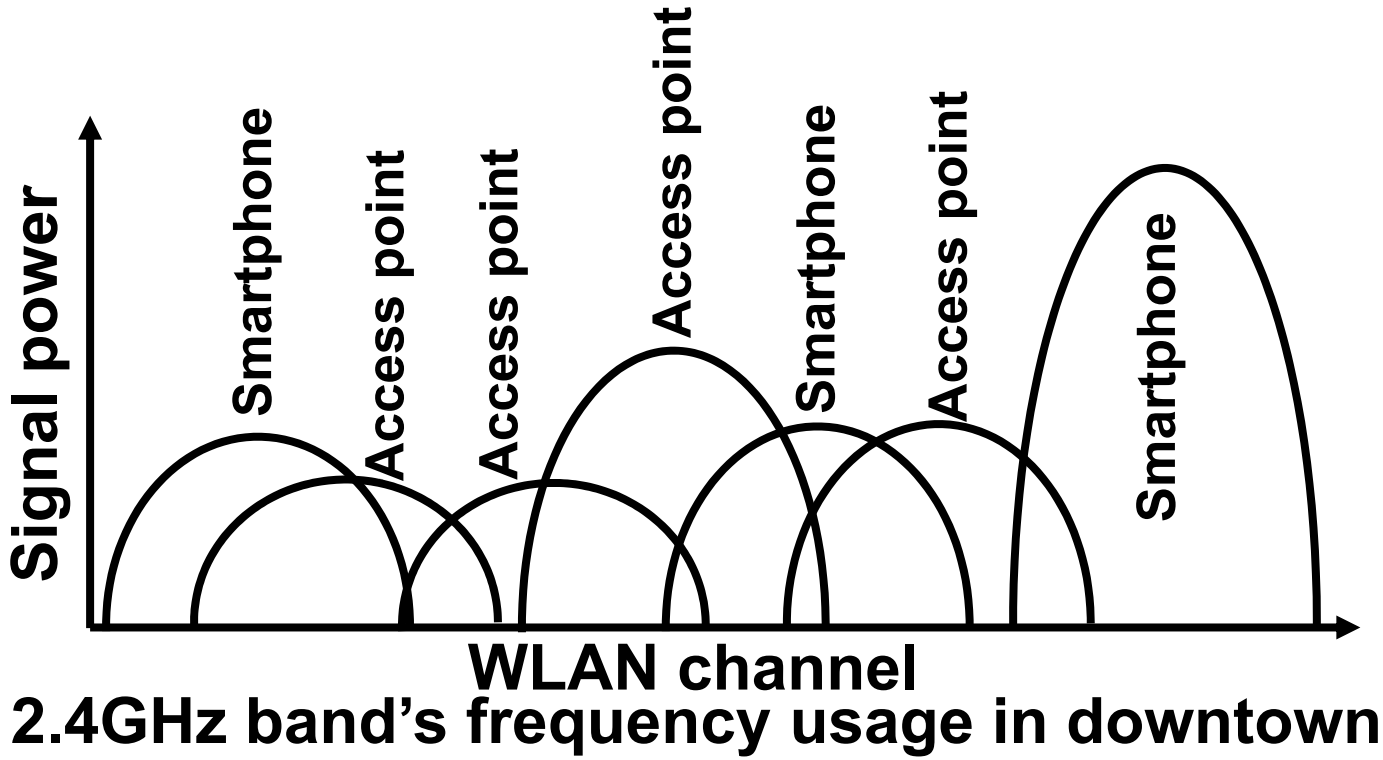
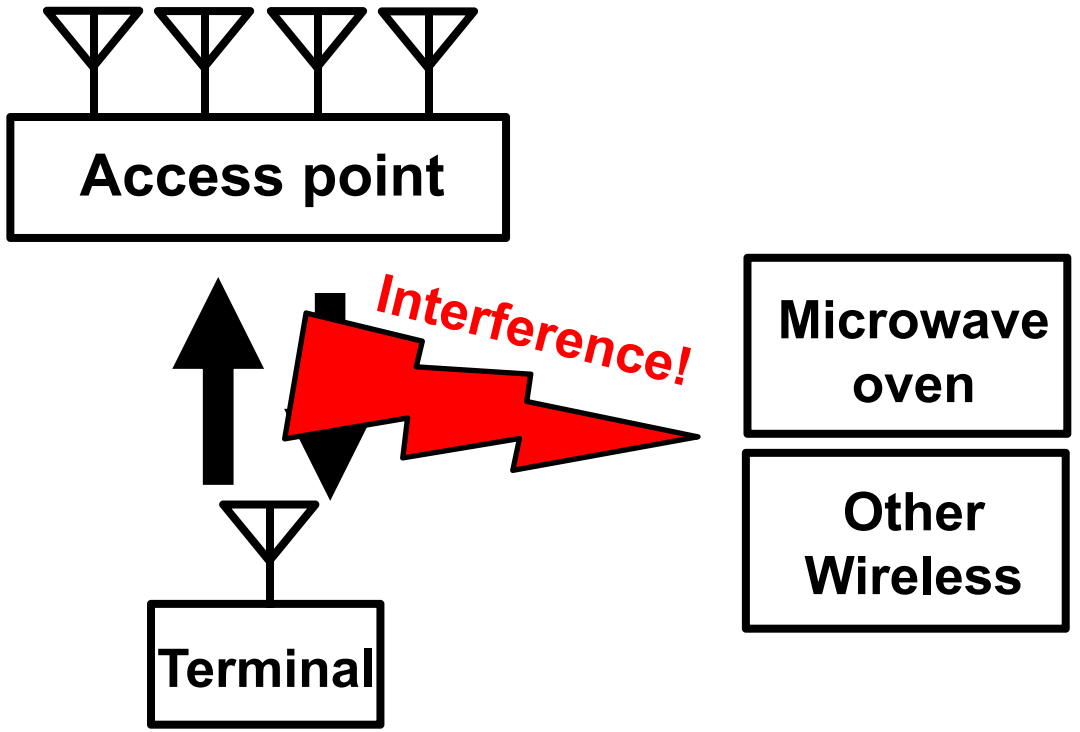
- **Interference analyzer**
- Measurement results
- Conclusion

Background of interference analyzer

- **Interference such as microwave oven and other wireless in the 2GHz/5GHz band limit WLAN channel and degrade throughput**

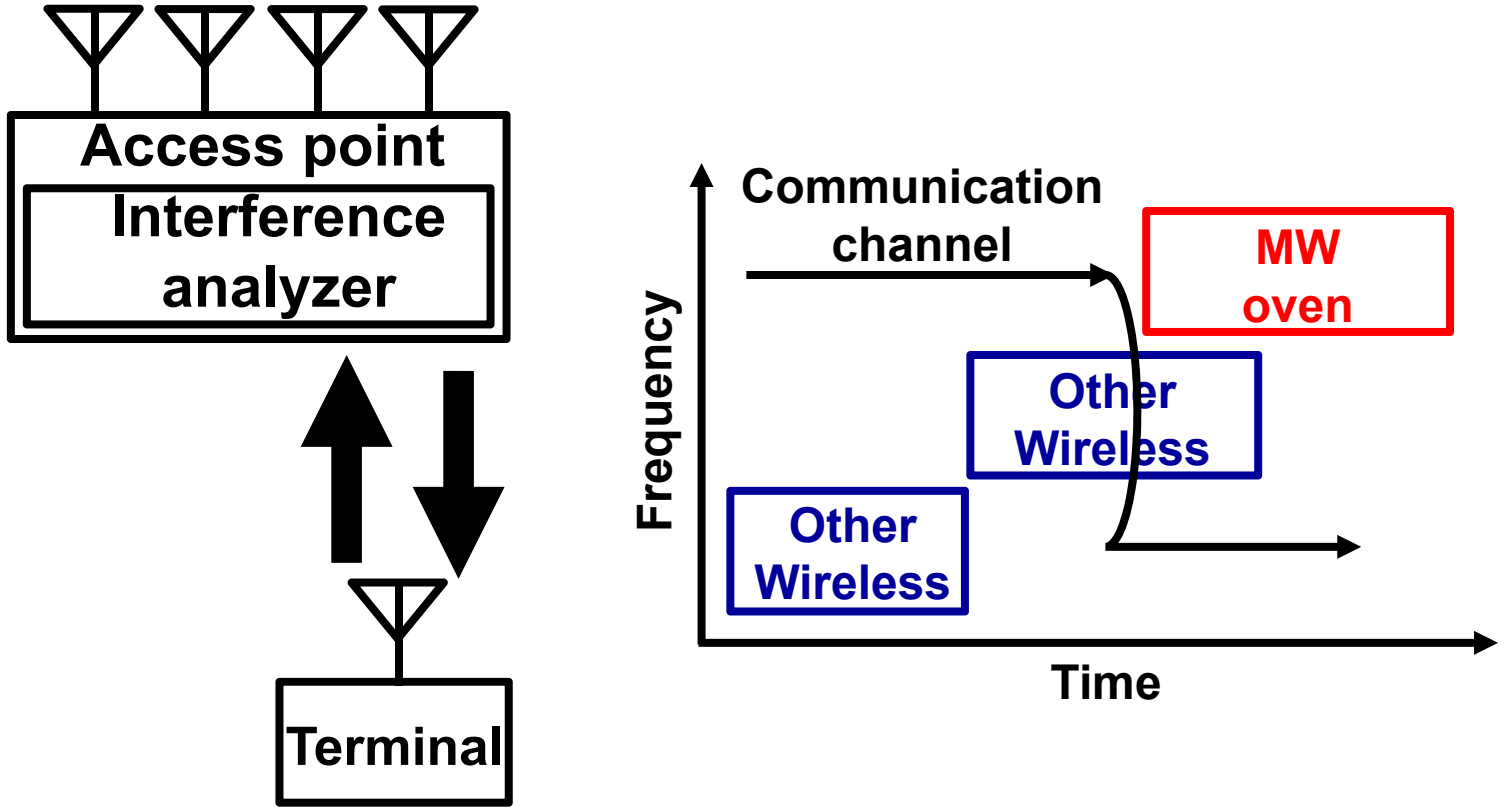


2.4GHz band's frequency usage in downtown



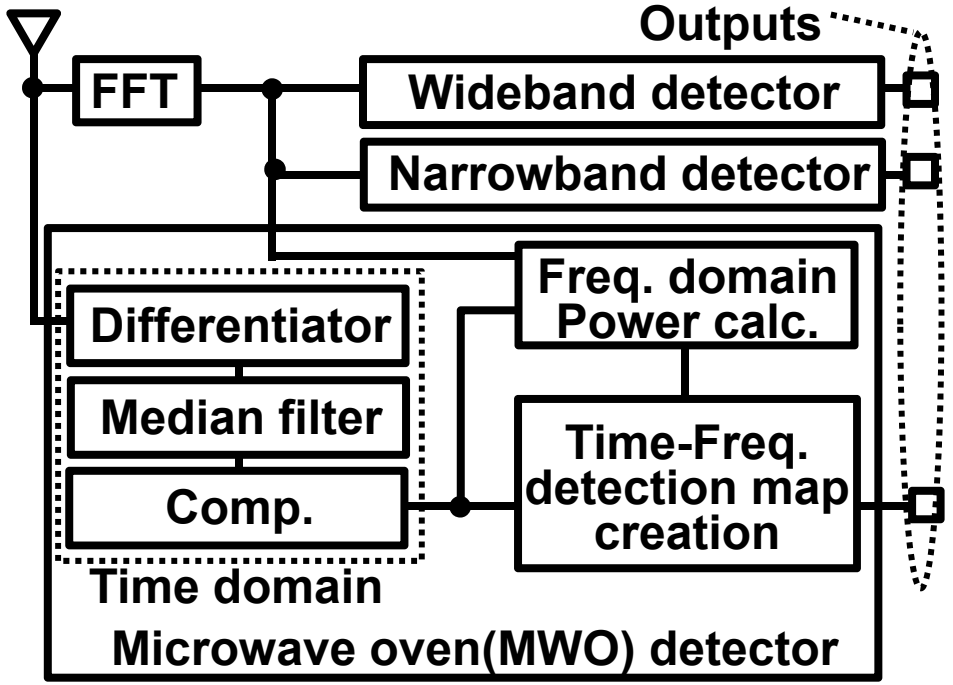
Concept of interference analyzer

- **Time-frequency-analysis-based identification enables optimum transmission strategy**



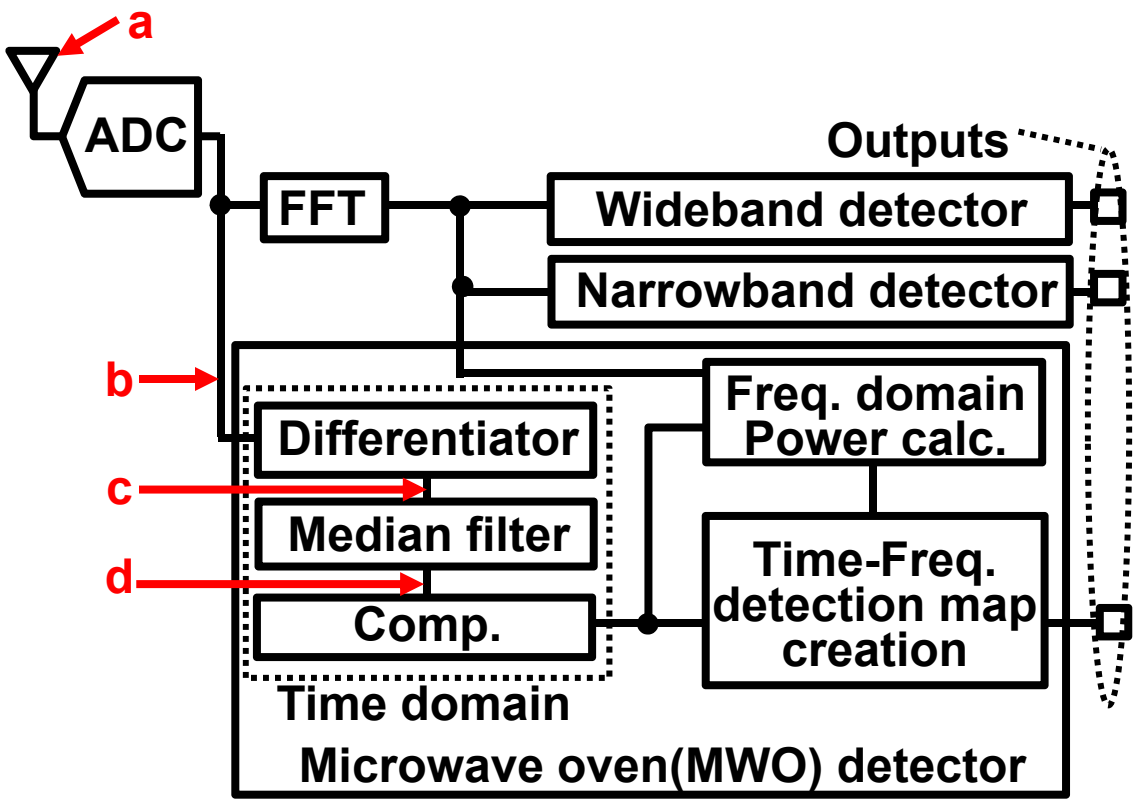
Proposed interference analyzer

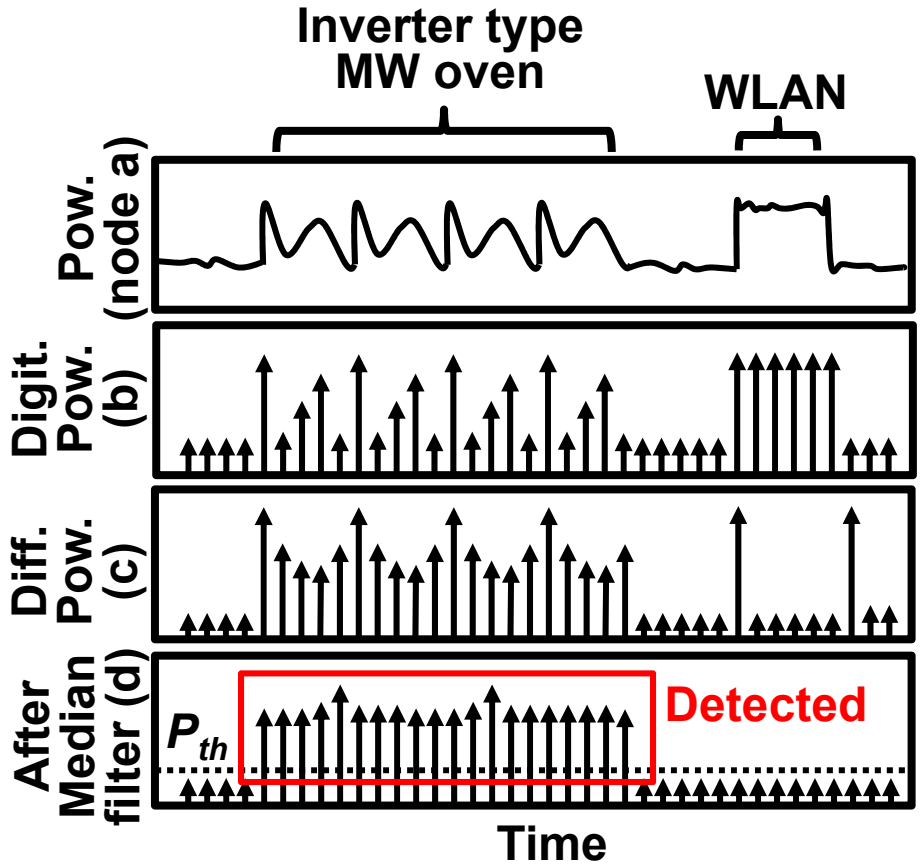
- Three parallel detector
  - Wideband detector: WLAN
  - Narrowband detector: BT, radar
  - Microwave oven detector: MW oven (including inverter type)



Time domain calculation

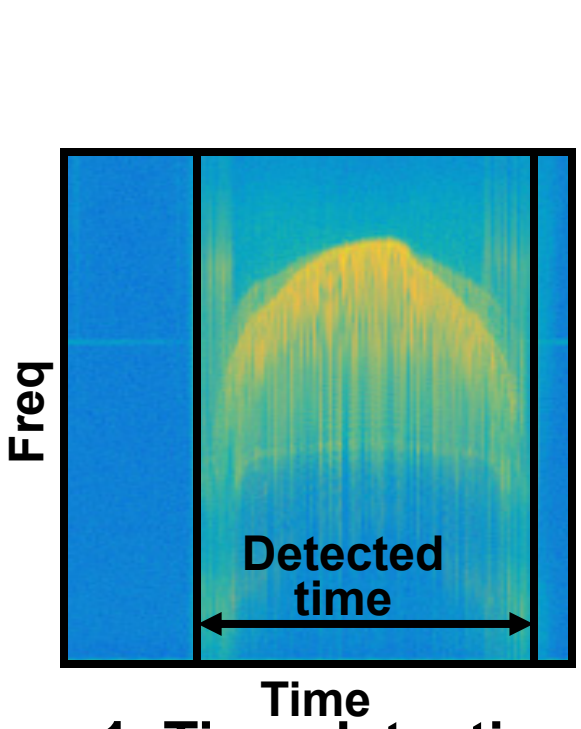
- **Differentiator and median filter detect the inverter type MW oven signal**





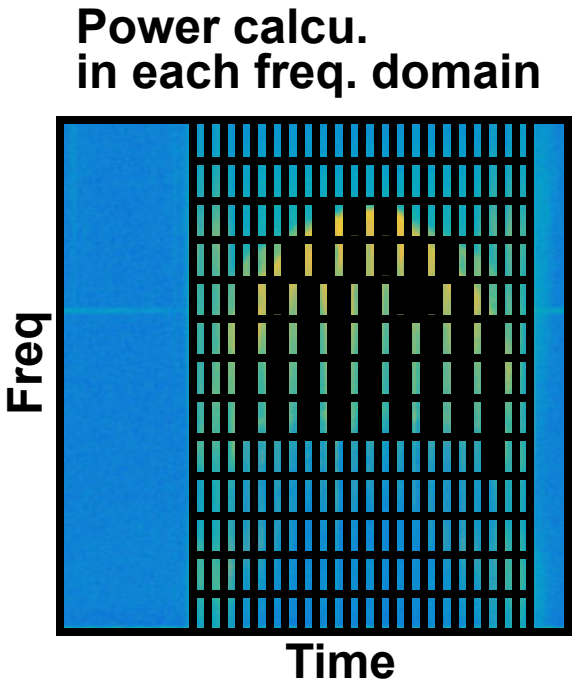
Frequency domain calculation

- **Frequency detection is done by detecting rapidly changed waveform**



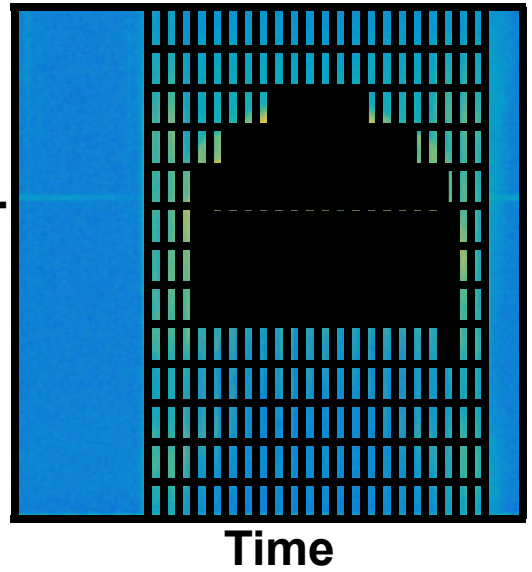
1. Time detection

Power calcu. in each freq. domain



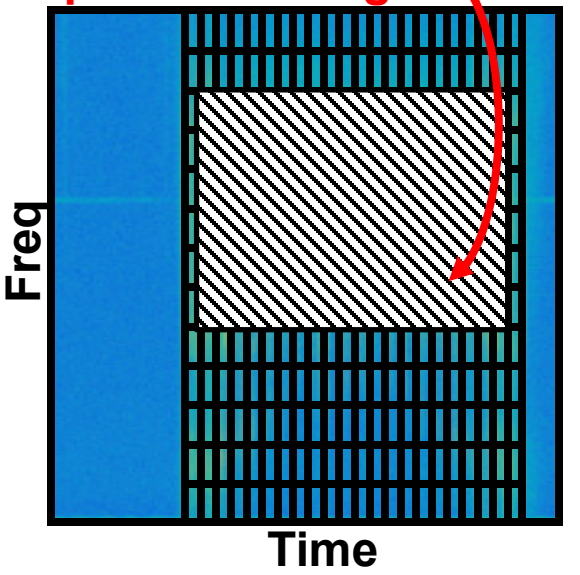
2. Power calc. in each cell

Diff. power calcu. in each freq. domain



3. Diff. power calc. in each cell

Detected area: Power and differentiated power are large



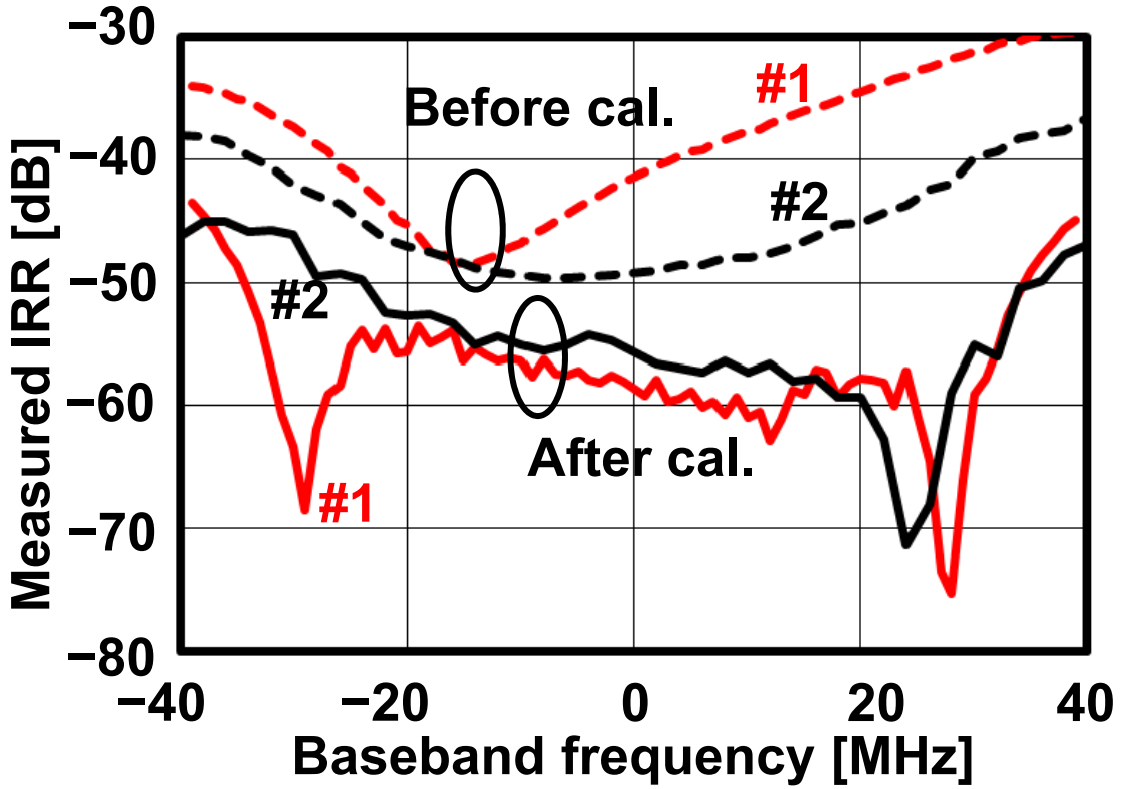
4. Time-freq. map creation

Outline

- Background
- Block diagram of proposed SoC
- Frequency-dependent IQ error calibration
- Pure current mode TXBB
- Isolated LO distribution circuit
- Interference analyzer
- **Measurement results**
- Conclusion

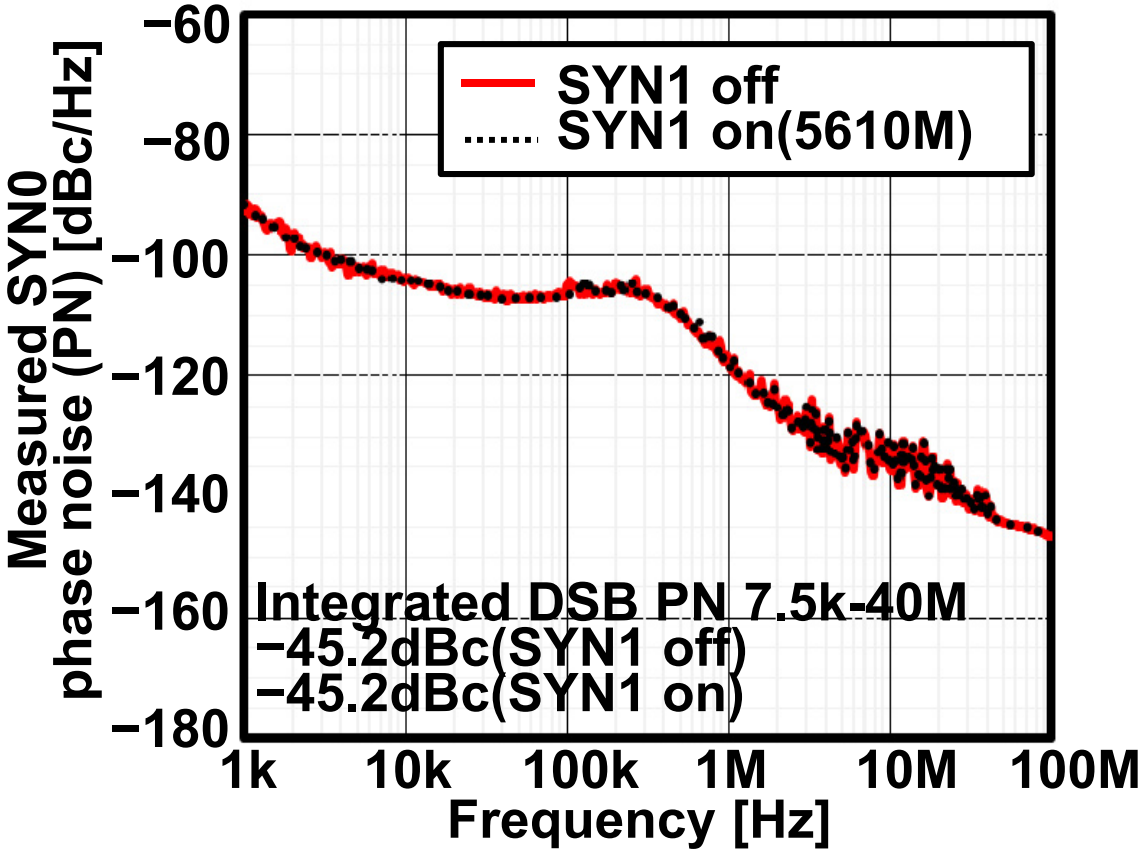
Measured RX image rejection ratio

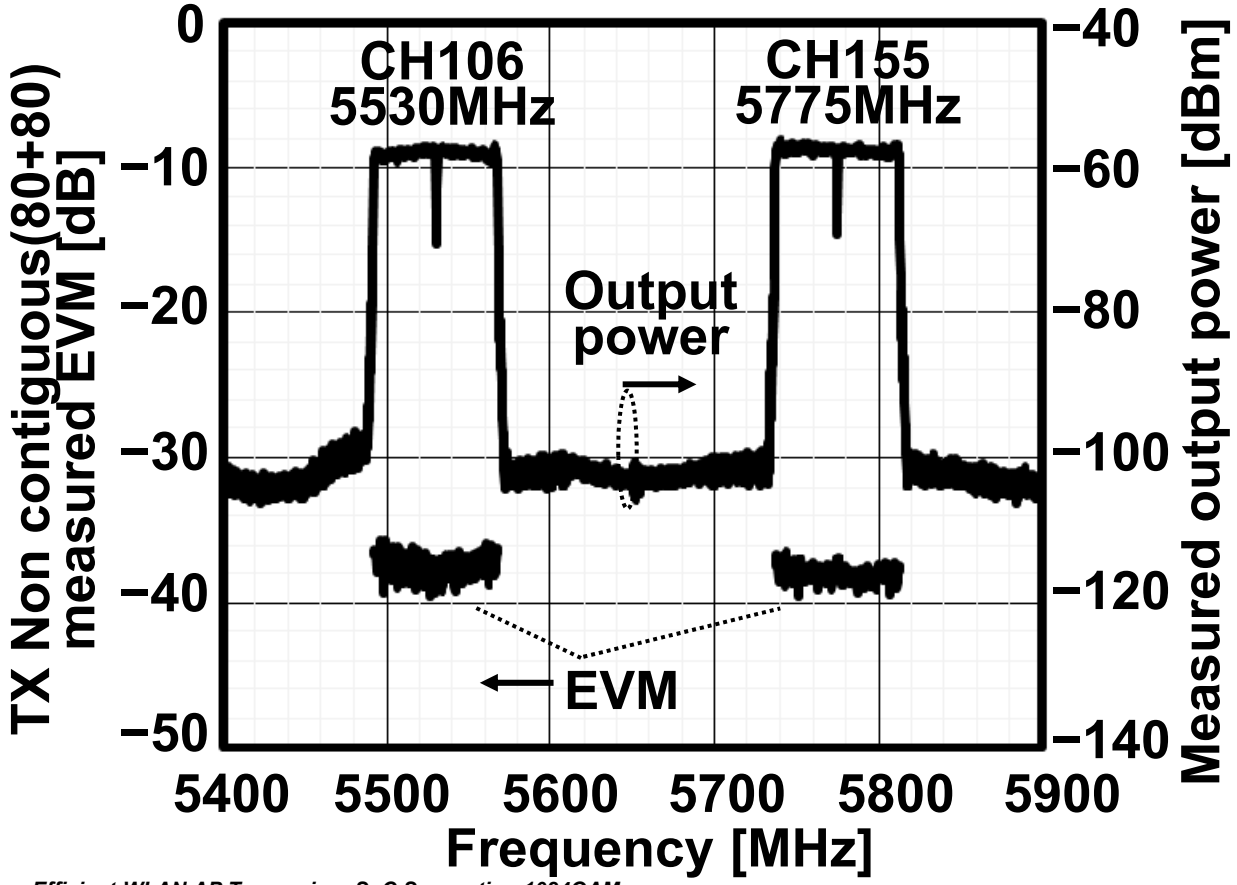
- Image rejection ratio is decreased after IQ calibration



Measured phase noise of SYN0

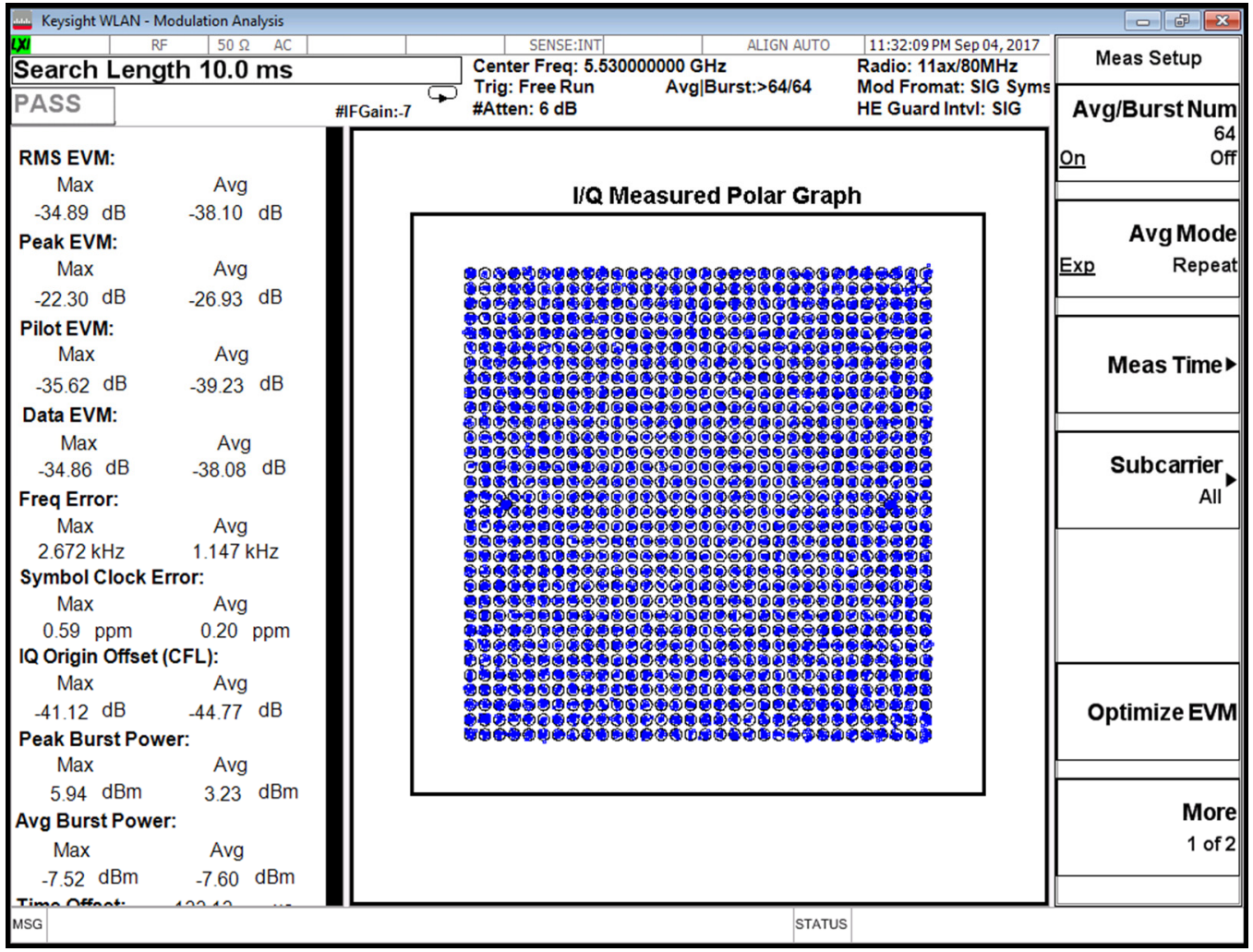
- **Phase noise is not degrade even if the other PLL is operated and non-contiguous spectrum are measured**





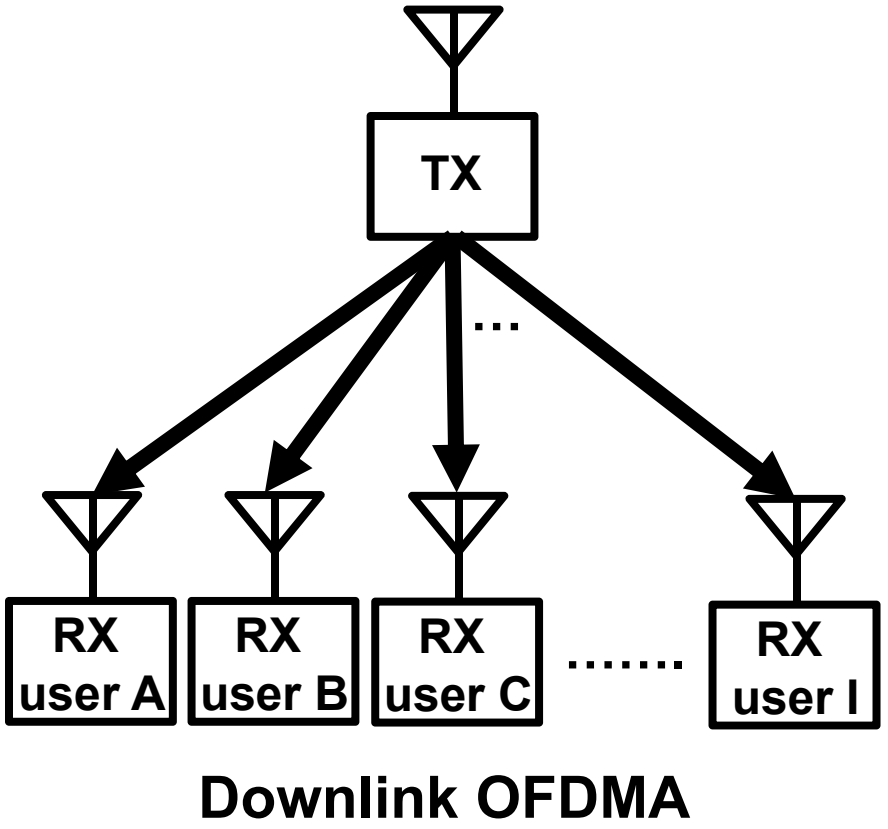
Measured TX 1K QAM constellation

- 1K QAM with EVM of -38.1dB is modulated

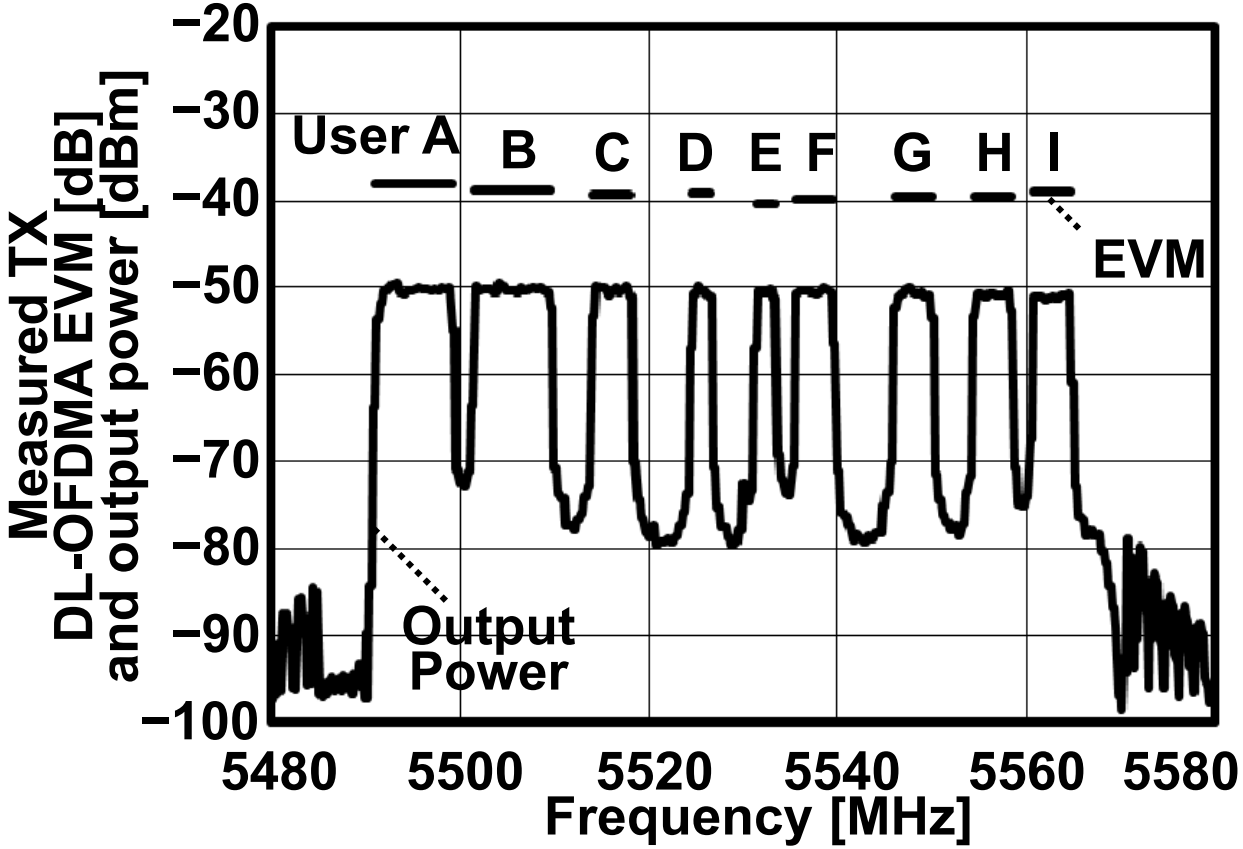


Measured TX Downlink-OFDMA

- **TX output spectrum are successfully measured. EVM is less than -37.99dB**

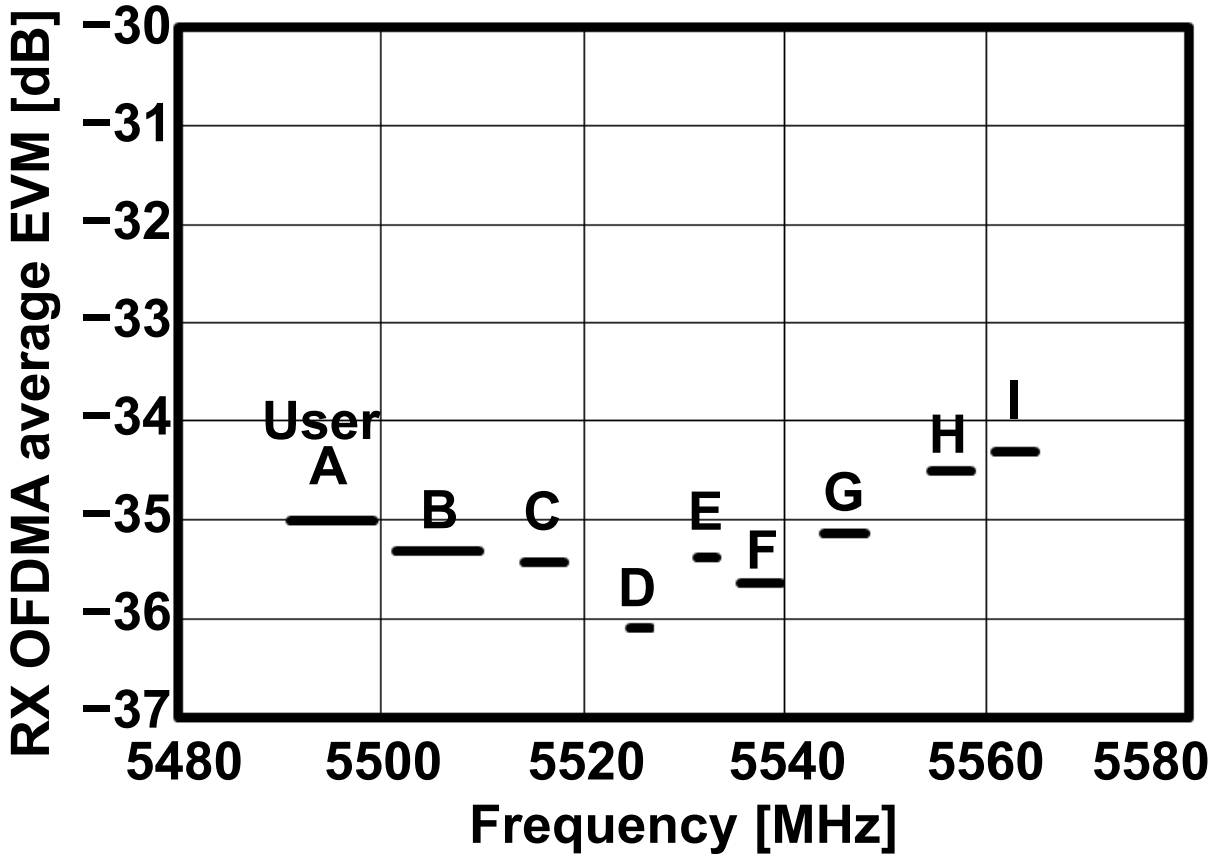


Downlink OFDMA



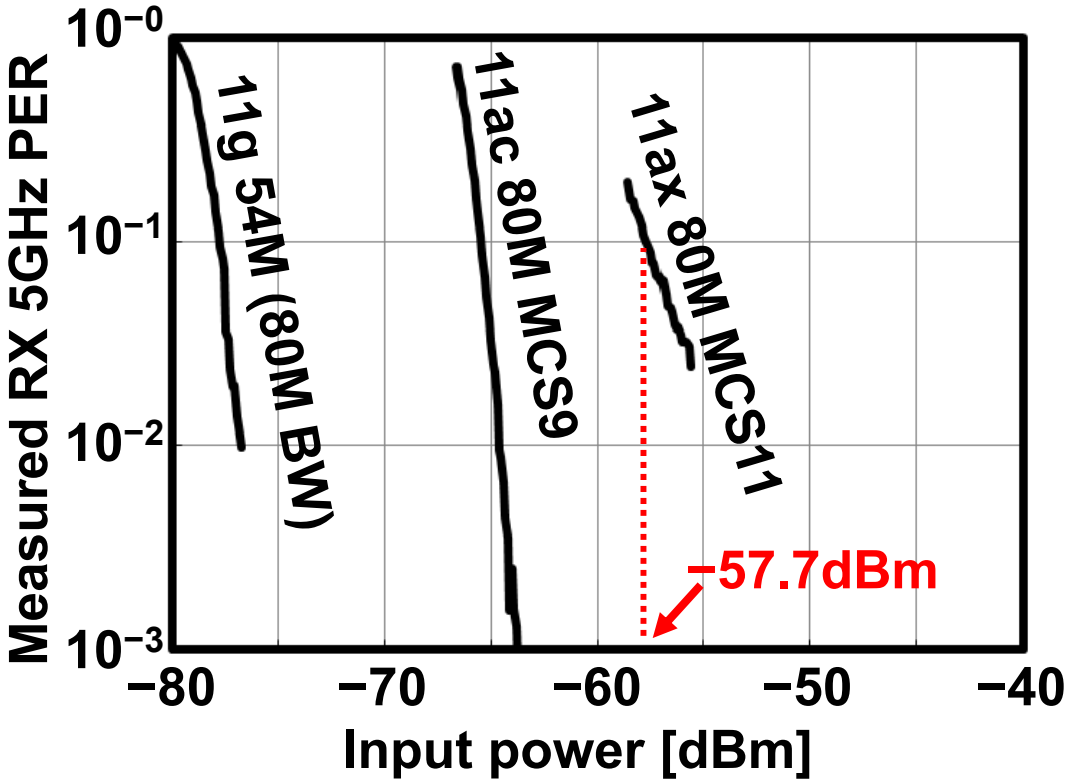
Measured RX-OFDMA EVM

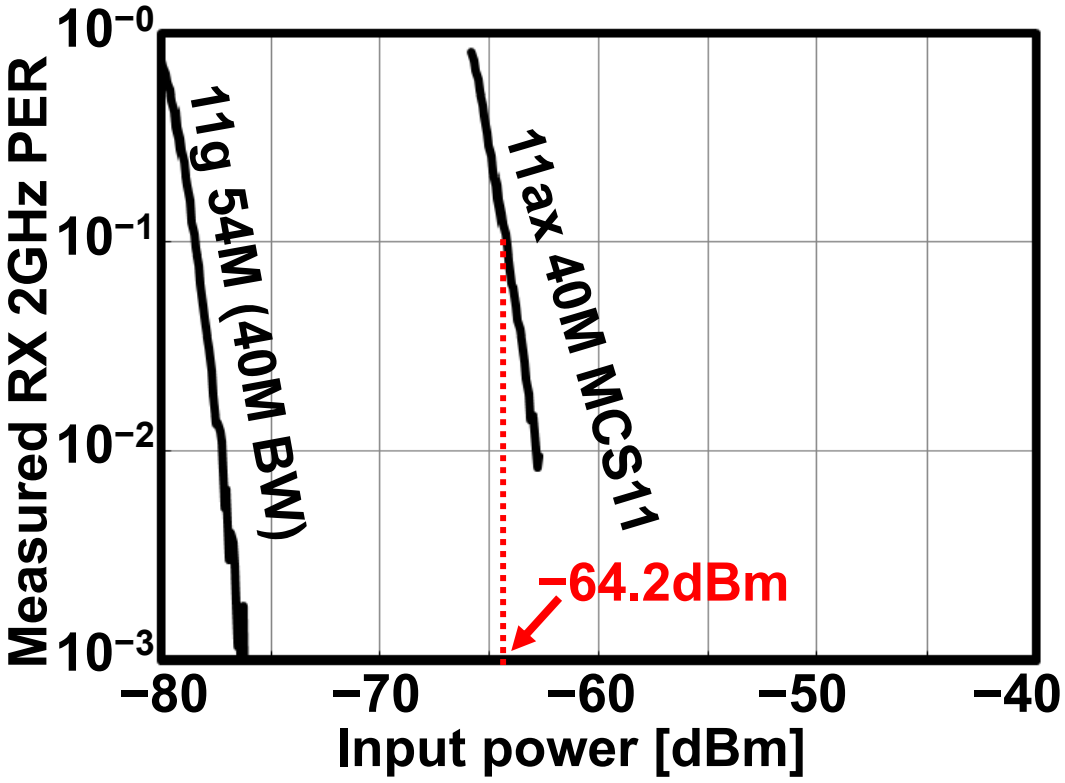
- **EVM of less than -34.3dB are measured**



Measured sensitivity

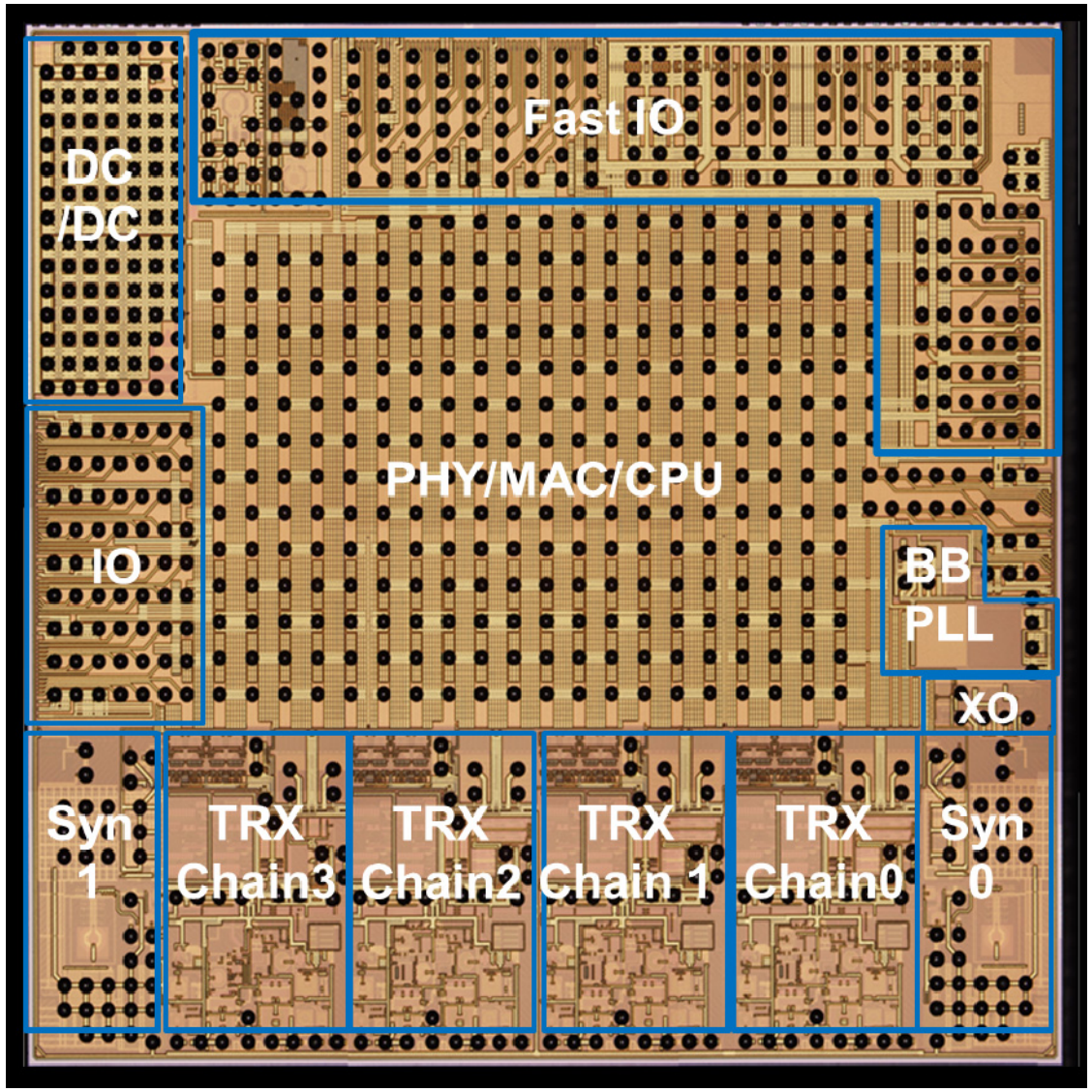
- 11ax signal is successfully measured with sensitivity of -57.7dBm (5GHz band), -64.2dBm(2.4GHz band)





Chip micrograph

- 28nm CMOS process
- Chip size is 44.6mm^2



Performance comparison

		This work	ISSCC2017[1]	JSSC2017[4]	ISSCC2014[5]
WLAN standards		4x4 11abgn/ac/ax	4x4 11abgn/ac	2x2 11abgn/ac	3x3 11abgn/ac
Process [nm]		28	40	40	40
TX EVM [dB]	2.4G	-42.1(n,64QAM,-5dBm) −42.5(ax,40M,1KQAM,-5dBm)	NA	−40 (20M, Floor)	−41 (HT40, −5dBm)
	5G	-38.4(ac,80M,256QAM,-5dBm) −38.1(ax,80M,1KQAM,-5dBm)	−36.5 (ac,80M,MCS9,Floor)	−38 (20M,Floor)	−37 (−5dBm)
RX sensitivity [dBm]	2.4G	-78.4(g,54M) −64.2(ax,40M,1KQAM)	−77(LG,54M)	−78.3(54Mbps)	NA
	5G	-65.4(ac,80M,256QAM) −57.7(ax,80M,1KQAM)	−62(ac,80M, MCS9)	−66(MCS9)	NA
Image rejection ratio after cal. [dB]		−53(RX, Ave. over 80M) −58(RX, at 5MHz) −61(TX, Ave. over 80M) −64(TX, at 5MHz)	−61(TX,at 5MHz)	NA	NA

Outline

- Background
- Block diagram of proposed SoC
- Frequency-dependent IQ error calibration
- Pure current mode TXBB
- Isolated LO distribution circuit
- Interference analyzer
- Measurement results
- **Conclusion**

Conclusion

- 11ax compliant AP transceiver SoC is proposed
- Frequency dependent IQ amplitude calibration compensate the IRR less than -50dB
- Current-mode TXBB improves the SNR > 50dB
- Isolated LO distribution circuit are presented for better isolation larger than 50dB
- Interference analyzer detects MW oven signal

An ADPLL-Centric Bluetooth Low-Energy Transceiver with 2.3mW Interference-Tolerant Hybrid-Loop Receiver and 2.9mW Single-Point Polar Transmitter in 65nm CMOS

Hanli Liu, Zheng Sun, Dexian Tang, Hongye Huang, Wei Deng, Rui Wu, Kenichi Okada, and Akira Matsuzawa

Tokyo Institute of Technology, Japan

Outlines

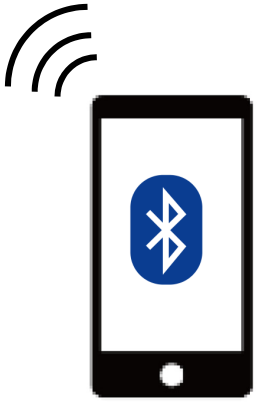
- Introduction and Prior Art
- Proposed BLE TRX
- Measurement Results
- Comparison & Conclusion

Outlines

- **Introduction and Prior Art**
- **Proposed BLE TRX**
- **Measurement Results**
- **Comparison & Conclusion**

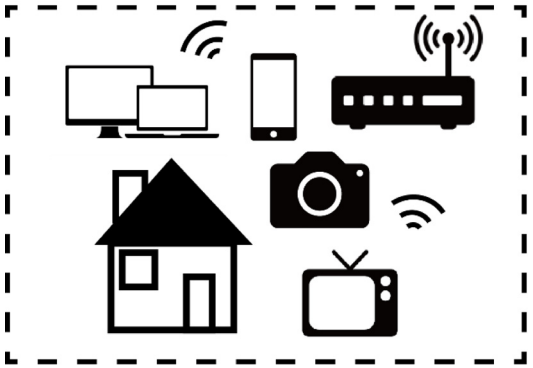
Introduction

Smart Infrastructure

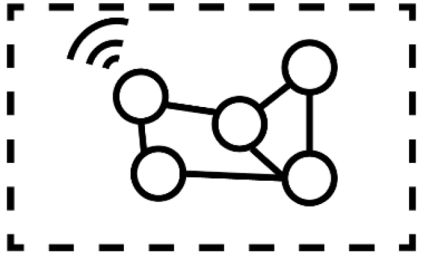


Bluetooth Low-Energy(BLE):

- **Low power operation**
  - More than 10yr battery life
- **Good sensitivity**
  - Less than -90dBm
- **Strong anti-interference**



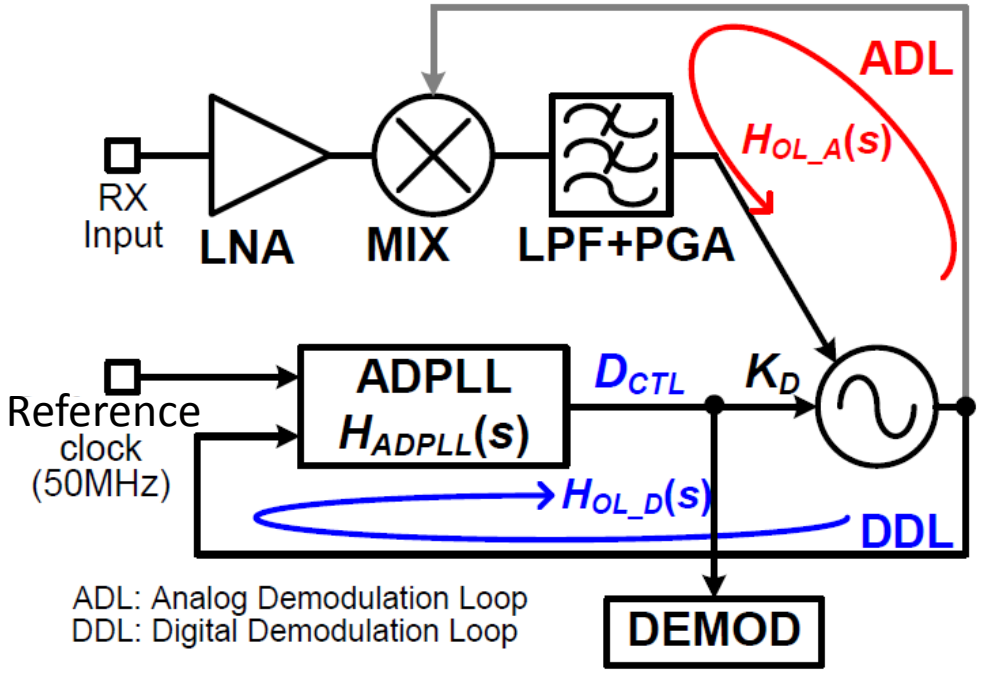
Smart House

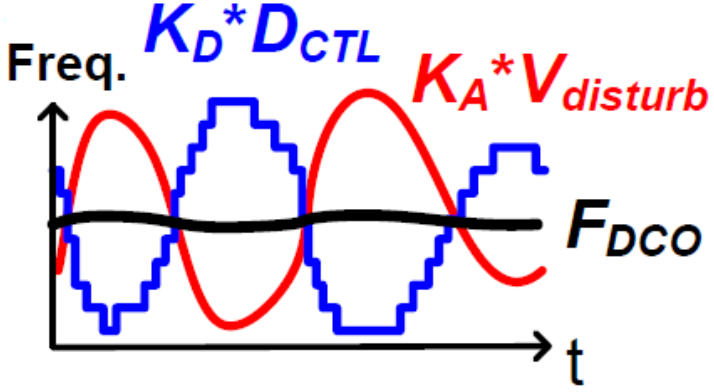


oT

Massive Sensor Network

Prior Art: Hybrid-loop RX





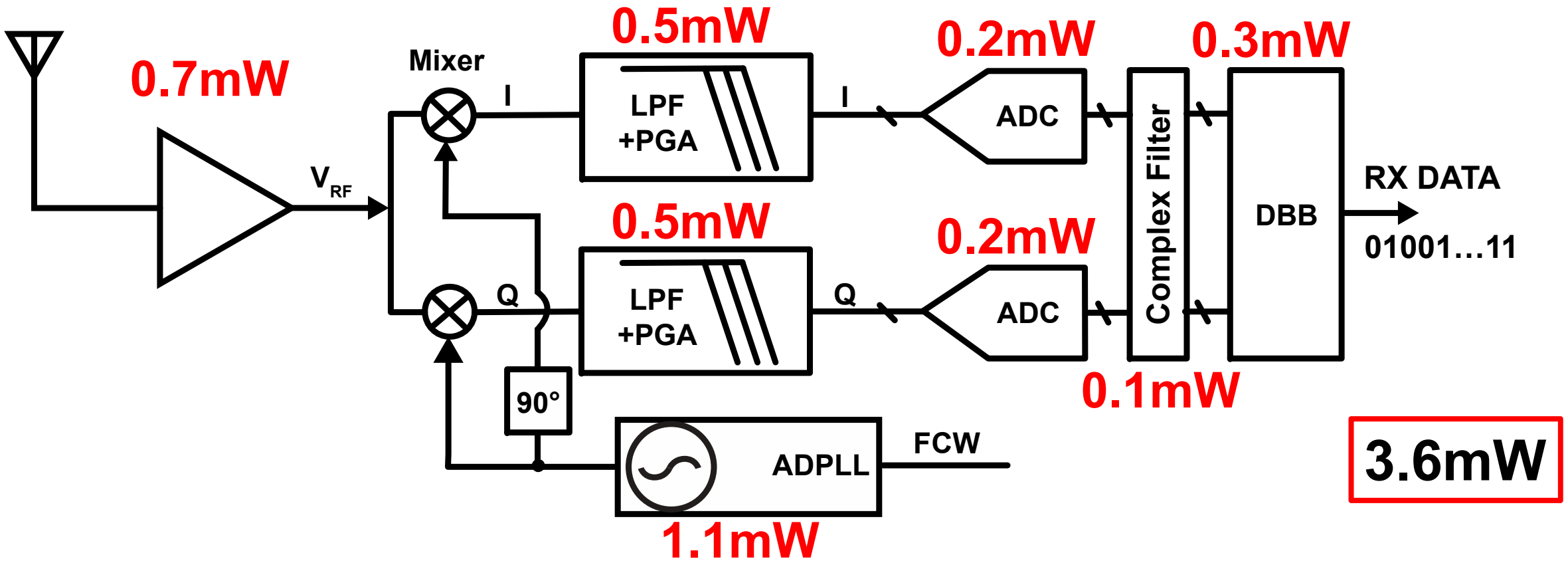
[H. Okuni, ISSCC 2016]

- ☺ Good energy efficiency of demodulation(dual loop digitization)
- ☺ Good in-band and out-band blocker tolerance
- ☹ Limited dynamic range of digitization loop
- ☹ Suffer from unknown carrier phase
- ☹ Large ADPLL power consumption

Outlines

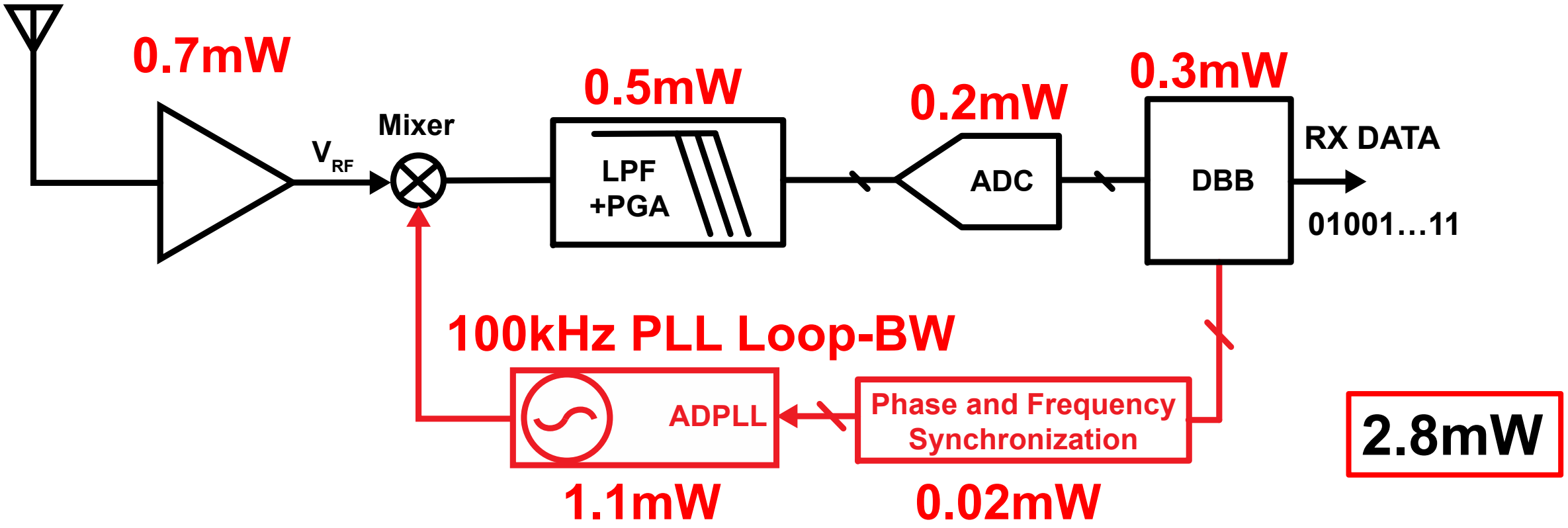
- Introduction and Prior Art
- **Proposed BLE TRX**
- Measurement Results
- Comparison & Conclusion

Conventional I/Q RX



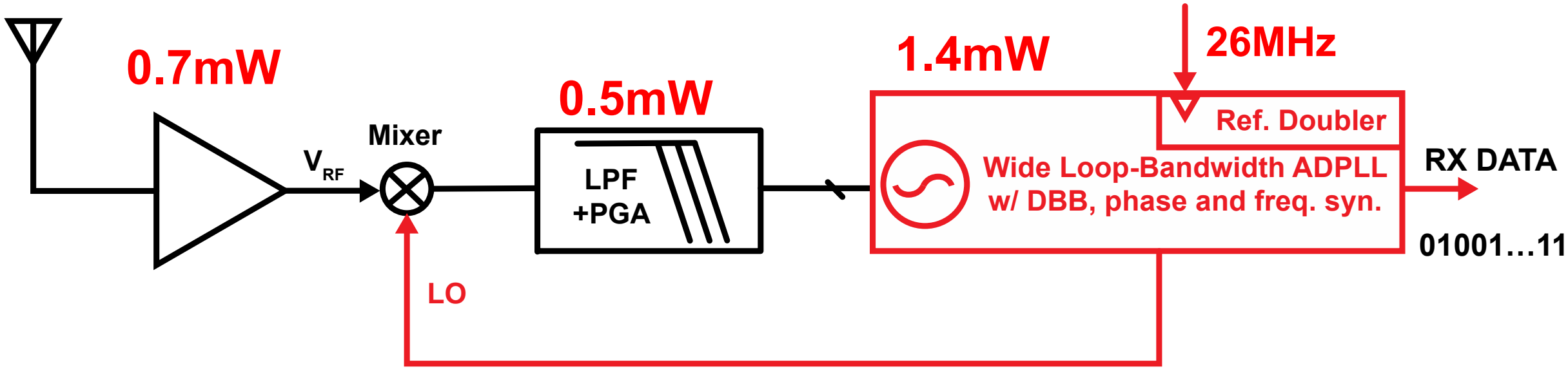
Two down-conversion paths, LPFs, PGAs, and ADCs(1.4mW)

Single-Path RX



- **Narrow loop-bandwidth** of ADPLL limits the convergence speed
- Still require **an ADC** with good dynamic range

Proposed Hybrid-loop BLE RX

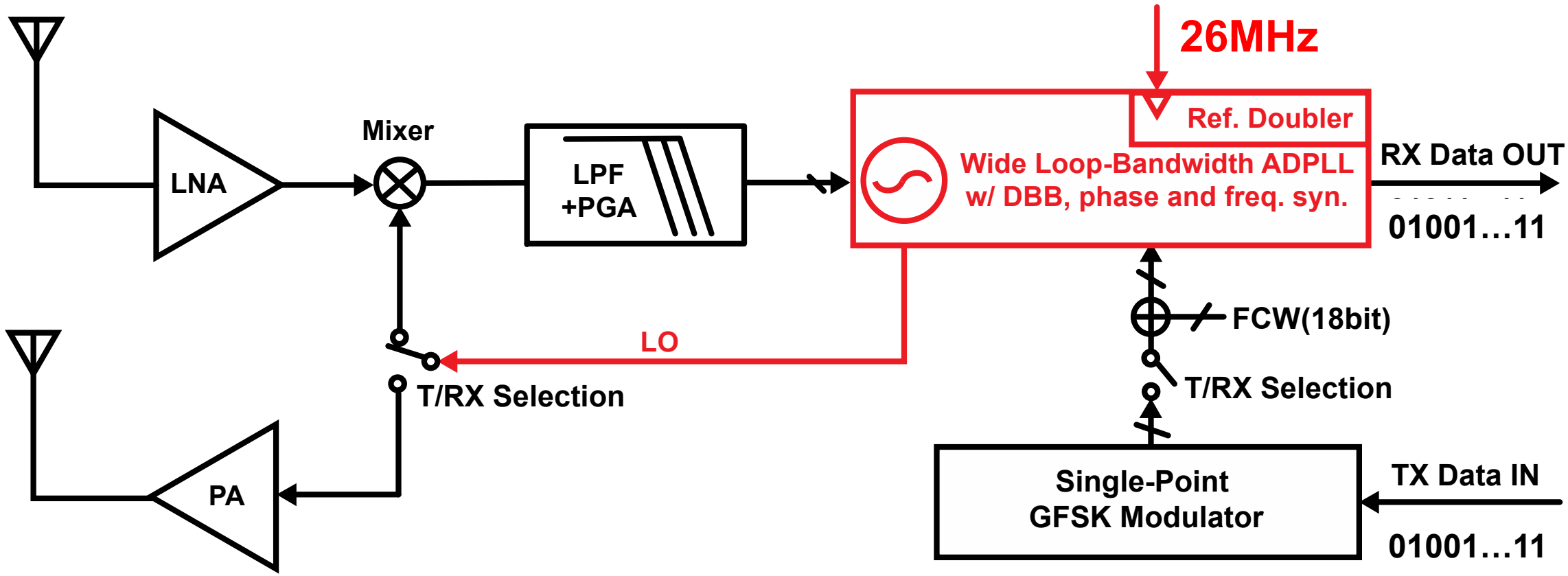


- Greatly reduced RX power consumption (1mW)

2.6mW

- Enhance ADPLL loop-bandwidth using reference doubler
- Enhanced loop convergence time
- Enhanced dynamic range when using ADPLL as ADC

Proposed BLE TRX

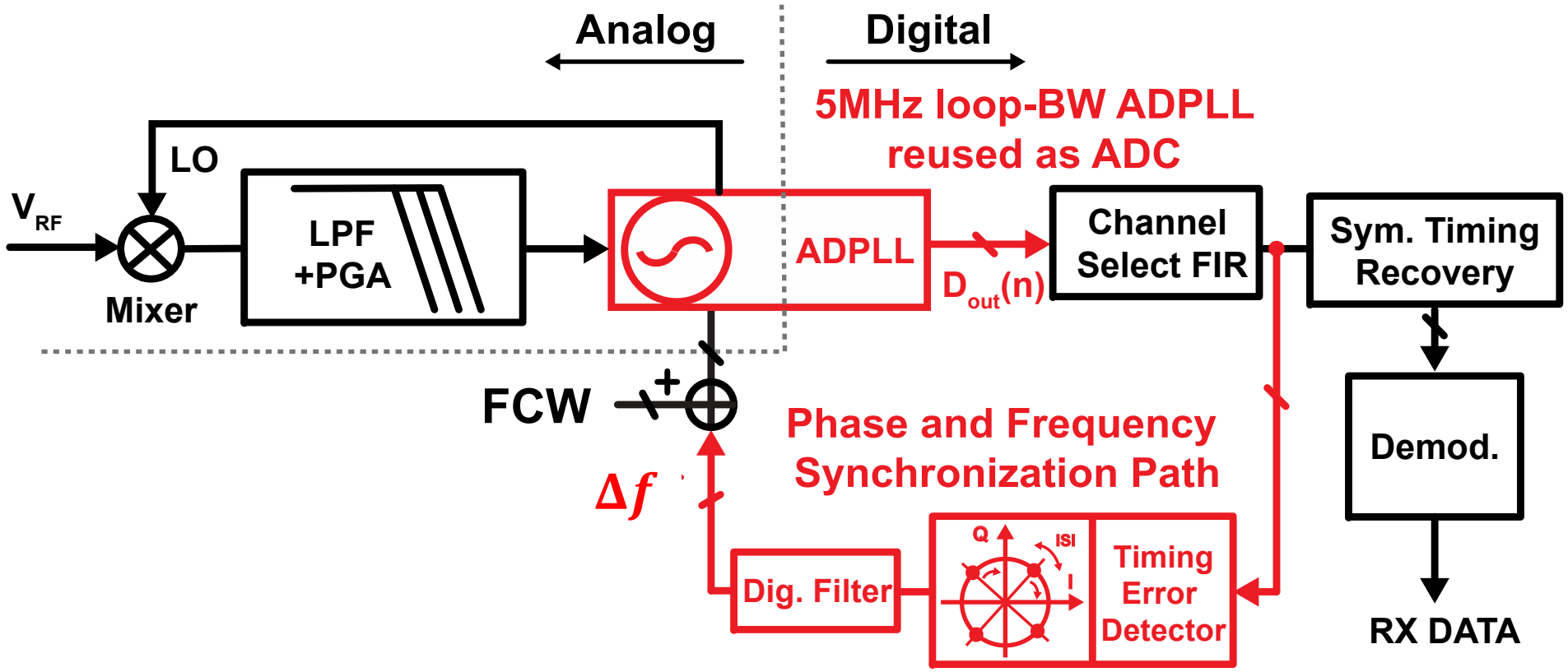


- Reused wide loop-bandwidth ADPLL for TX
- Improved TX EVM performance by single-point modulation

Challenges of Proposed TRX

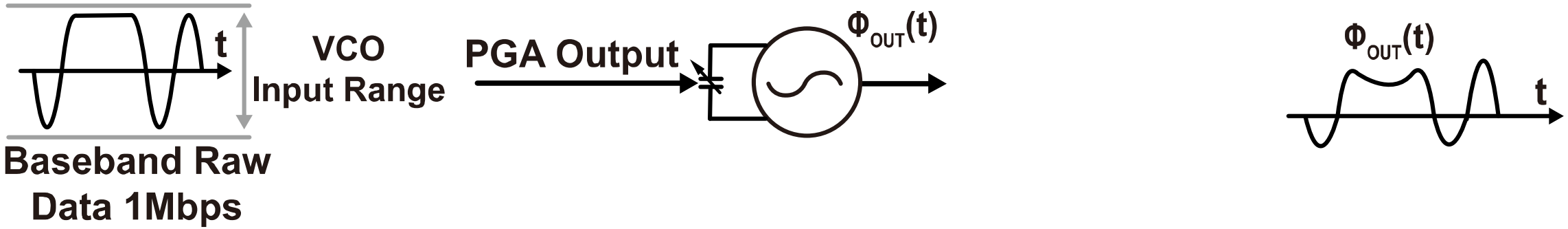
- **Hybrid loop RX**
  - **Phase-and-frequency tracking to synchronize LO phase and incoming carrier phase**
  - **High dynamic range when using ADPLL as ADC**
  - **Wide loop-bandwidth ADPLL with low power operation**
- **Single-point modulation TX**
  - **Wide loop-bandwidth ADPLL with low power operation**
- **ADPLL**
  - **Wide loop-bandwidth (>4MHz)**
  - **Good in-band phase noise (<-100dBc/Hz)**
  - **Good fractional spurs (<-40dBc)**
  - **Low power operation (about 1mW)**

ADPLL with LO Synchronization



- ☺ Halving RX blocks in baseband
- ☺ No ADCs(LDOs, bias circuits and clock buffers)
- ☺ Enhanced convergence time(<8us)

Reuse ADPLL as ADC

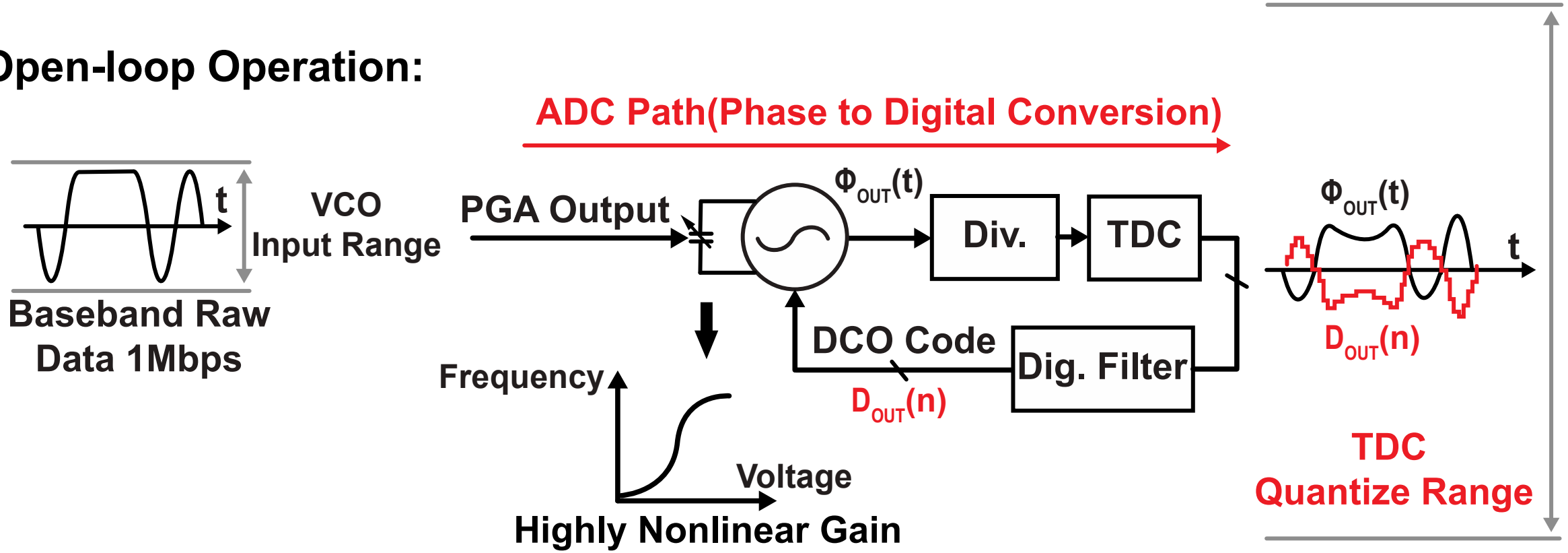


- **PGA/LPF output inputs into varactor, and varies frequency**

[H. Okuni, ISSCC 2016]

Reuse ADPLL as ADC

Open-loop Operation:



- ☹ Limited dynamic range by varactor linearity
- ☹ Waste of TDC range and resolution
- ☹ High power ADPLL with poor phase noise and spurs

SNDR of ADPLL-based ADC

Large Input → SNDR → ACR/Blocker etc.

- Varactor Linearity
- TDC Linearity

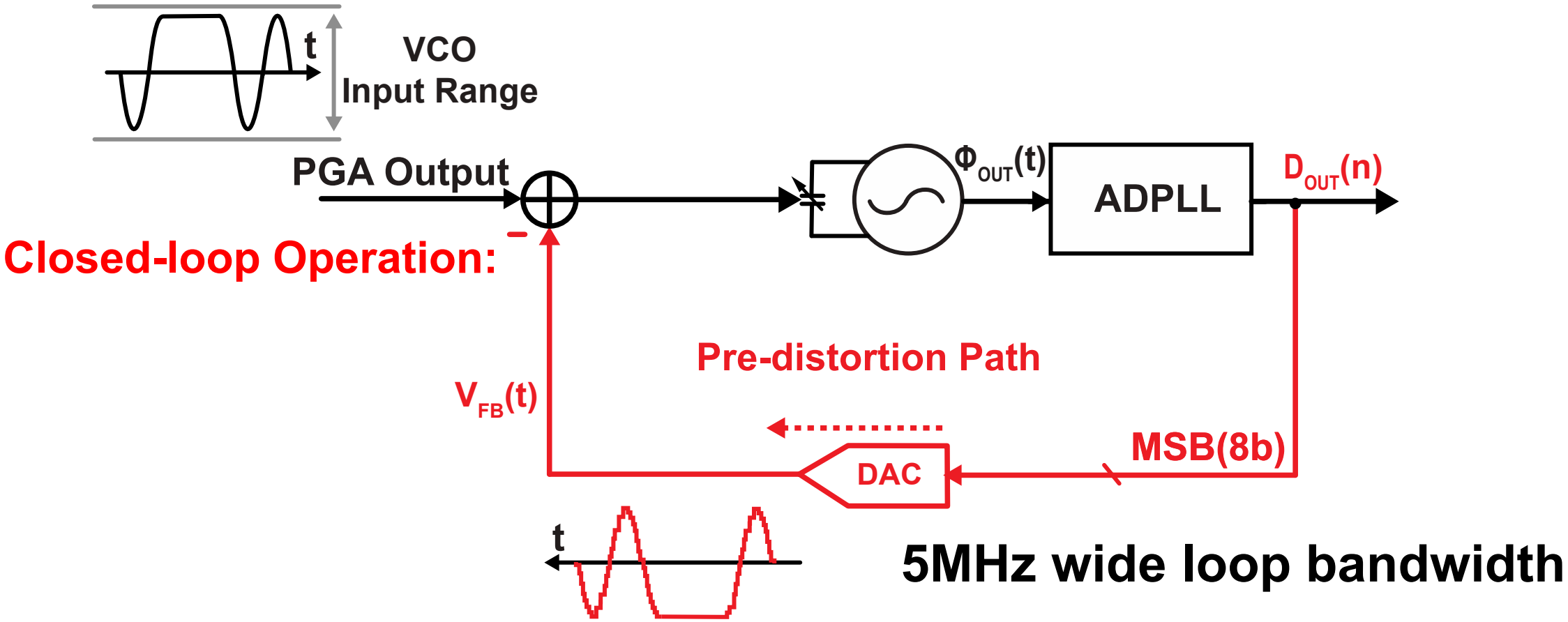
Small Input → SNR → Sensitivity etc.

- Varactor Gain
- TDC Resolution

☹ Larger varactor gain causes much poor linearity(poor SNDR)

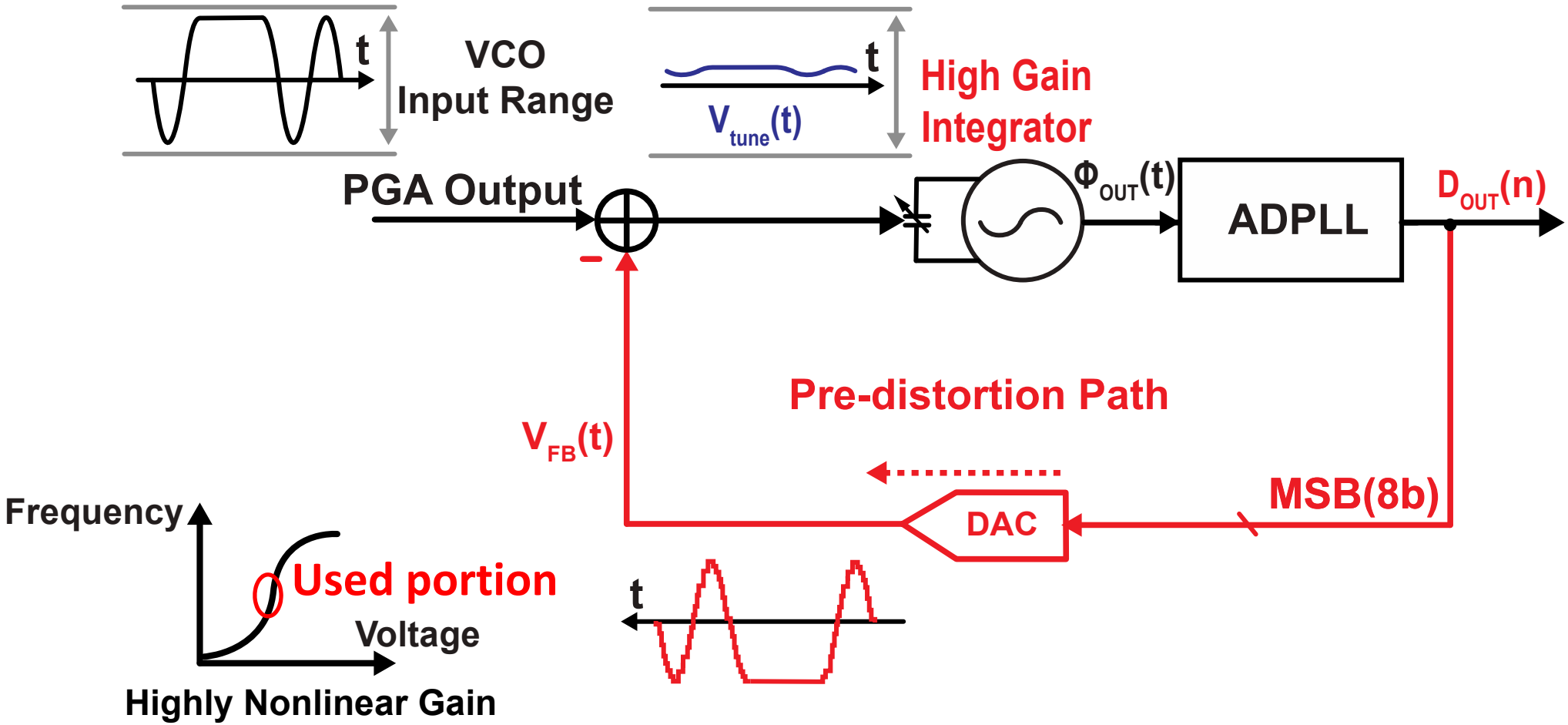
☹ Smaller varactor gain stresses TDC res. and linearity(large power)

Enhancement of Varactor Linearity



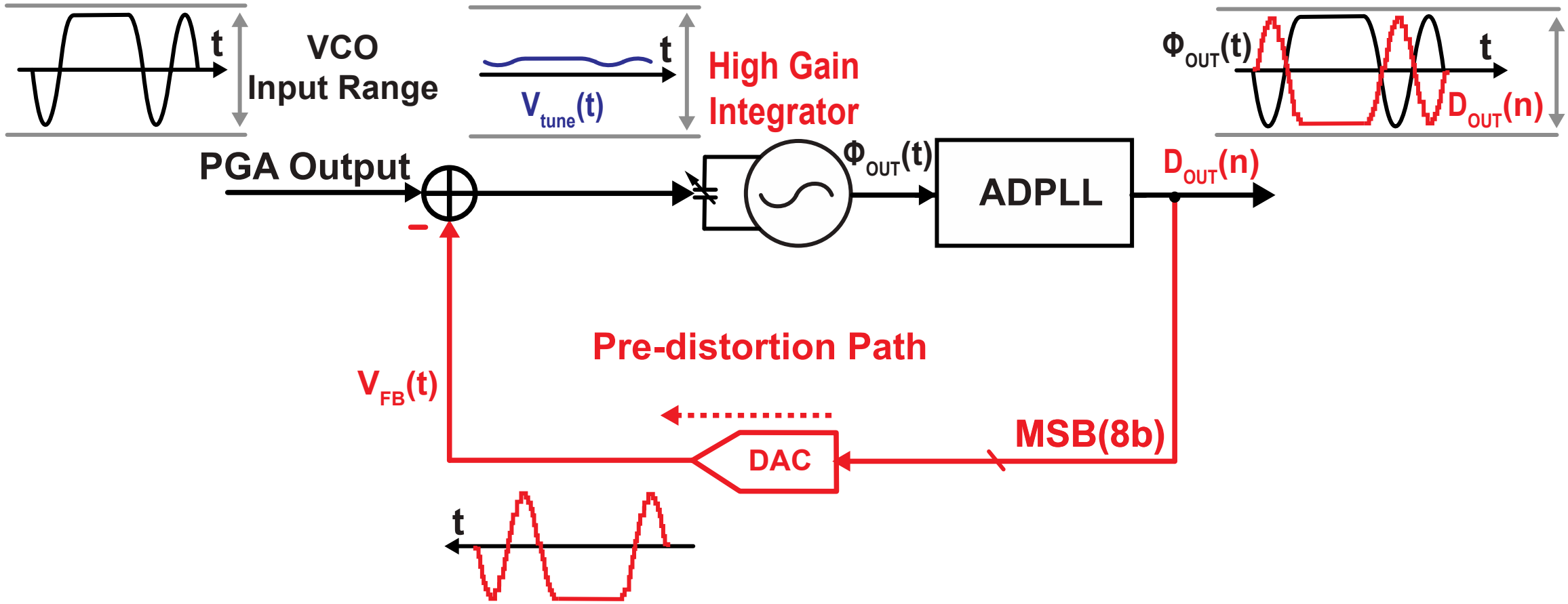
- Employ DAC feedback path at varactor input
- Effectively cancelled due to large loop bandwidth

Enhancement of Varactor Linearity



- **Only residue signal at varactor input**

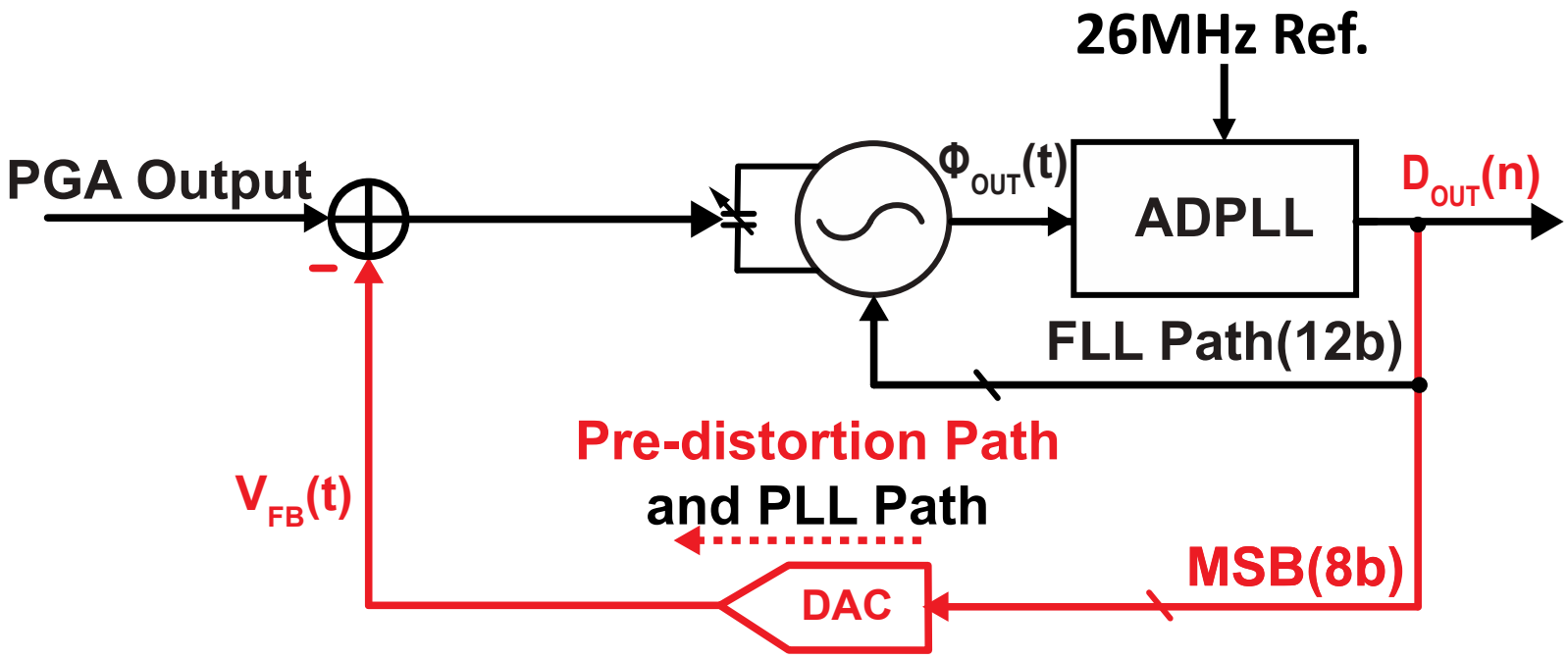
Enhancement of Varactor Linearity



☺ Enhanced varactor linearity

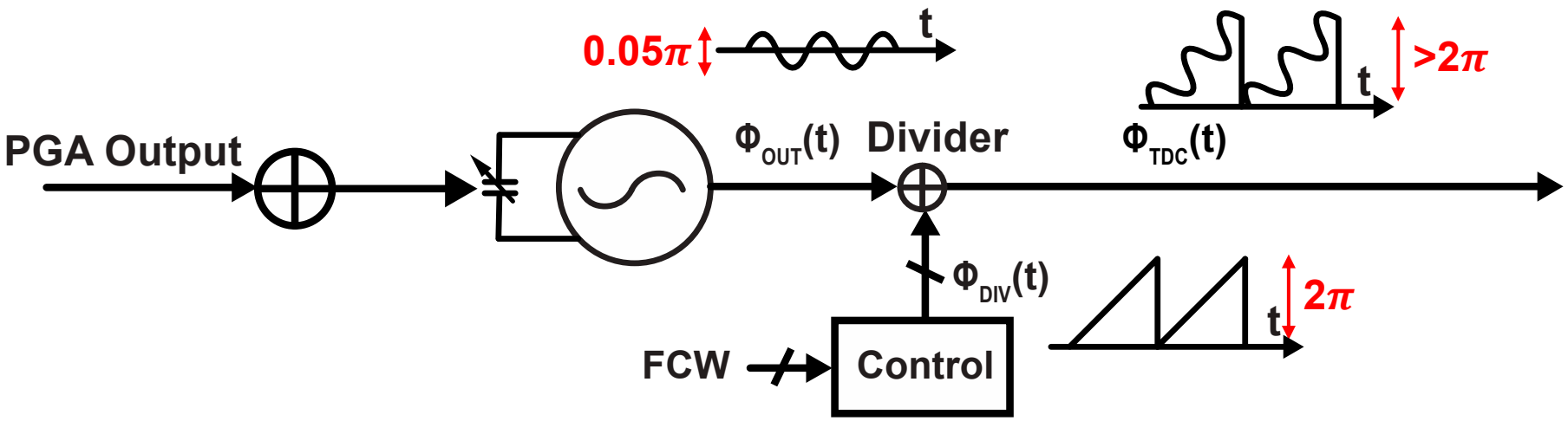
☺ Benefits from TDC resolution improvement(ADPLL also requires)

Enhancement of Varactor Linearity



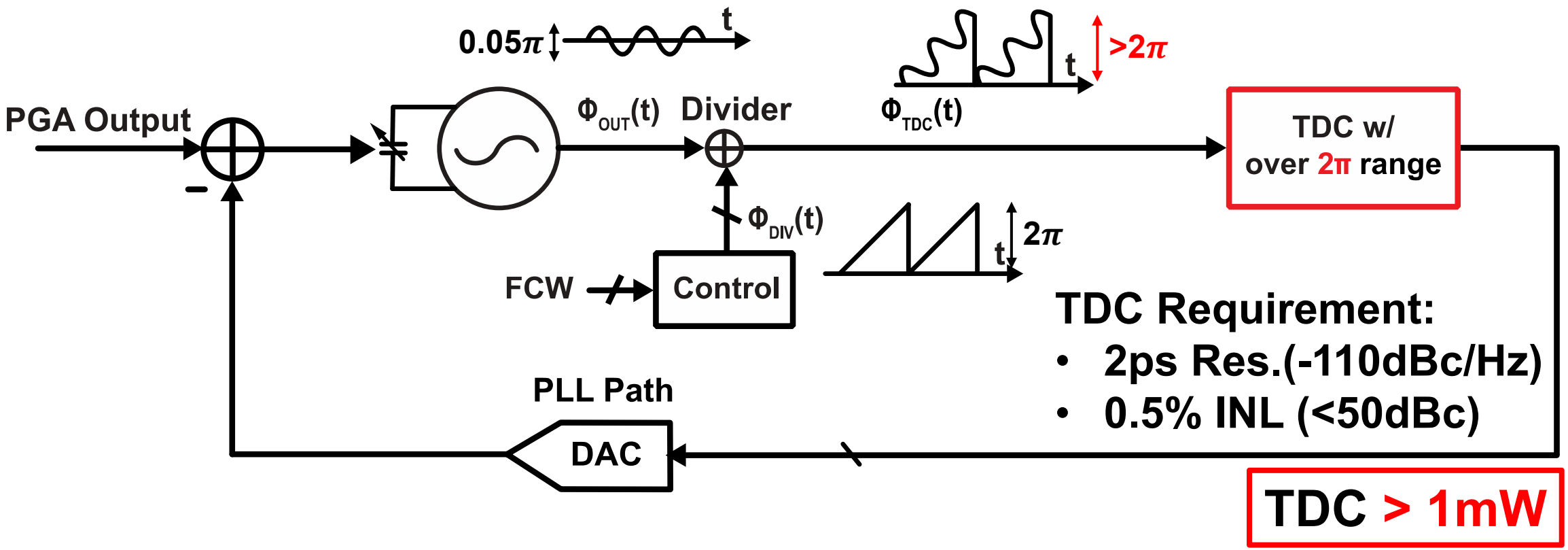
- Reuse DAC feedback path as PLL path

Enhancement of TDC



- 2π is equal to one oscillator period

Conventional Phase Quantization

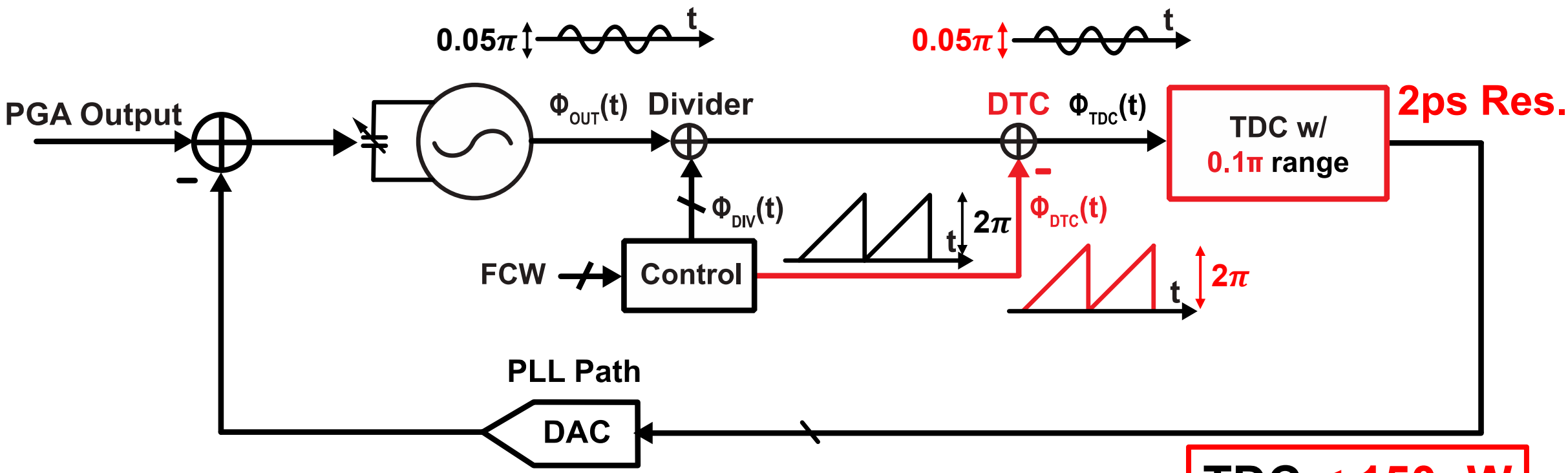


☹ Poor TDC resolution and linearity

☹ Large power consumption

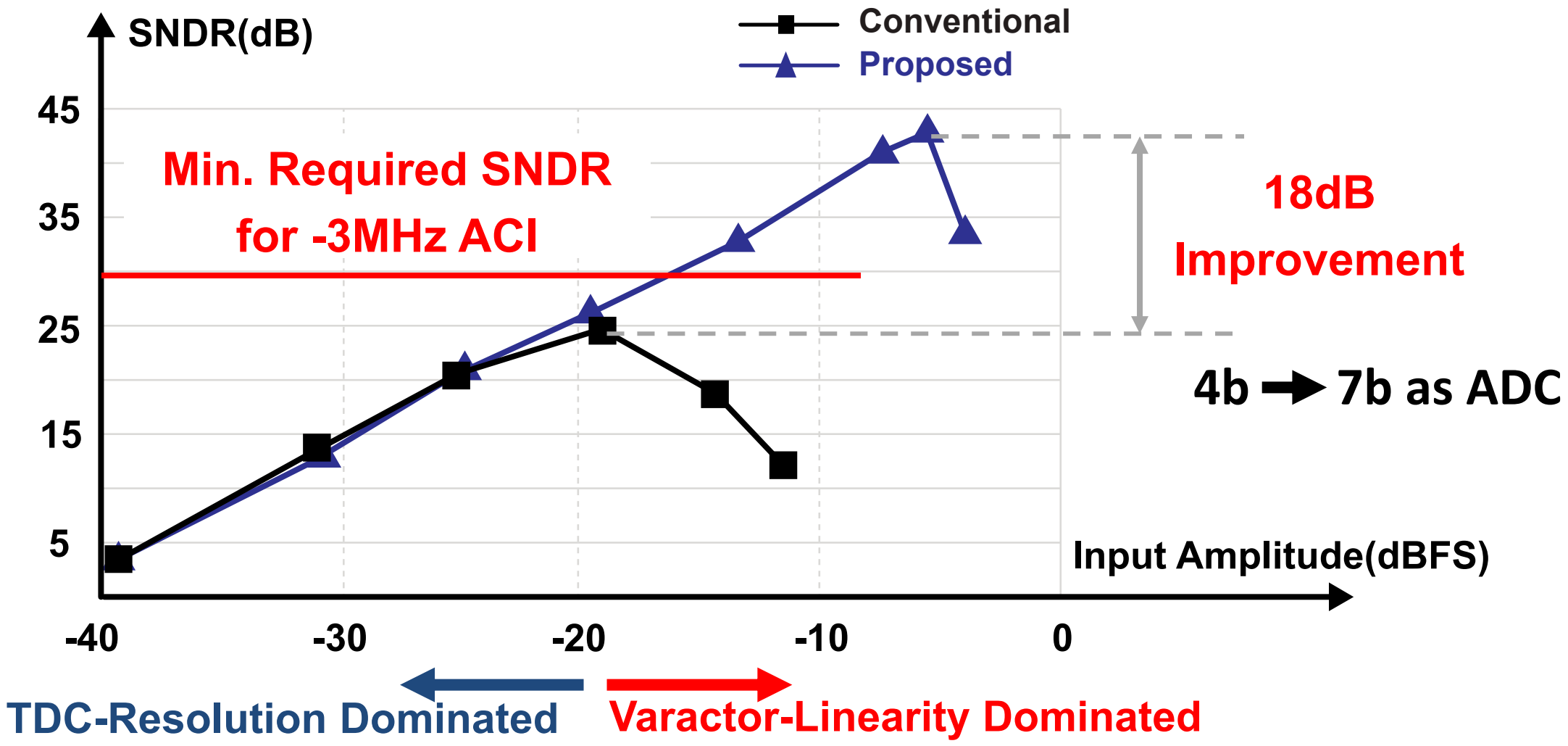
[H. Okuni, ISSCC 2016]

Enhanced Phase Quantization

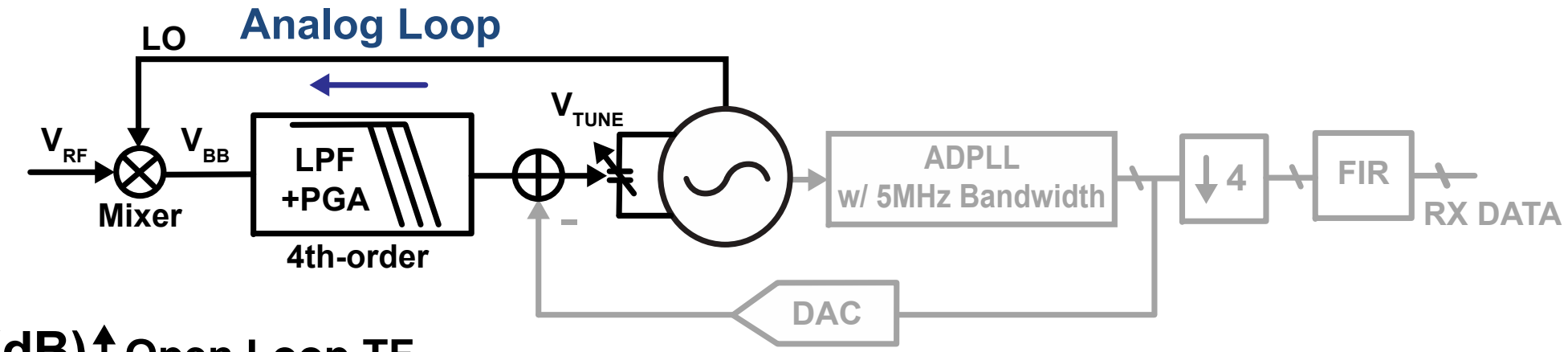


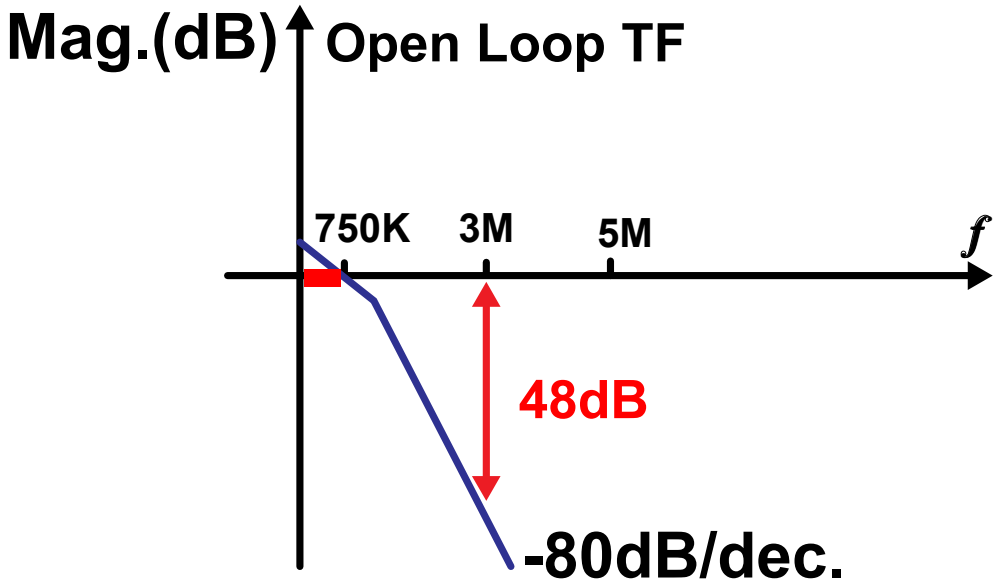
- ☺ Enhanced TDC resolution(2ps) and linearity
- ☺ Wide loop bandwidth operation with good in-band PN and spurs
- ☺ Lower power consumption

Measurement Results



Interference Immunity of Hybrid-loop

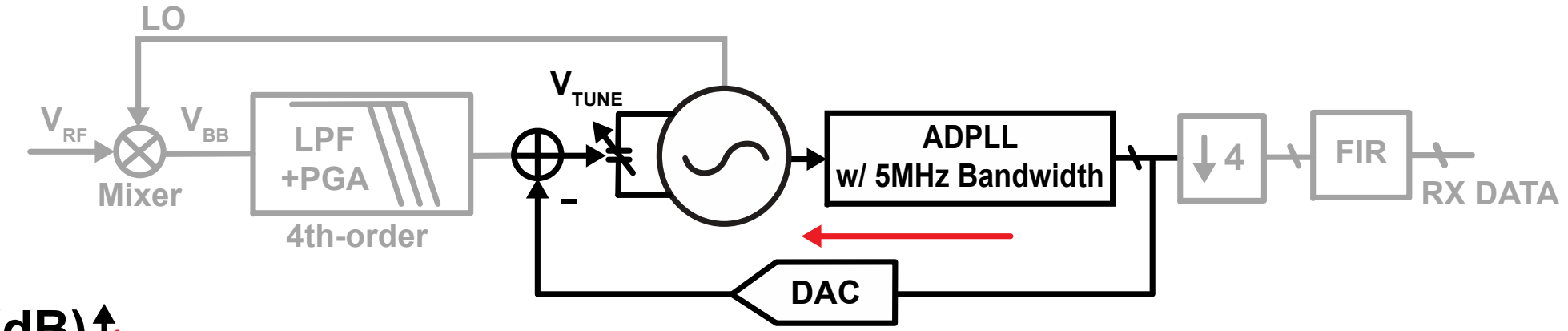




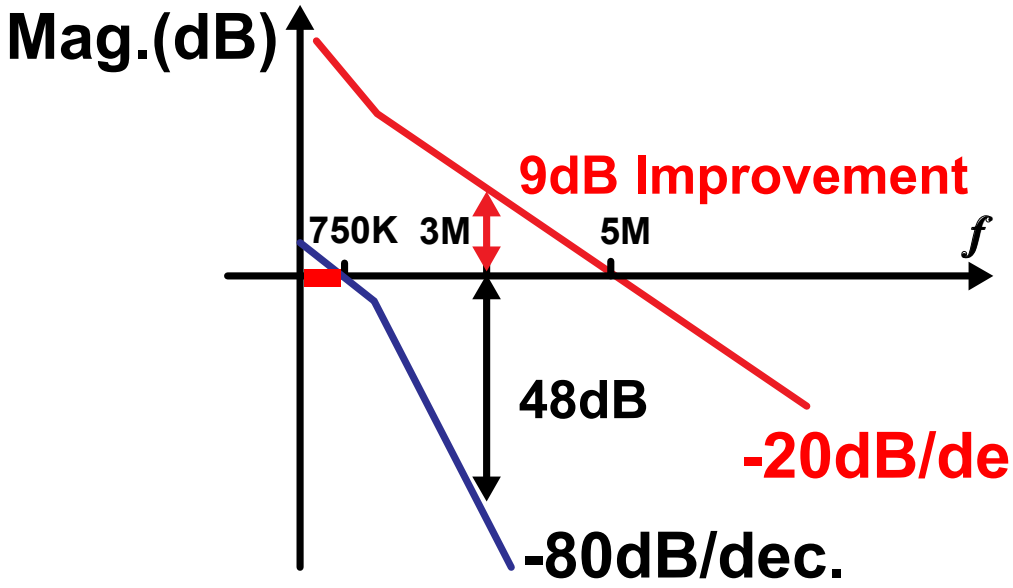
Analog Loop:

- **Narrow-bandwidth high-order LPF to suppress blocker power**

Interference Immunity of Hybrid-loop



Digital PLL Loop



Digital PLL Loop:

- **Wide-bandwidth ADPLL** to stable hybrid loop at blocker power

More than 57dB blocker immunity over 3MHz

Outlines

- Introduction and Prior Art
- Proposed BLE TRX
- **Measurement Results**
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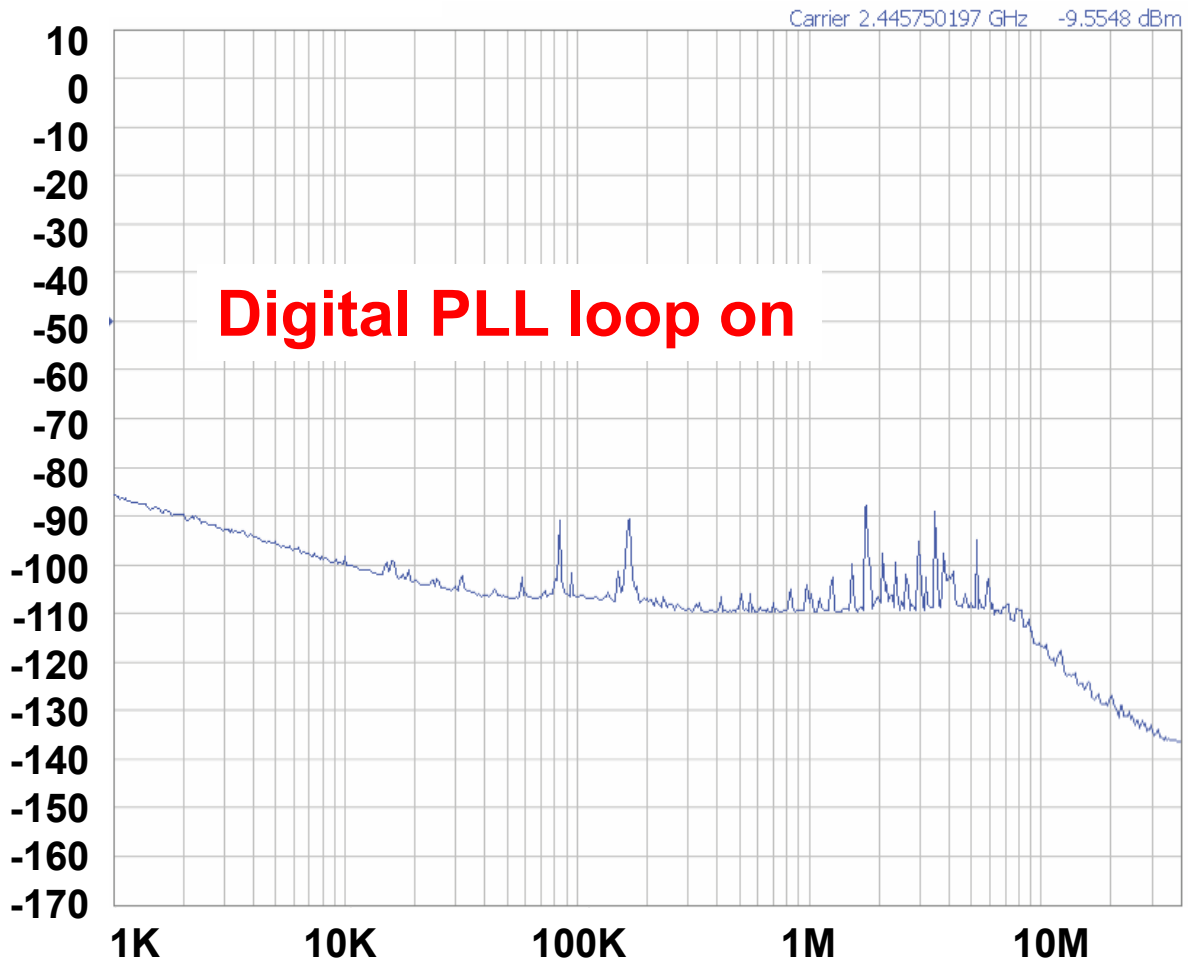
ADPLL Phase Noise

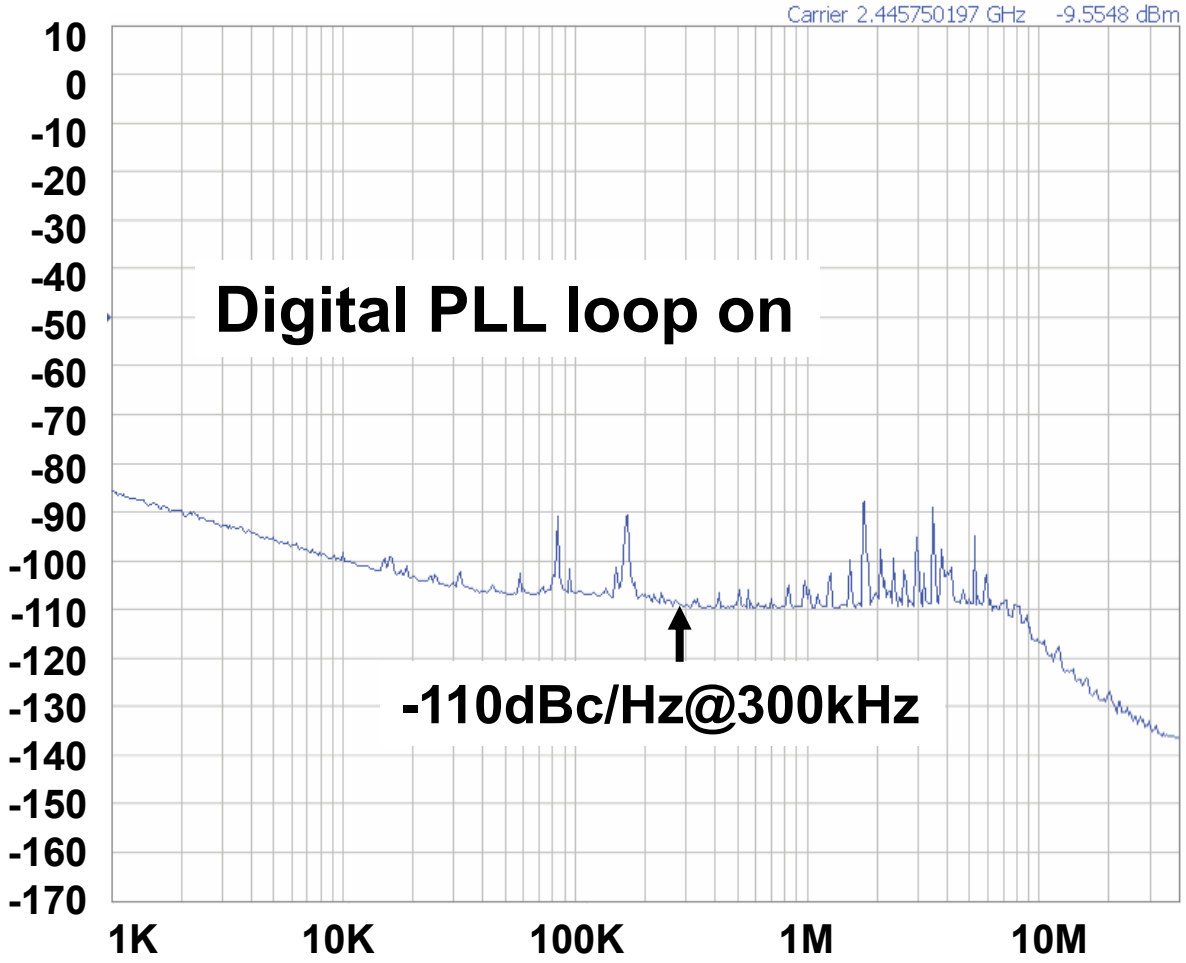


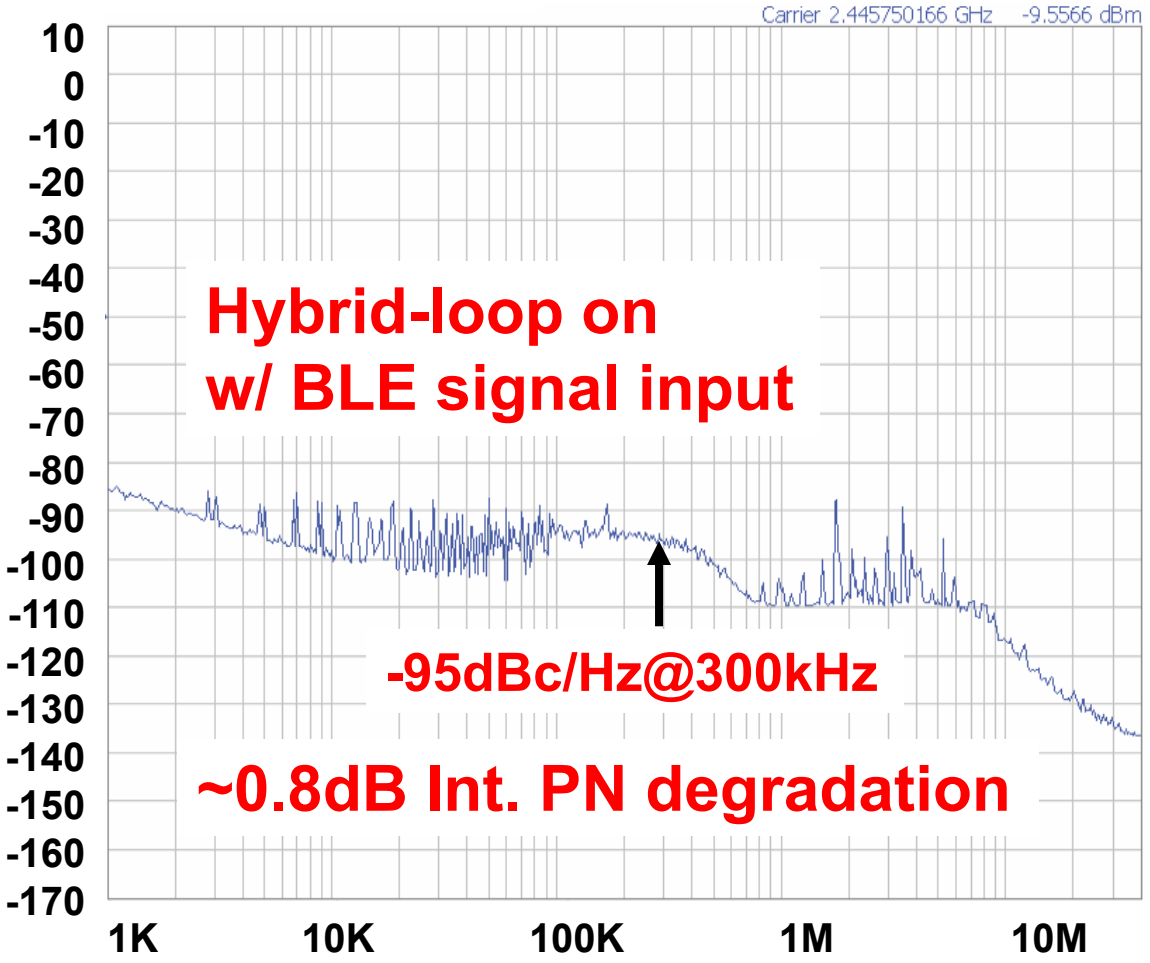
Requirement:

- **>4MHz bandwidth**
- **<-40dBc spur**
- **<-100dBc/Hz in-band PN**

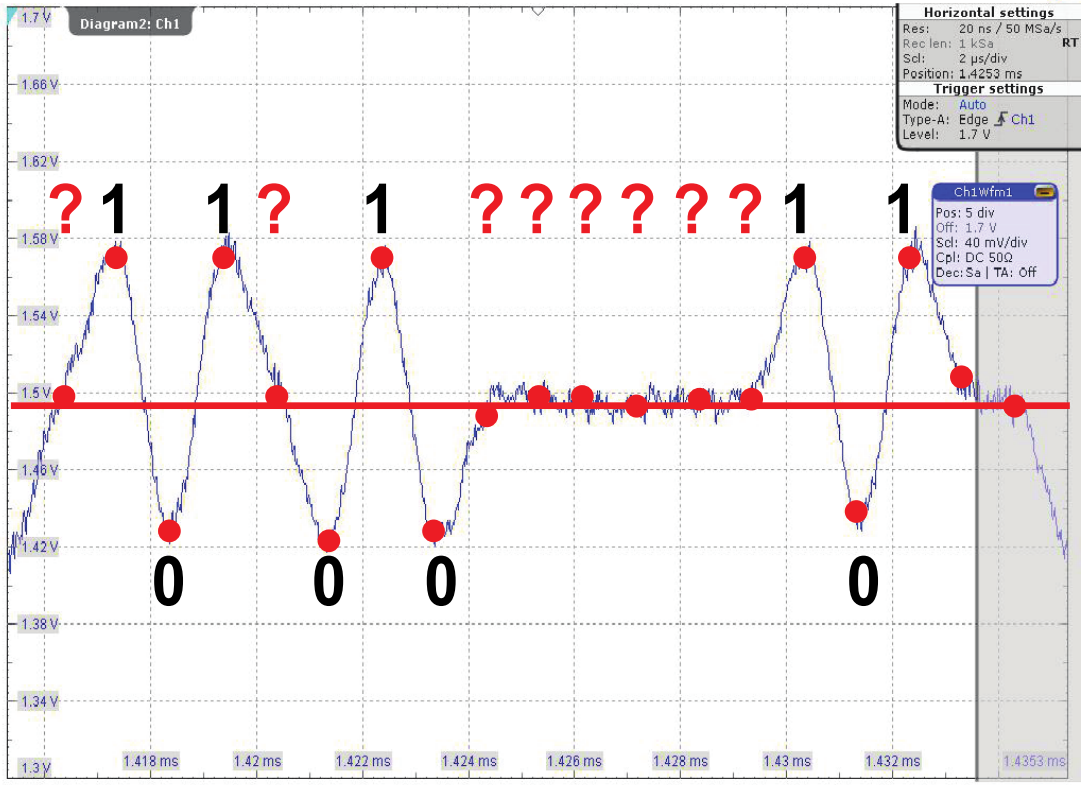
- **5MHz bandwidth**
- **<-50dBc fractional spur**
- **-110dBc/Hz in-band PN**

Phase Noise w/ Hybrid-Loop On

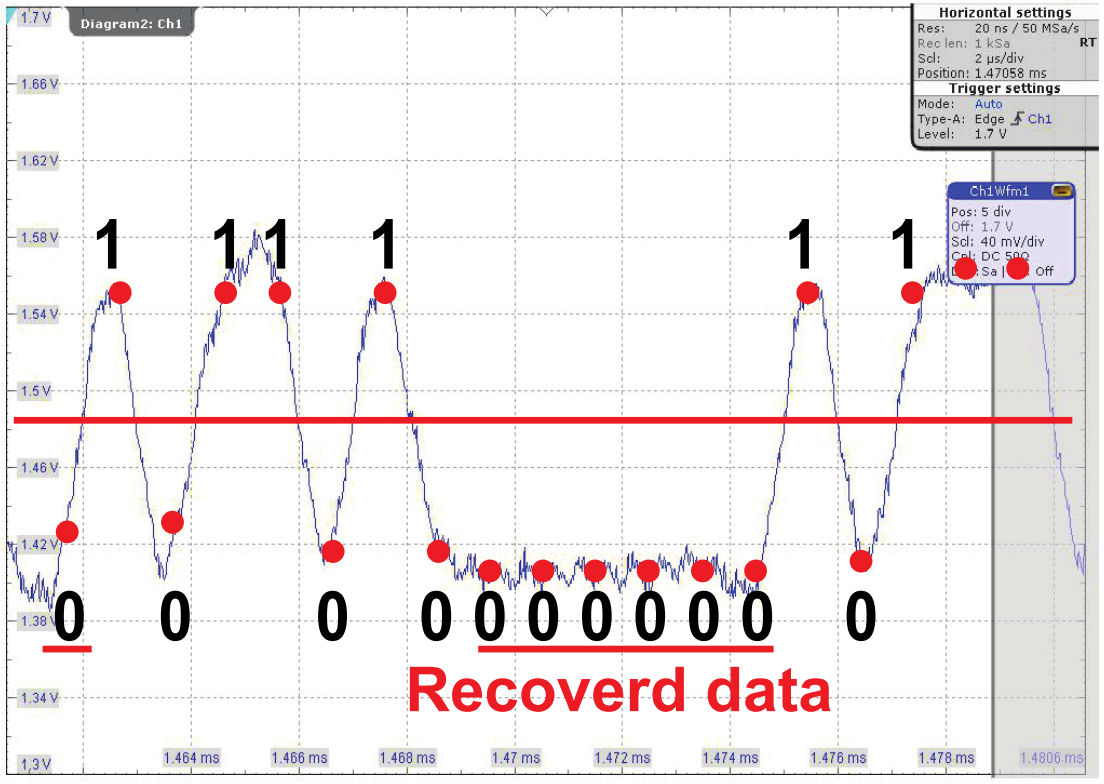




Phase and Frequency Synchronization

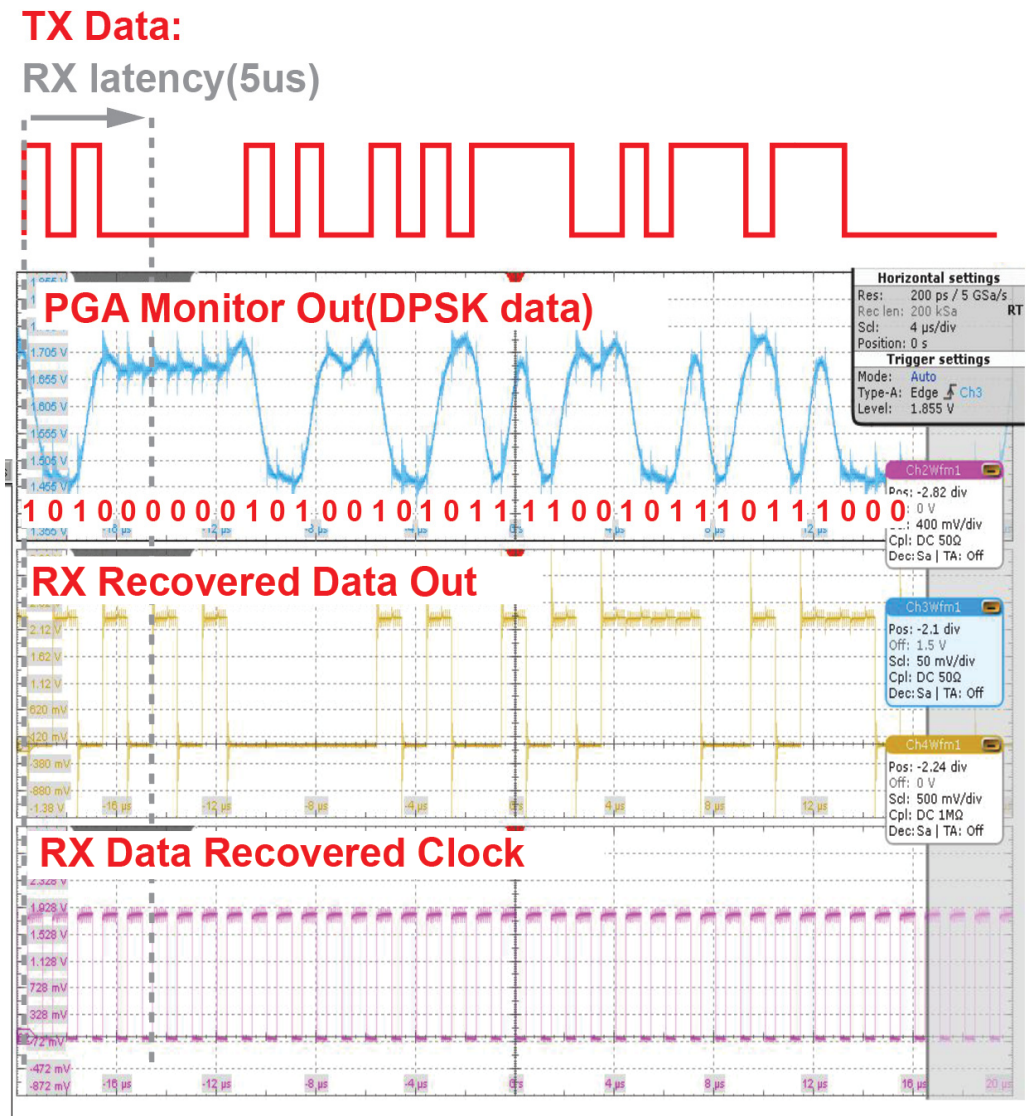


w/o Phase and Frequency Synchronization

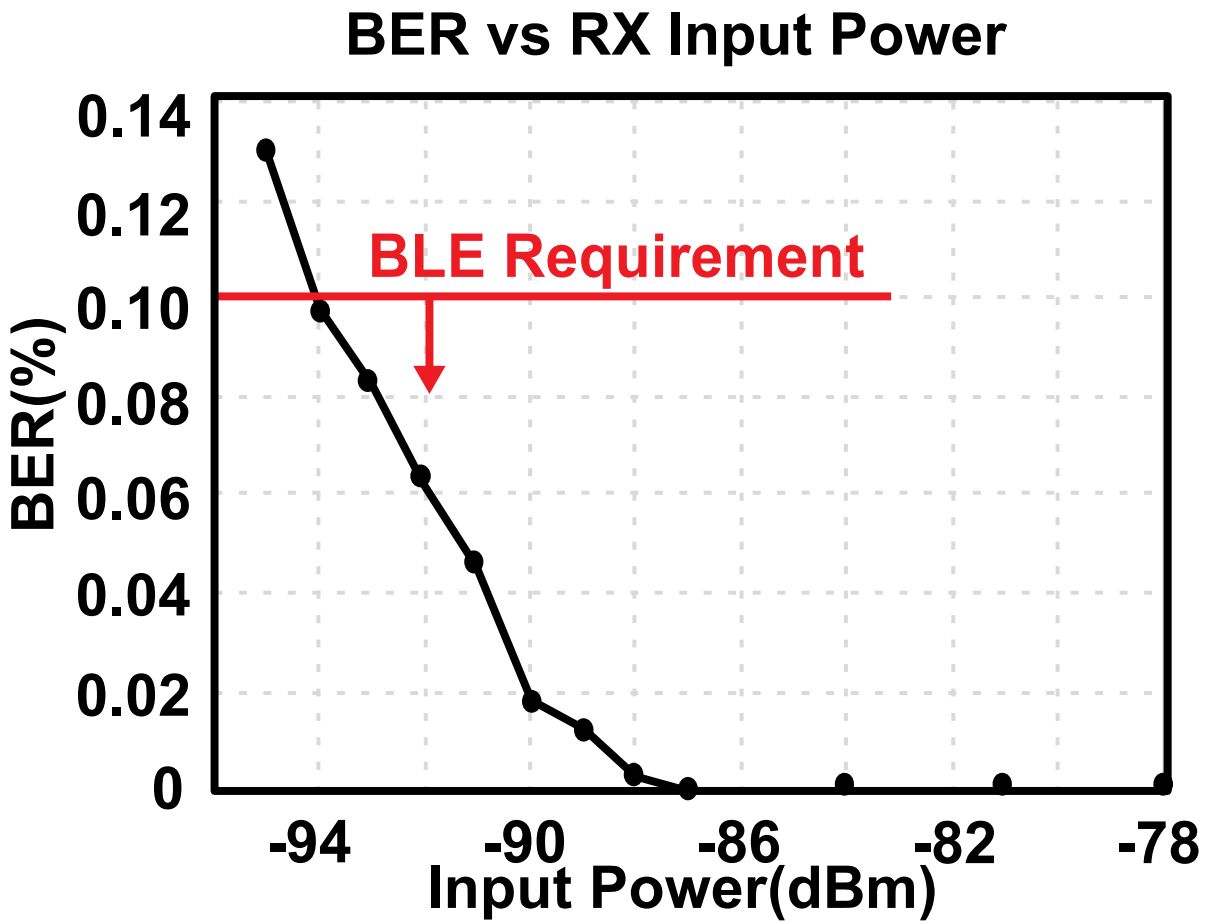


w/ Phase and Frequency Synchronization

Data Demodulation and Sensitivity

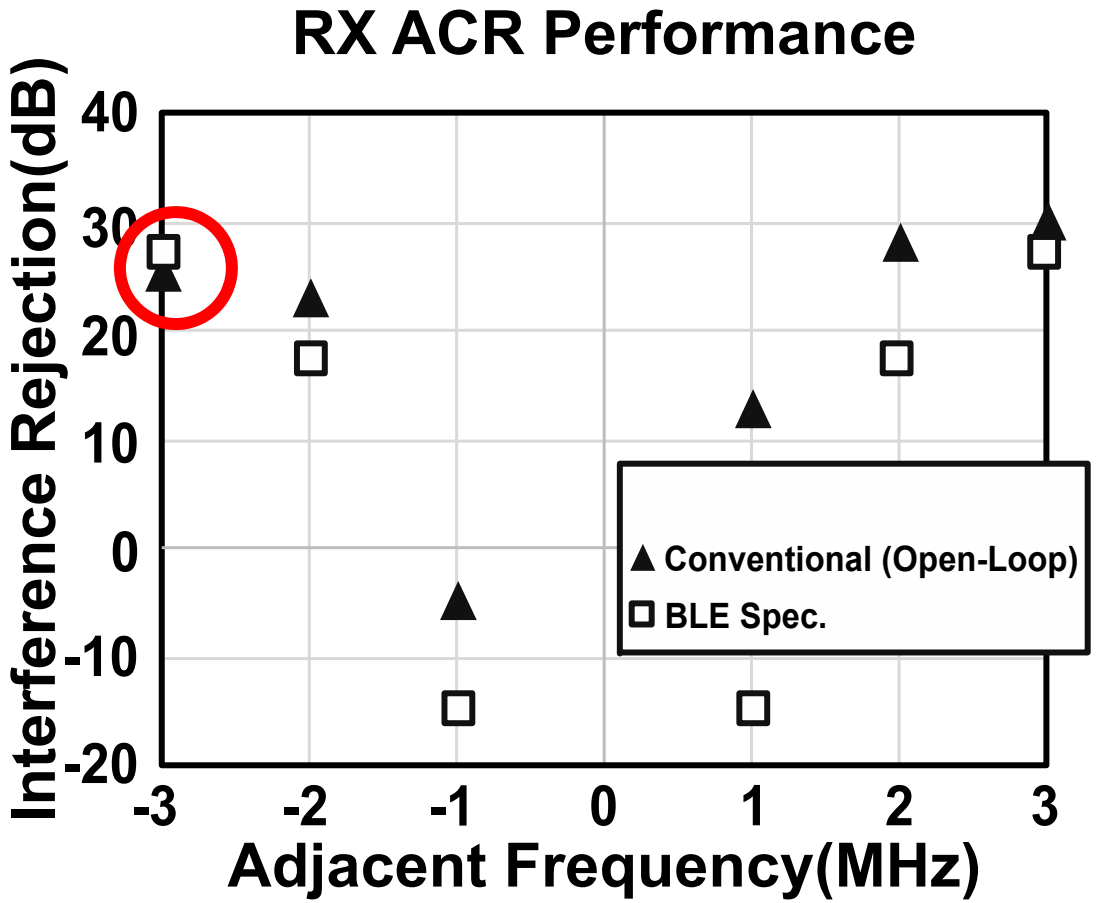


RX Sensitivity



Interference Tolerance

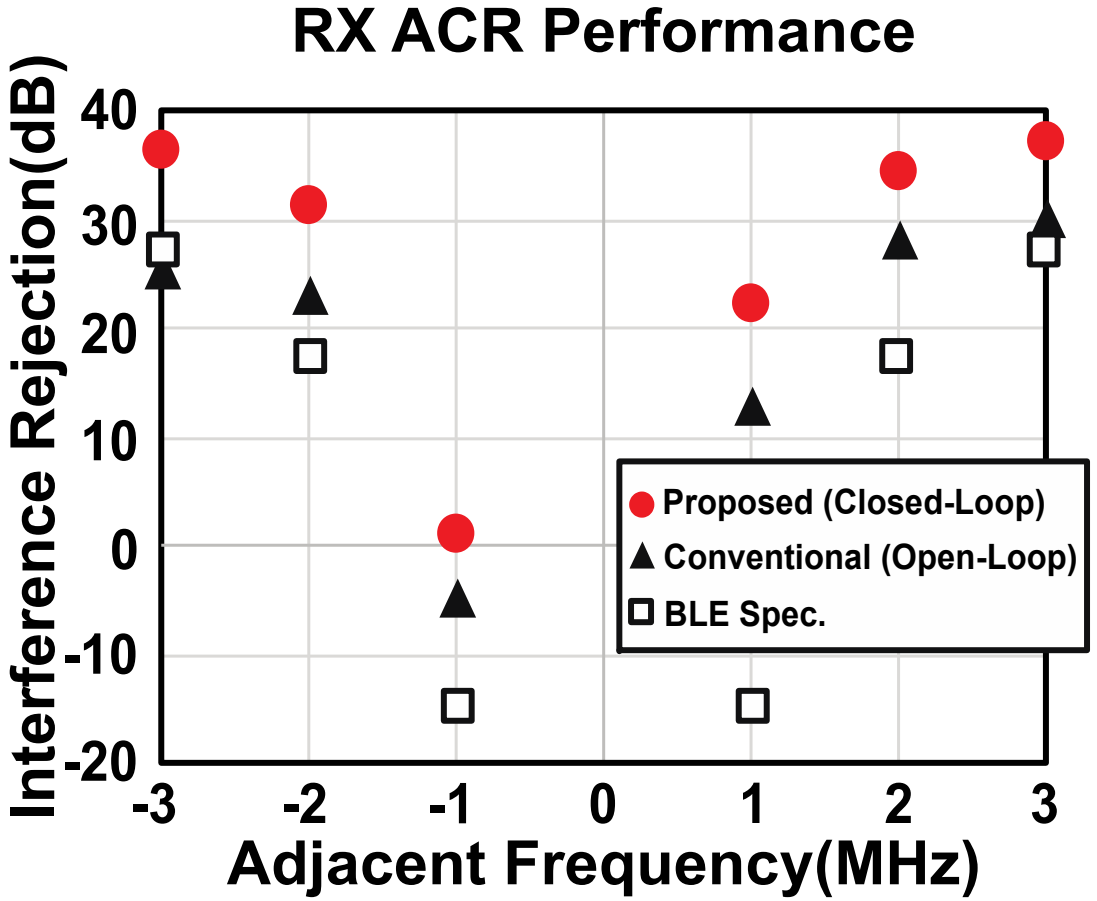
ADPLL w/o DAC feedback(Open-loop): (~4b ADC)

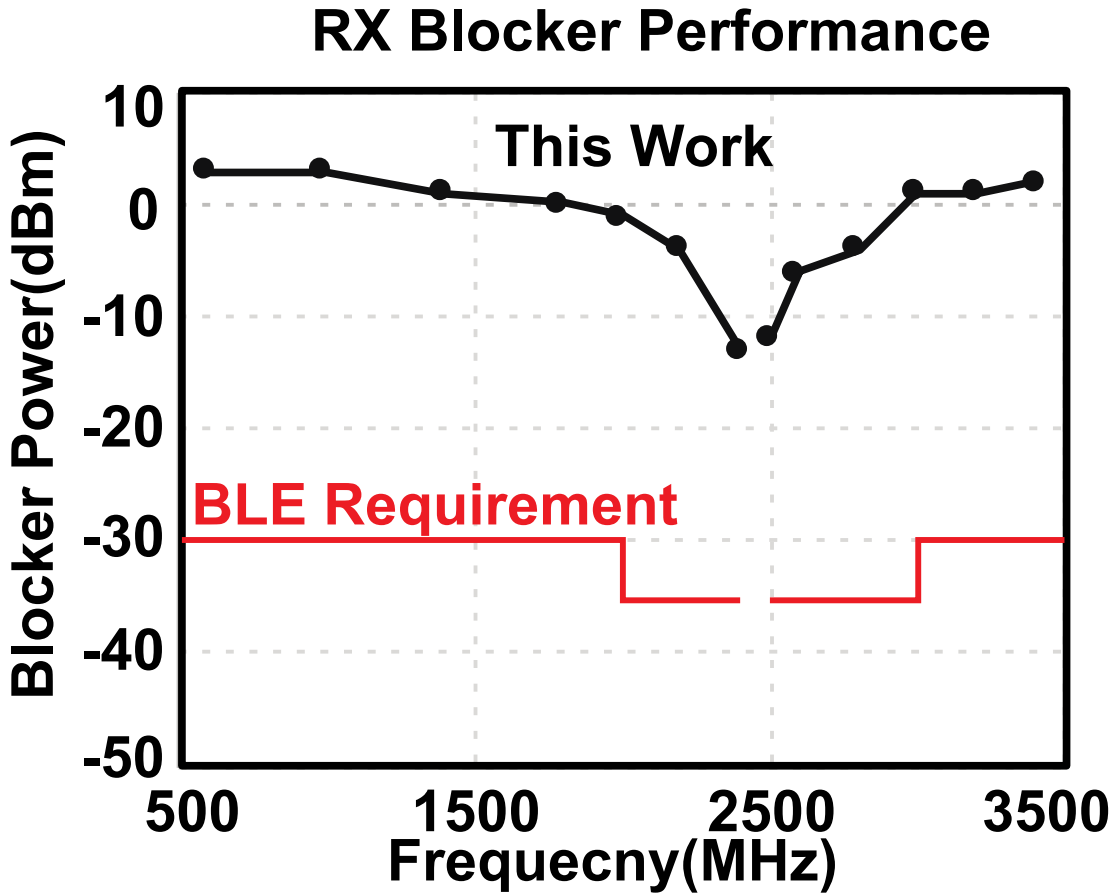


-3MHz ACR does not satisfy the BLE requirement

Interference Tolerance

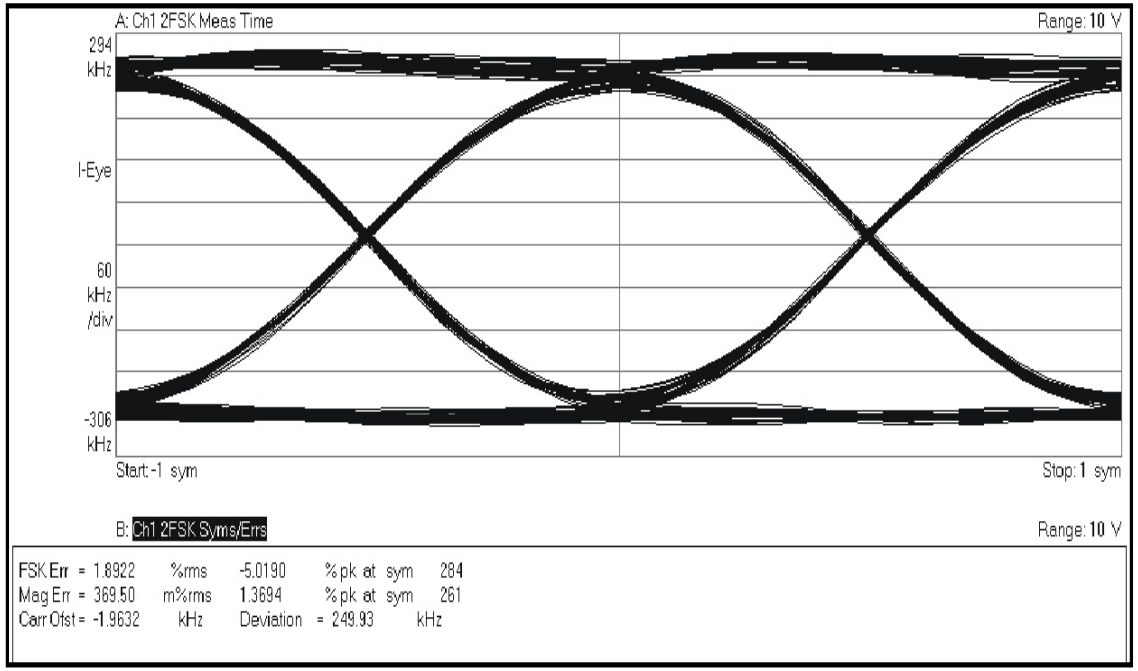
ADPLL w/ DAC feedback(Closed-loop): (~7b ADC)





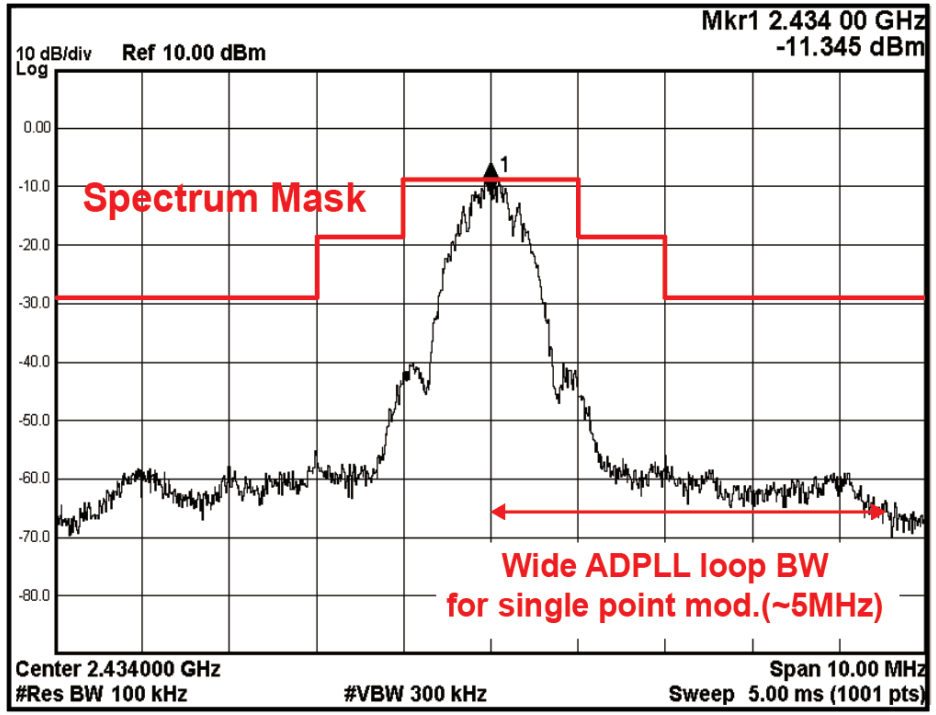
TX Eye Diagram and Spectrum Mask

Eye Diagram

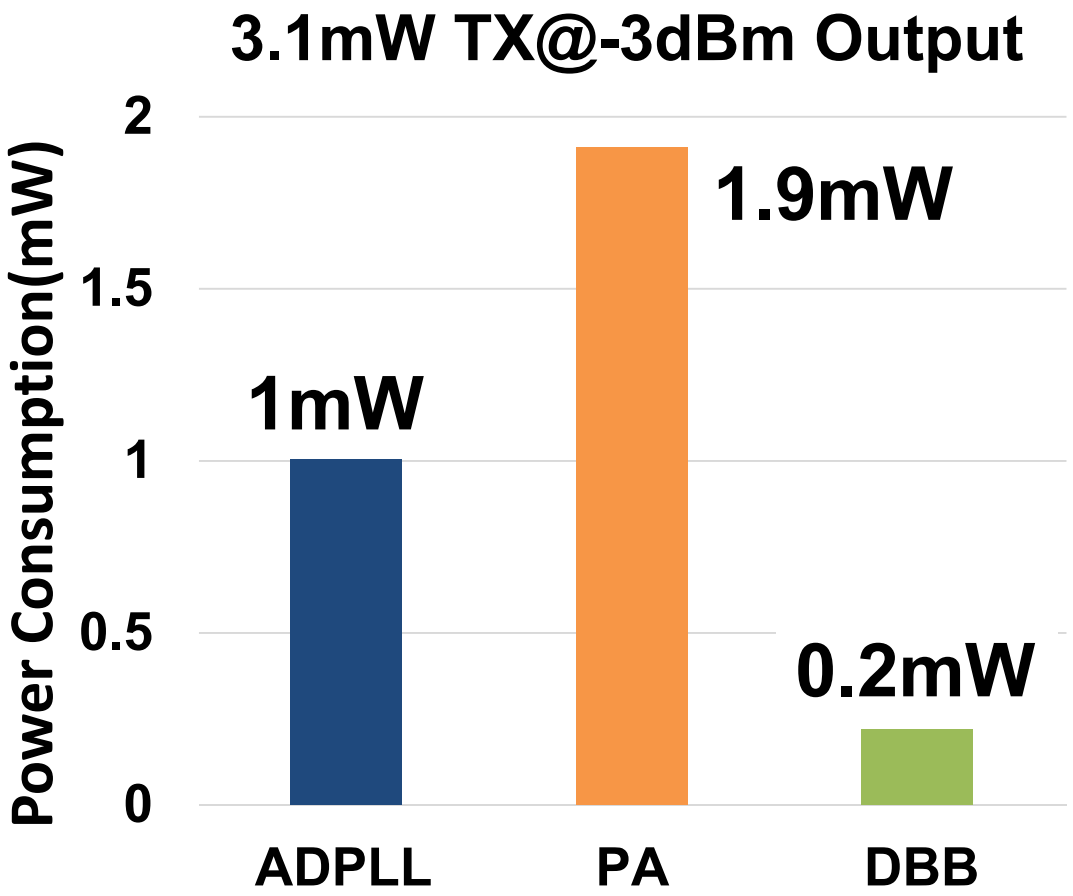


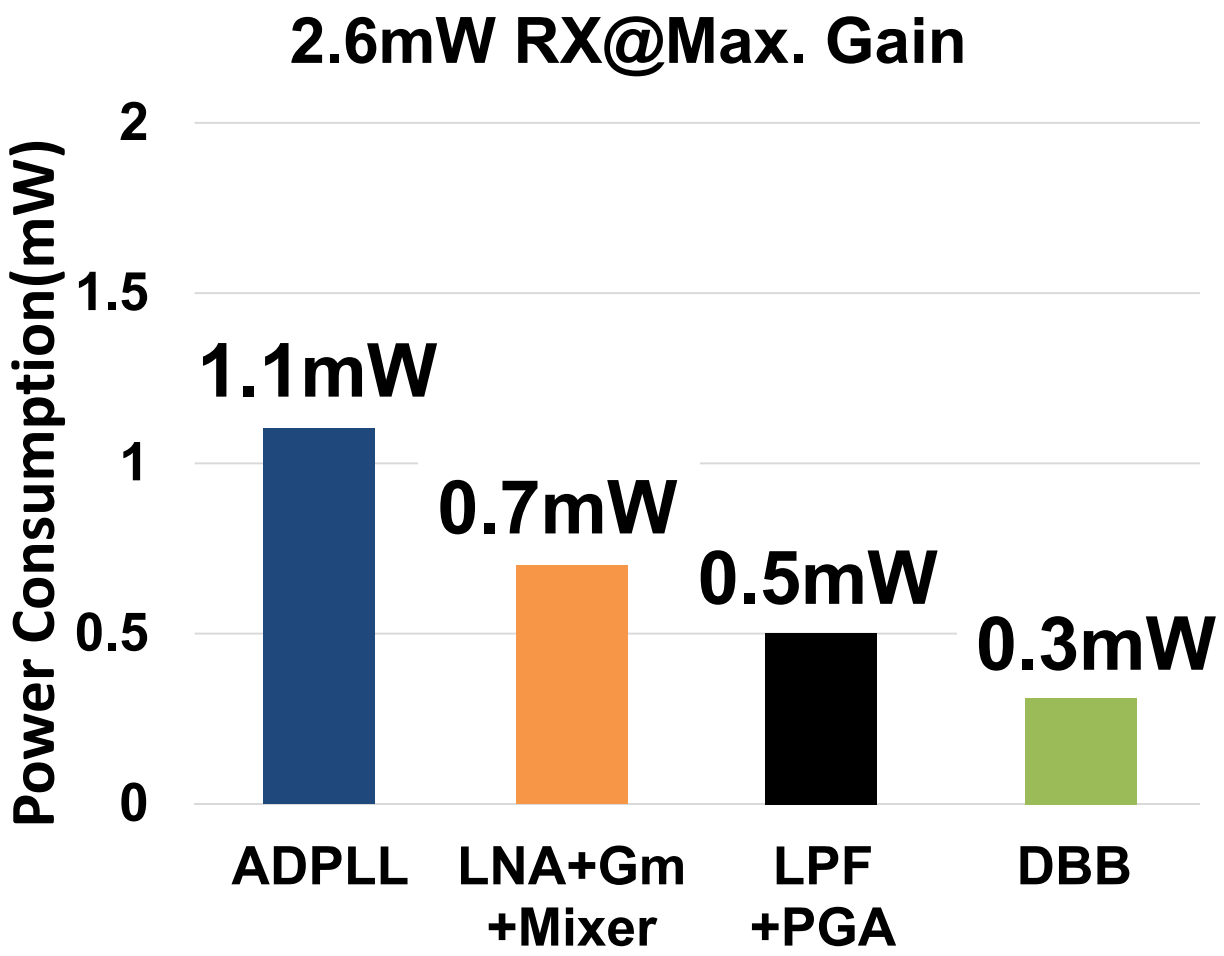
Freq. Deviation Error = 0.03%
FSK Error = 1.89%

Spectrum Mask

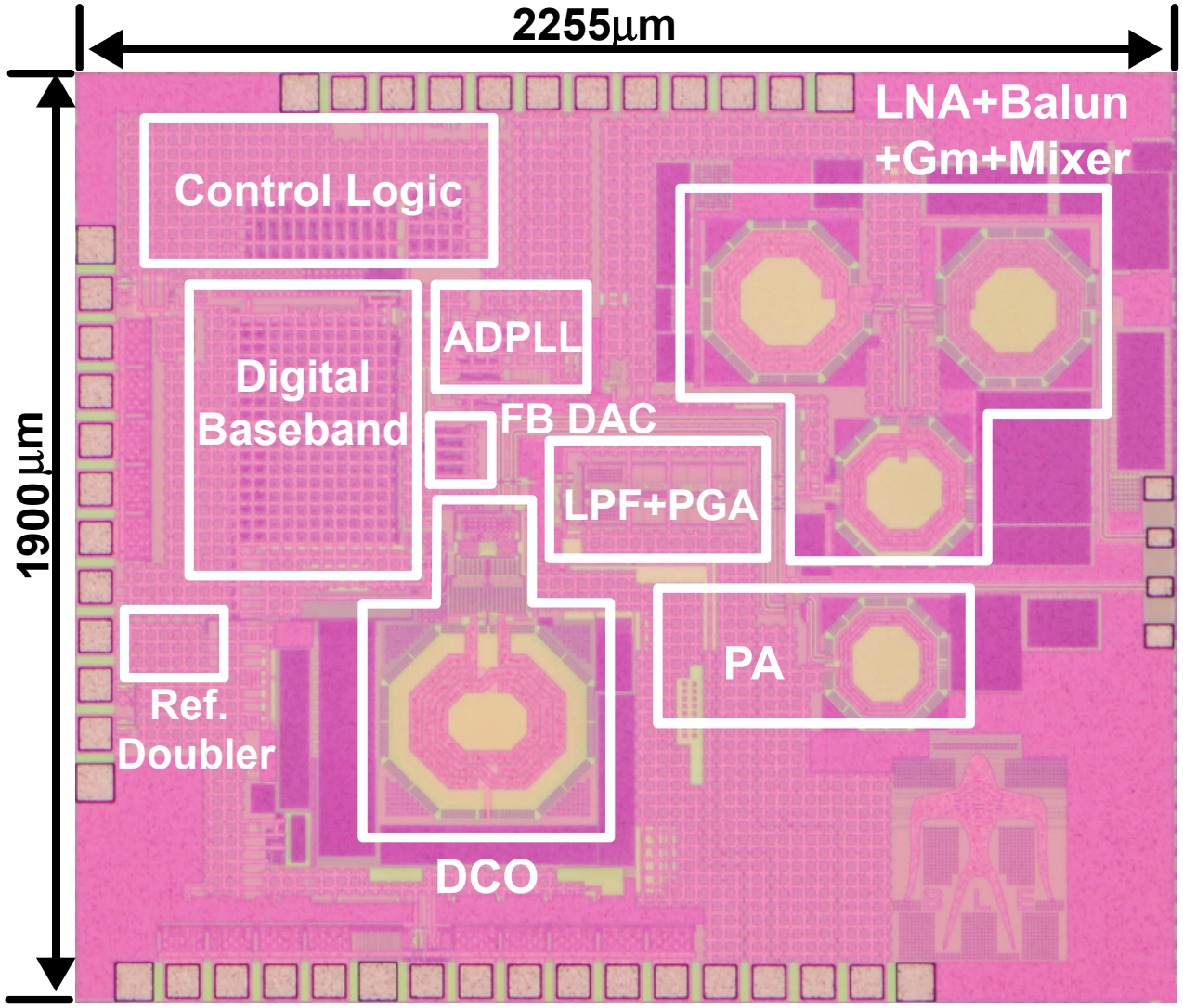


Power Consumption Break Down





Chip Photo



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RX Comparison

		This Work	ISSCC 16[1]	ISSCC 15[4]	ISSCC 15[5]
Technology		65nm CMOS	65nm CMOS	40nm CMOS	55nm CMOS
Integration Level		RF+ADPLL +DBB	RF+ADPLL +DBB	RF+PLL +PMU	RF+PLL+DBB +PMU
RX sensitivity		**-94dBm**	-90dBm	-94.5dBm	-94.5dBm
RX ACR		**1/31/36 dB**	N.A./24/29 dB	2/32/N.A. dB	N.A.
RX Blocker Tolerance (3~2000MHz, 2003~2399MHz, 2484~2997MHz, 3000~12750MHz)		**-1dBm, -13dBm, -12dBm, 1dBm**	-6dBm, -22dBm, -16dBm, 0dBm	-18dBm, -28dBm, -28dBm, -13dBm	4.5dBm, -9dBm, -9dBm, >9dBm
Power Consumption	**Analog**	**2.3mW**	5.5mW	6.3mW	11.2mW
	DBB	0.3mW	0.5mW	N.A.	

TX Comparison

		This Work		VLSI 16[2]	ISSCC 15[3]
Technology		65nm CMOS		28nm CMOS	40nm CMOS
Data Rate & Modulation		1-Mbps GFSK		1-Mbps GFSK	1-Mbps GFSK
TX Architecture		Single Point		Two Point	Two Point
Supply Voltage		1V		0.5/1V	1V
FSK Error(EVM)		**1.89%**		2.67%	4.8%
TX Output Power		-3dBm	0dBm	0dBm	-2dBm
Power Consumption	**Analog**	**2.9mW**	5mW	4.7mW	4.2mW
	DBB	0.2mW		N.A.	0.2mW

[1] H. Okuni, ISSCC 2016 [2] F.-W. Kuo, VLSI 2016 [3] Y.-H. Liu, ISSCC 2015

[4] T. Sano, ISSCC 2015 [5] J. Prummel,, ISSCC 2015

Conclusion

- The proposed BLE TRX achieves 2.3mW in RX mode and 2.9mW in TX mode.
- ADPLL works as ADC, and interference performances are improved by DAC feedback technique.
- Phase and frequency tracking loop by ADPLL improves hybrid-loop RX sensitivity.
- Single-point modulation mitigates calibration requirement and improves the EVM.

Acknowledgement

This paper is based on results obtained from a project commissioned by the New Energy and Industrial Technology Development Organization (NEDO).

A 0.8V 0.8mm^2 Bluetooth 5/BLE Digital-Intensive Transceiver with a 2.3mW Phase-Tracking RX Utilizing a Hybrid Loop Filter for Interference Resilience in 40nm CMOS

M. Ding[1], X. Wang[1], P. Zhang[1], Y. He[1], S. Traferro[1],
K. Shibata[2], M. Song[1], H. Korpela[1], K. Ueda[2],
Y.-H. Liu[1], C. Bachmann[1], K. Philips[1]

[1]Holst Centre / imec, Eindhoven, The Netherlands
[2]Renesas Electronics, Tokyo, Japan

Outline

- Introduction
- The proposed BLE/BT5 radio
  - Phase-tracking RX with hybrid loop filter
  - Frequency-Modulation (FM) interface
  - Digital-assisted automatic calibrations
- Implementations
  - Receiver
  - Transmitter
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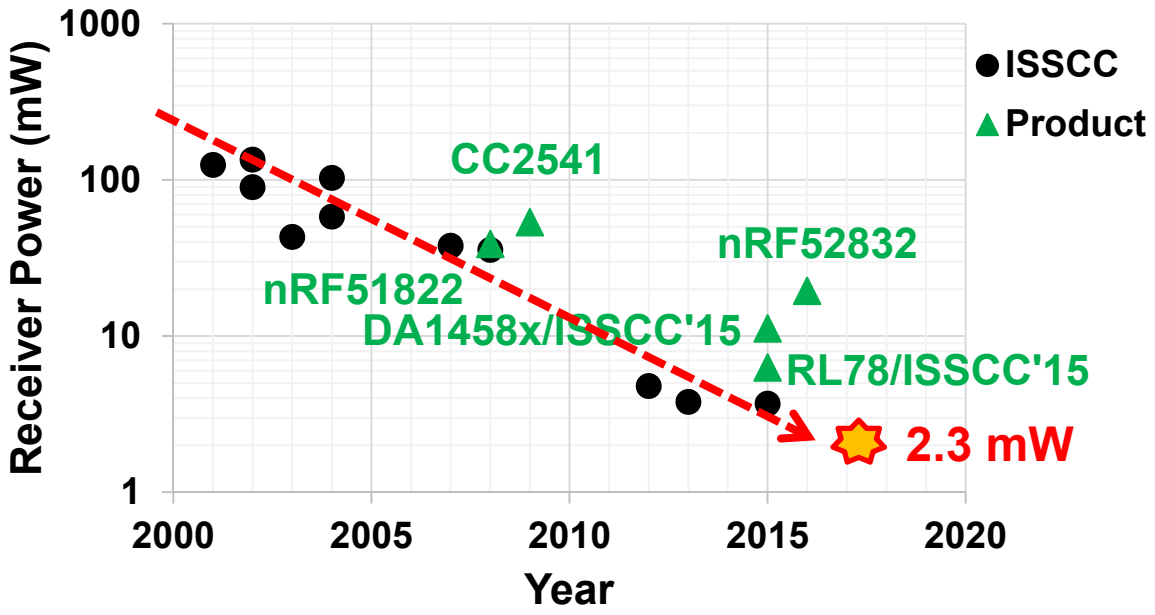
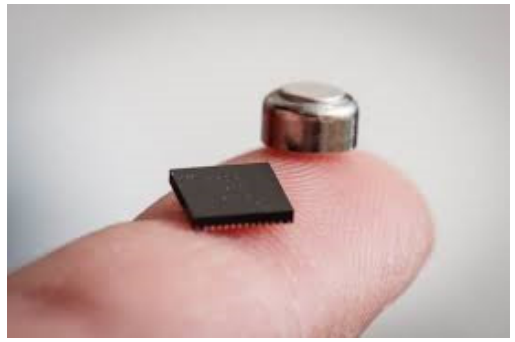
Bluetooth for IoT

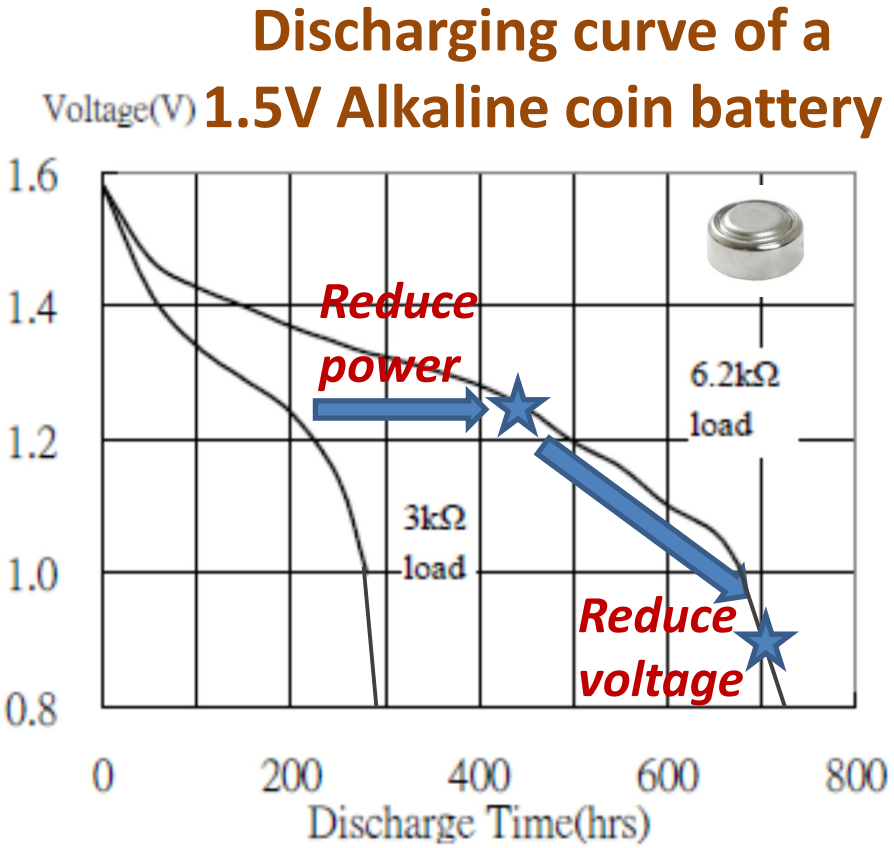


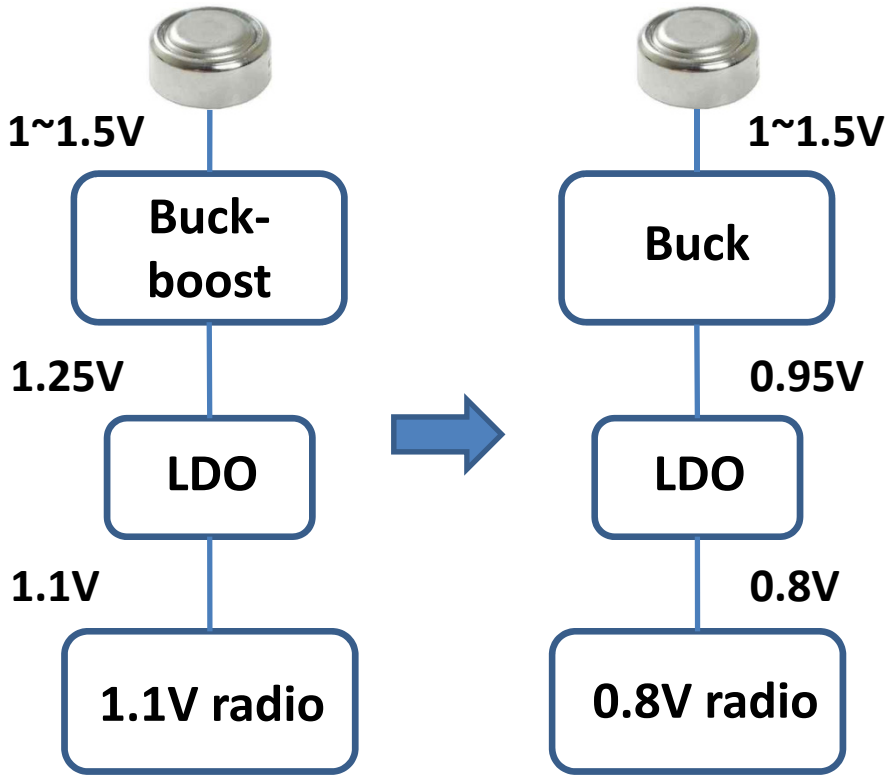
Bluetooth 5



- BT5: 2x higher data rate, 4x longer range, 8x longer packet to improve broadcasting capability
- Requirements:
  - Low-power and low supply voltage for long battery life time
  - Small die area and low BOM for low cost and module size

Longer battery life time





Reduce RF supply from typical 1.1V to 0.8V

- Extend battery life up to 50%
- Simplify DC-DC design (no boost) & improve efficiency + wide range of energy source

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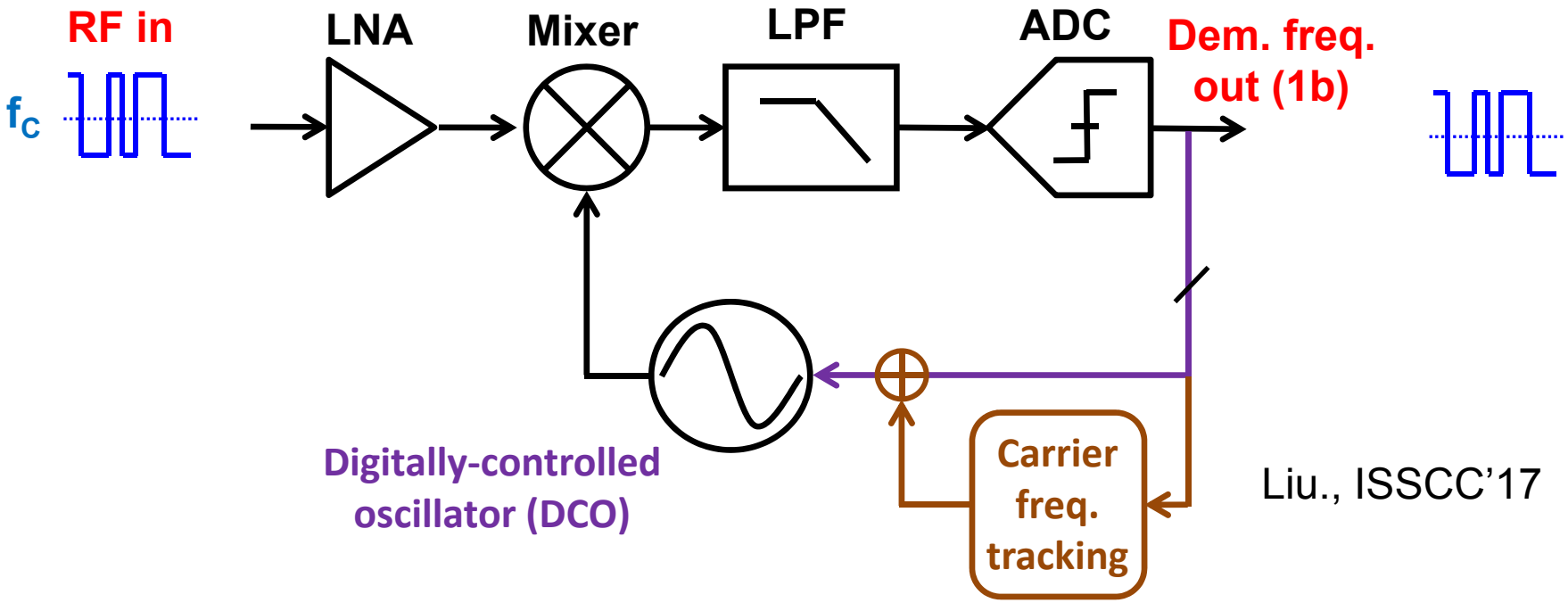
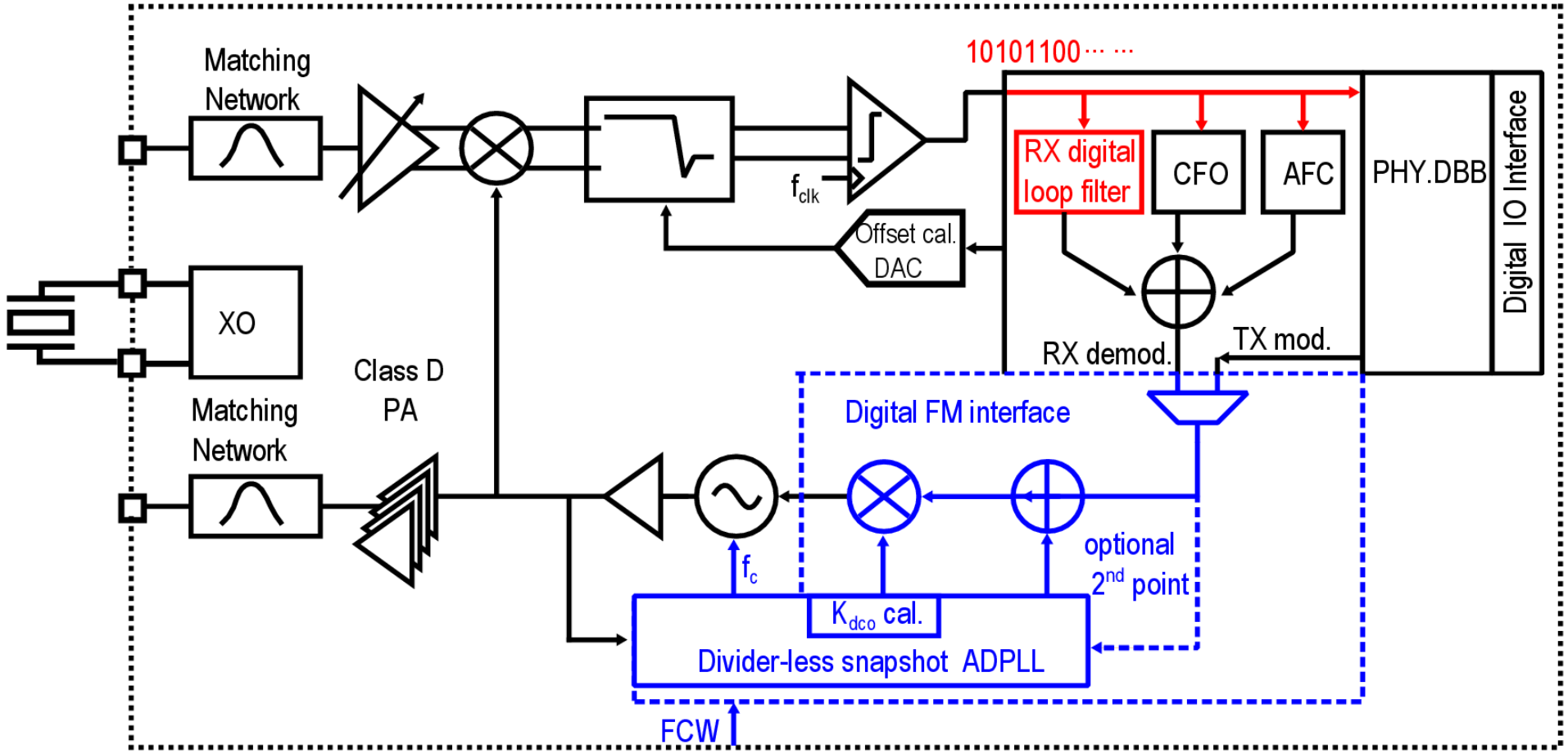
Prior-art: phase-tracking RX



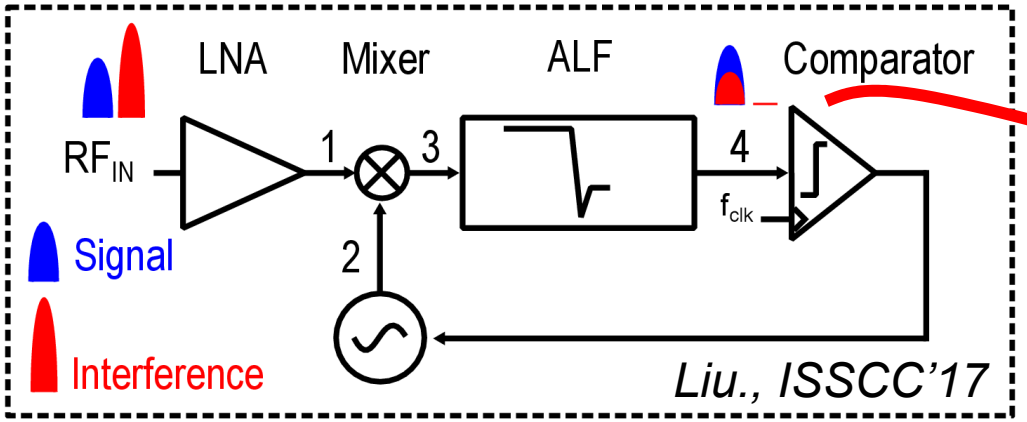
- Pros:
  - Low supply voltage
  - Low-power
  - Low-area
- Cons:
  - Limited Adjacent-Channel Rejection (ACR)
  - Sensitivity degraded due to lack of frequency control

The proposed BLE/BT5 radio

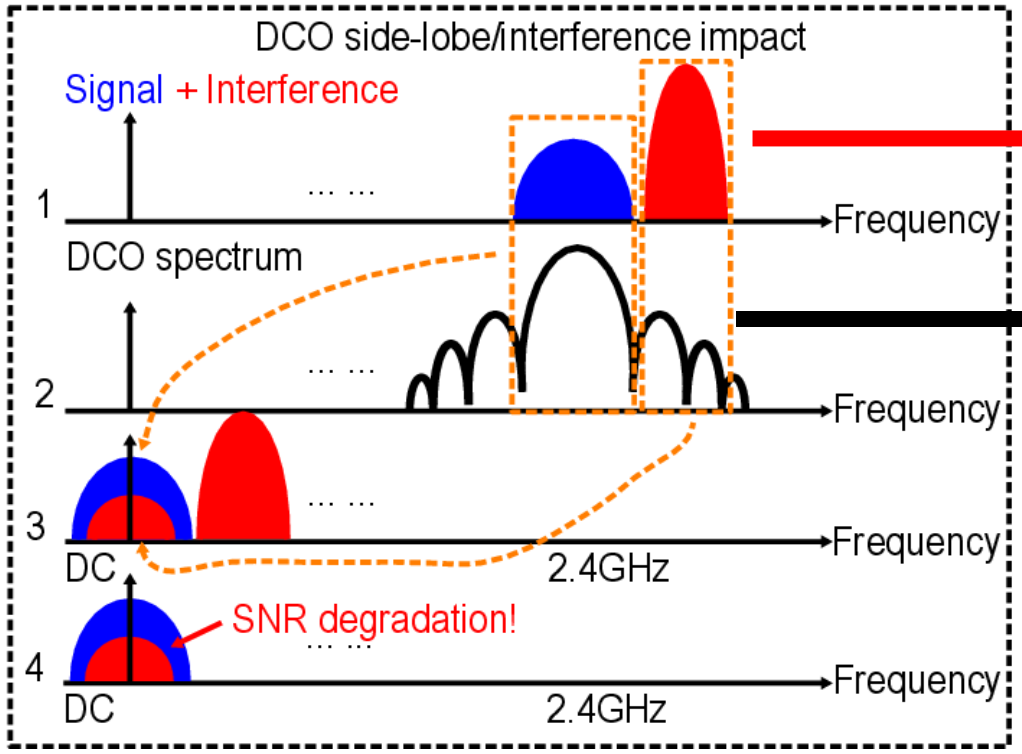


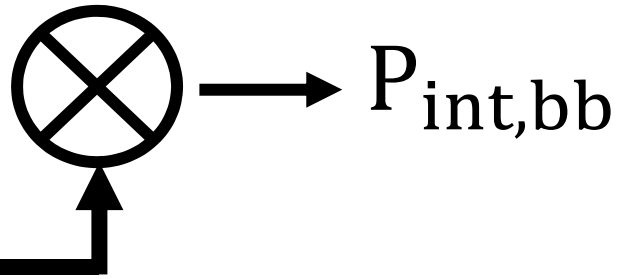
- Phase-tracking RX with hybrid loop filter for interference resilience
- Digital TX: divider-less snapshot ADPLL to define initial frequency + Class D digital PA
- Digital-intensive front-end and digital baseband enabling automatic calibrations

Adjacent-Channel-Rejection (ACR)



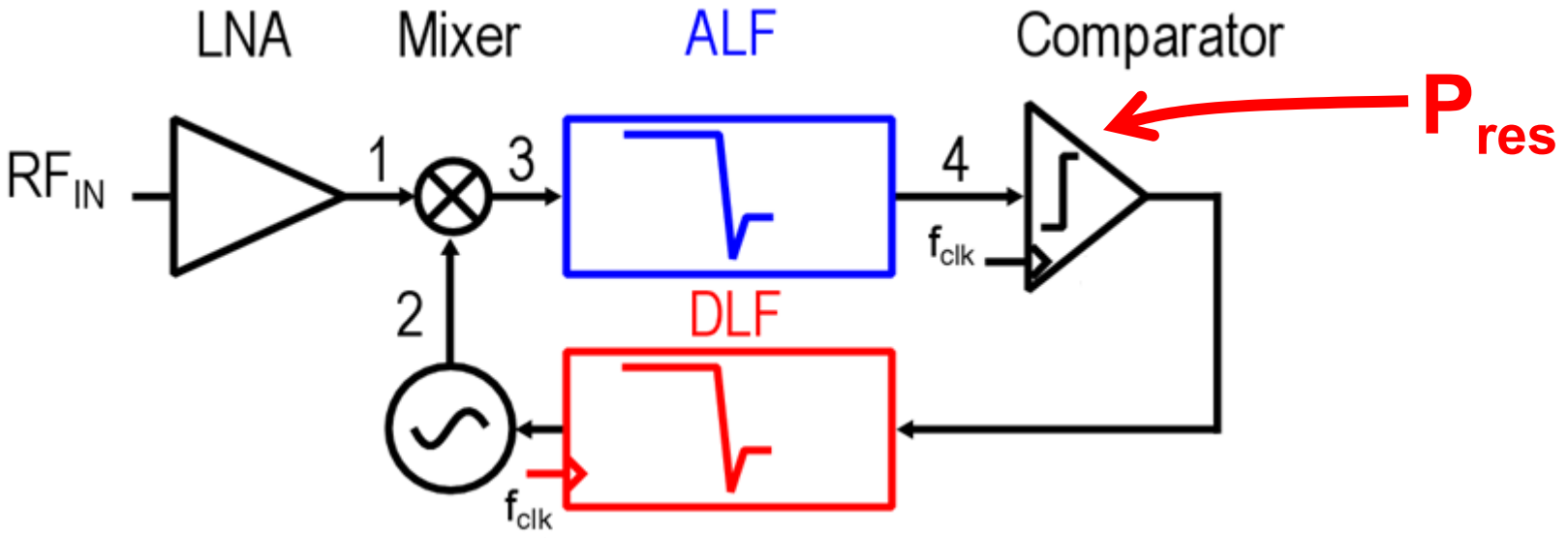
Error sources	Solution
P_{RES} Interference residue	***Analog loop filter (ALF)***
$P_{int,bb}$ Due to DCO slide-lobe energy	×



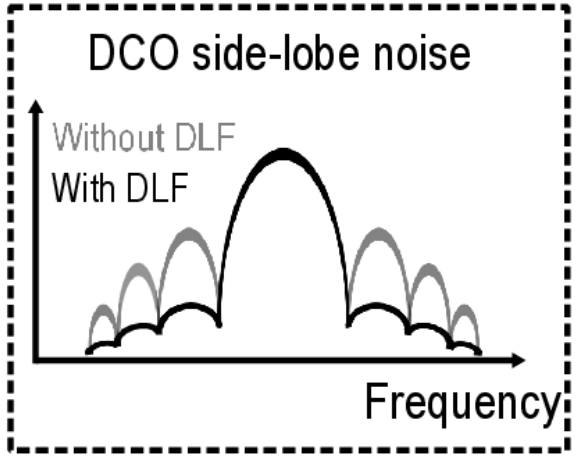


$$\mathrm{SNR}_{\mathrm{int}} = \frac{P_{sig,bb}}{P_{int,bb}}$$

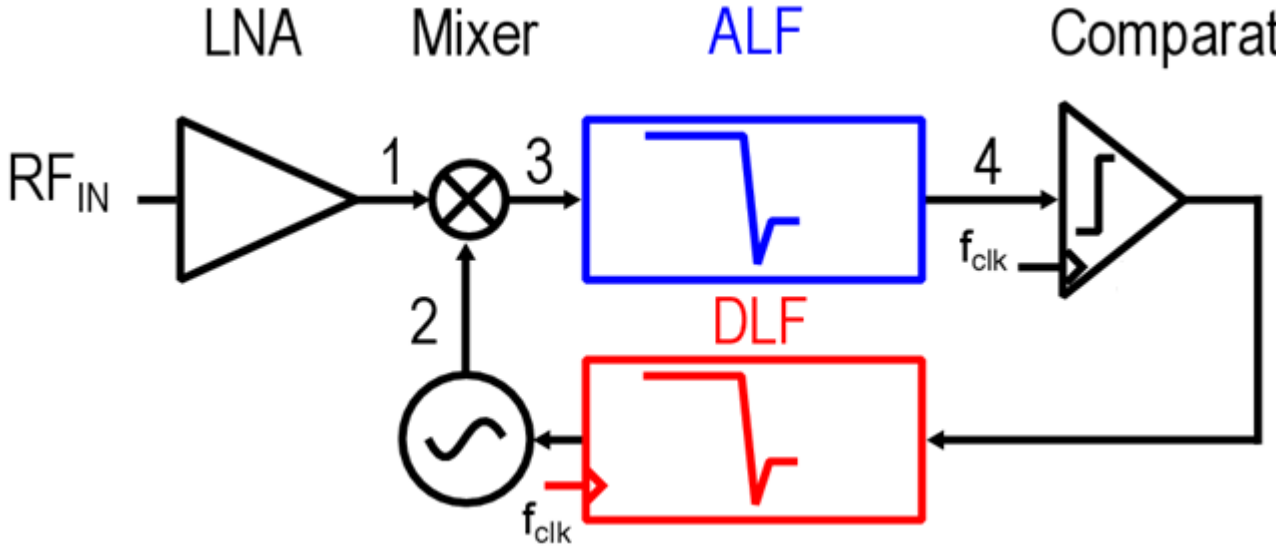
Proposed: Hybrid Loop Filter



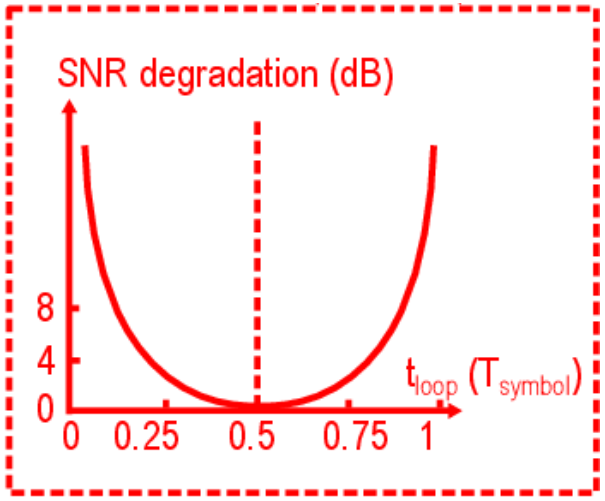
Error source	Solution
P_{RES} Interference residue	Analog loop filter (ALF)
$P_{int,bb}$ Due to DCO slide-lobe energy	*Digital loop filter (DLF)*



Design trade-offs in hybrid loop filter

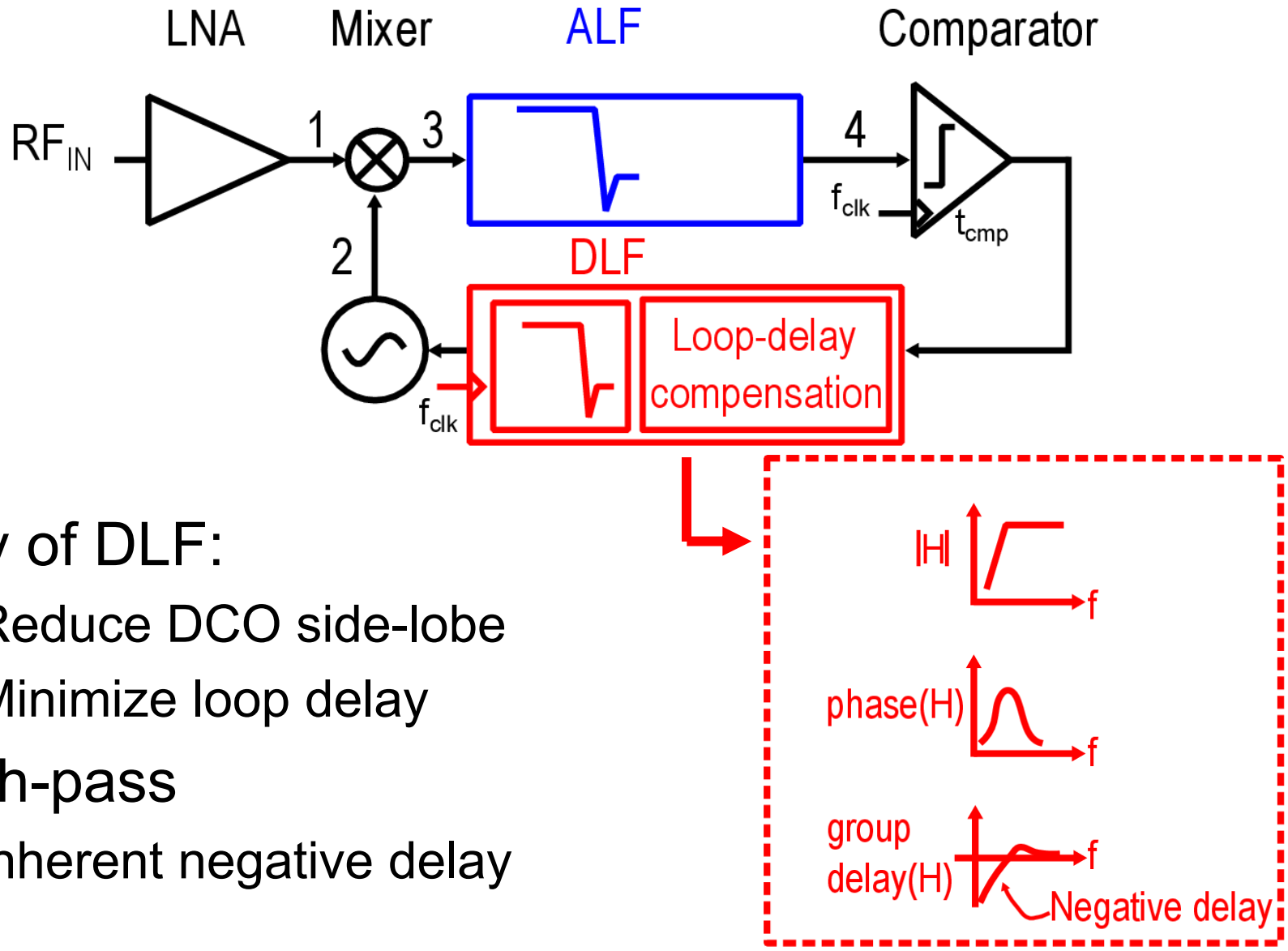


	T_{symbol}
1Mbps	0.5µs
2Mbps	0.25µs



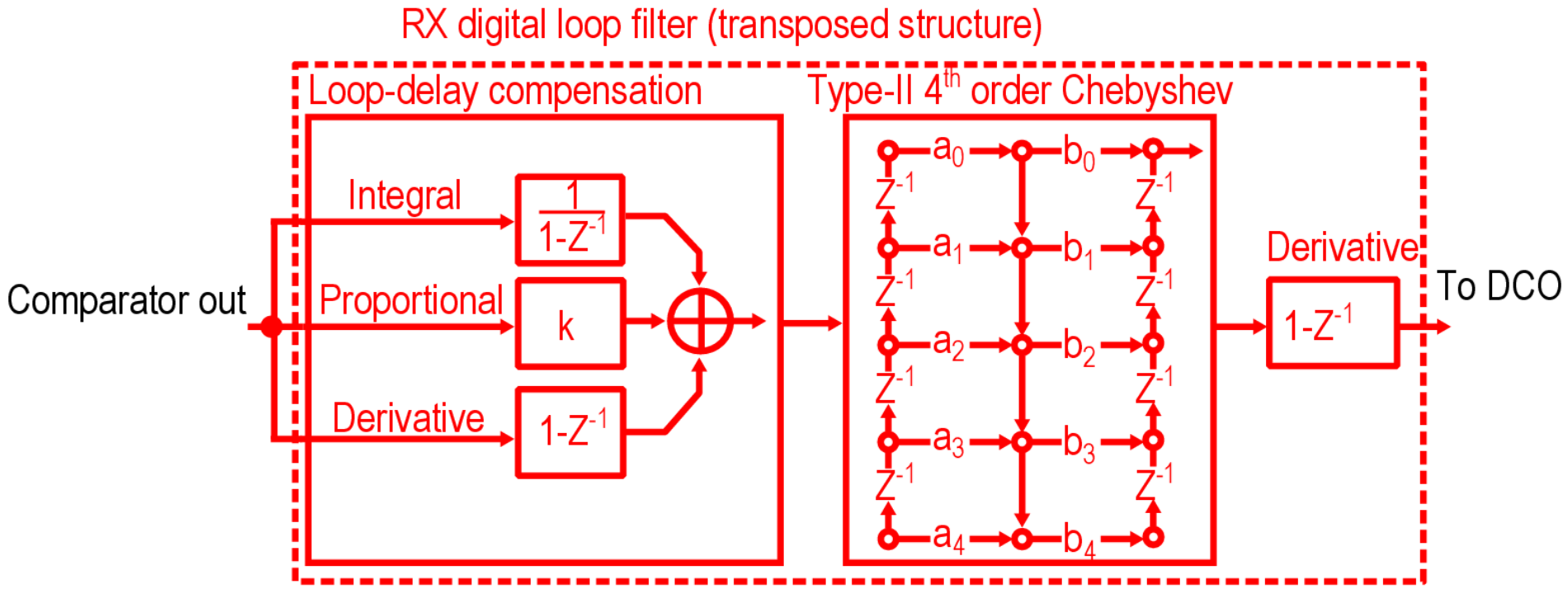
Analog loop filter (ALF)	Attenuation ↑	P_{RES} ☺	Delay ☹
Digital loop filter (DLF)	Attenuation ↑	P_{SLE} ☺	Delay ☹

DLF with Loop delay compensation



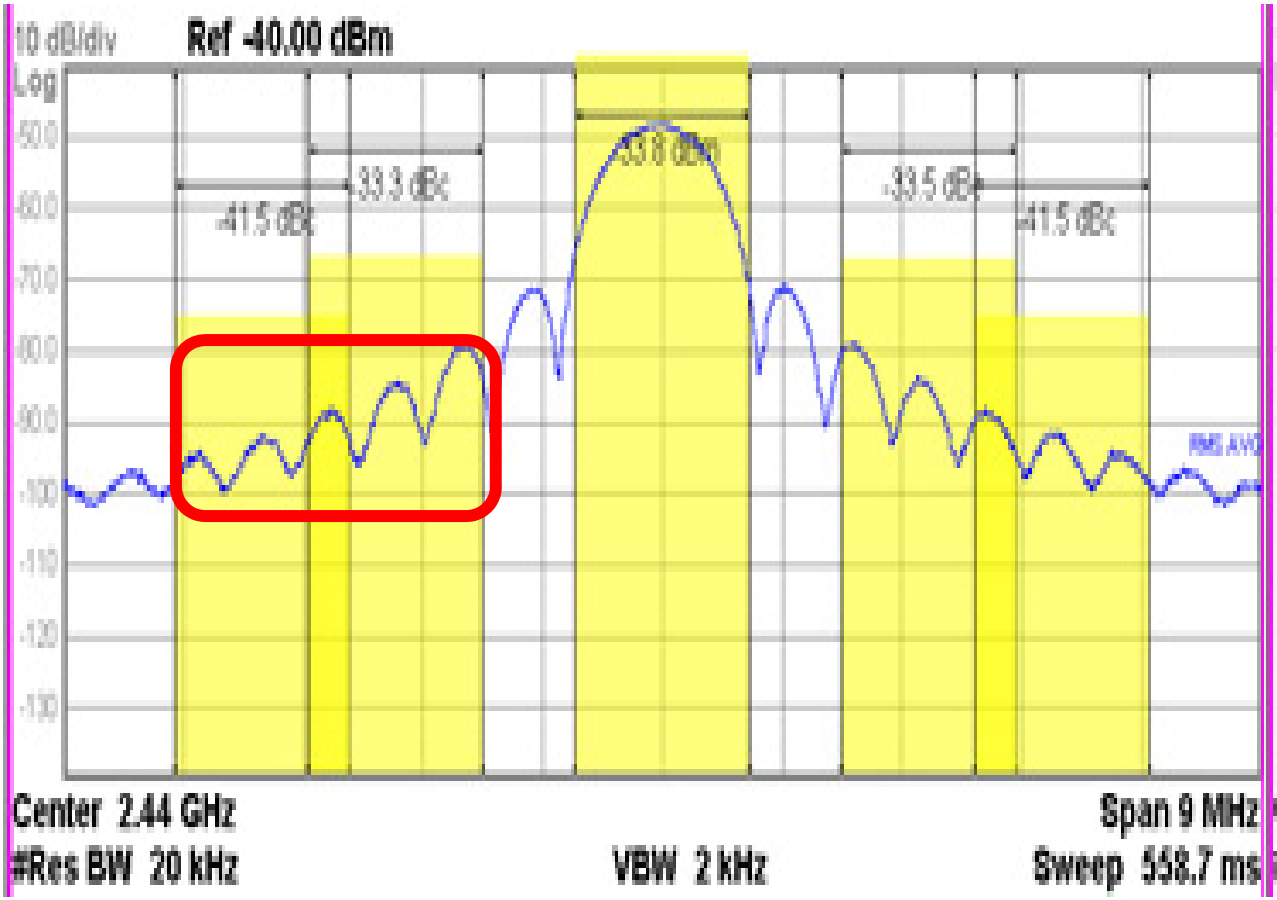
- Key of DLF:
  - Reduce DCO side-lobe
  - Minimize loop delay
- High-pass
  - Inherent negative delay

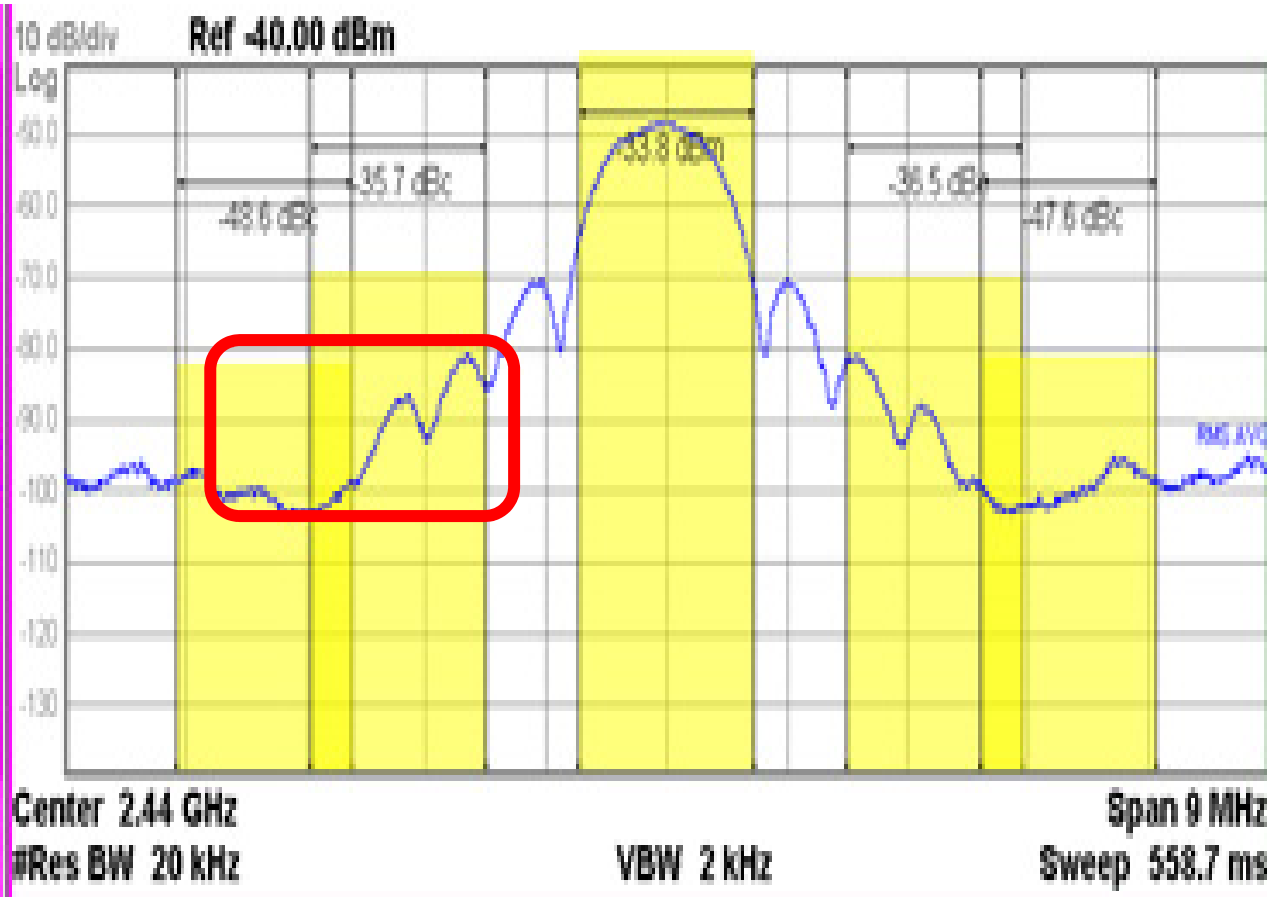
Digital Loop Filter (DLF) architecture



- Side-lobe filter: 4th order Chebyshev notch filter
- PID (Proportional, Integral, Derivative) compensates delay

Measured DCO side-lobe energy (SLE)





DLF=OFF

SLE_2nd=-33.5dBc

SLE_3rd= -41.5dBc

-3dB →

-6dB →

DLF=ON

SLE_2nd=-36.5dBc

SLE_3rd= -47.6dBc

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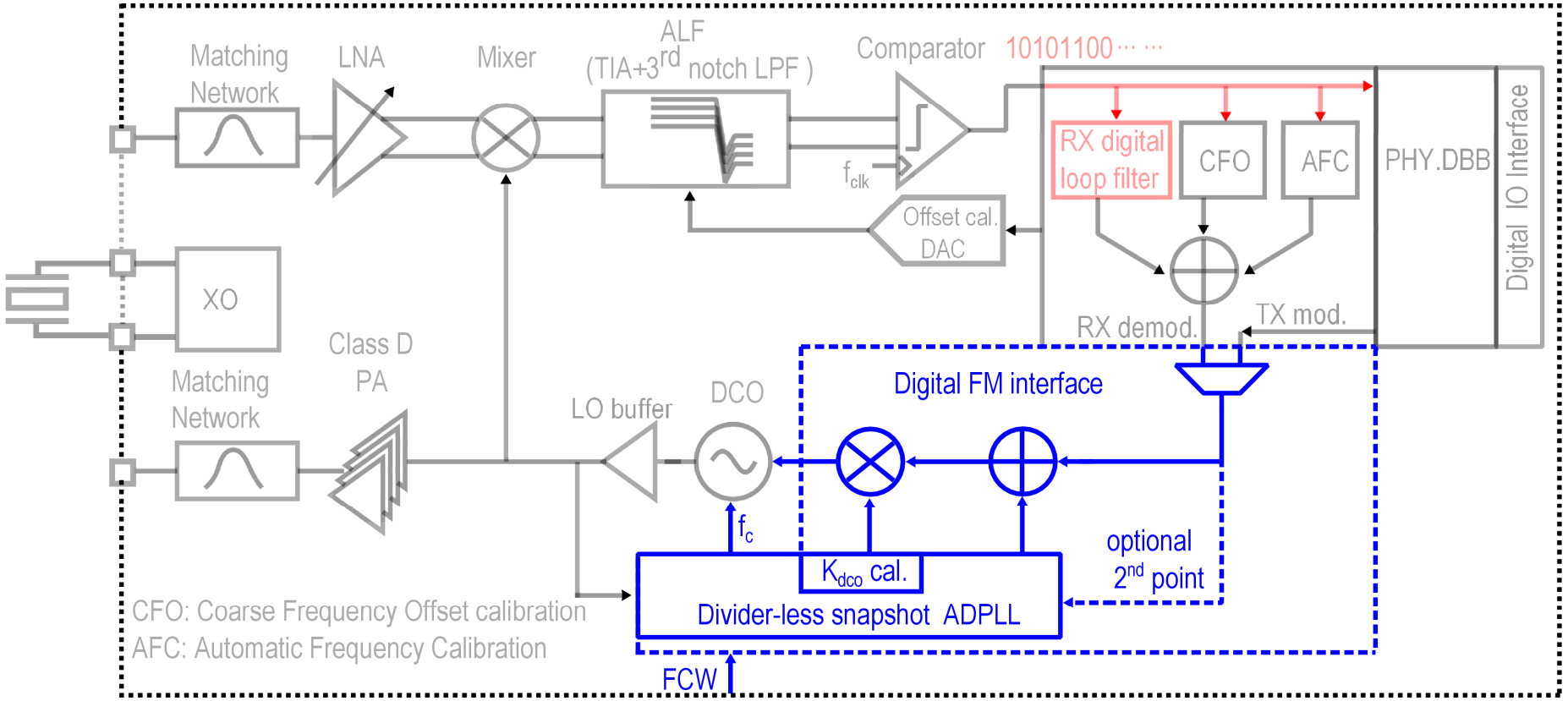
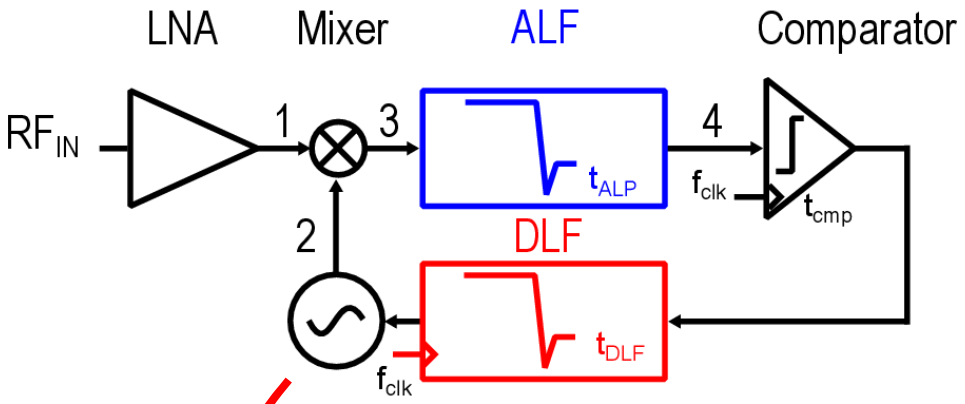
ADPLL-based FM interface

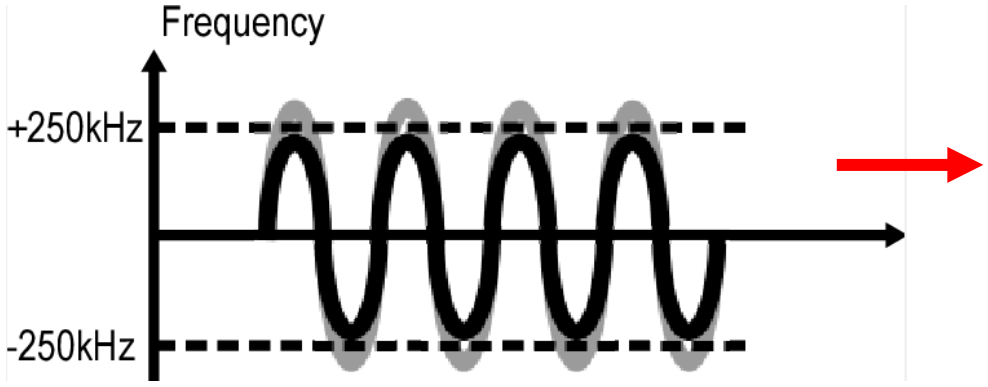


- Define initial frequency
- Enable the frequency deviation (k_{dco}) calibration
- Hardware/calibration reuse between RX/TX

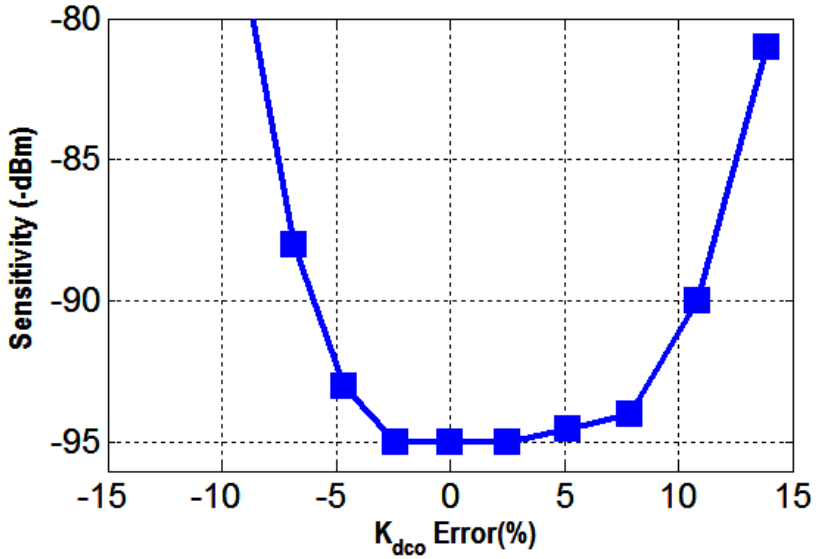
Frequency deviation (k_{dco}) calibration



- DCO gain (k_{dco}) suffers from PVT variations
- Can be calibrated thanks to the ADPLL



Impact on TX



Impact on RX

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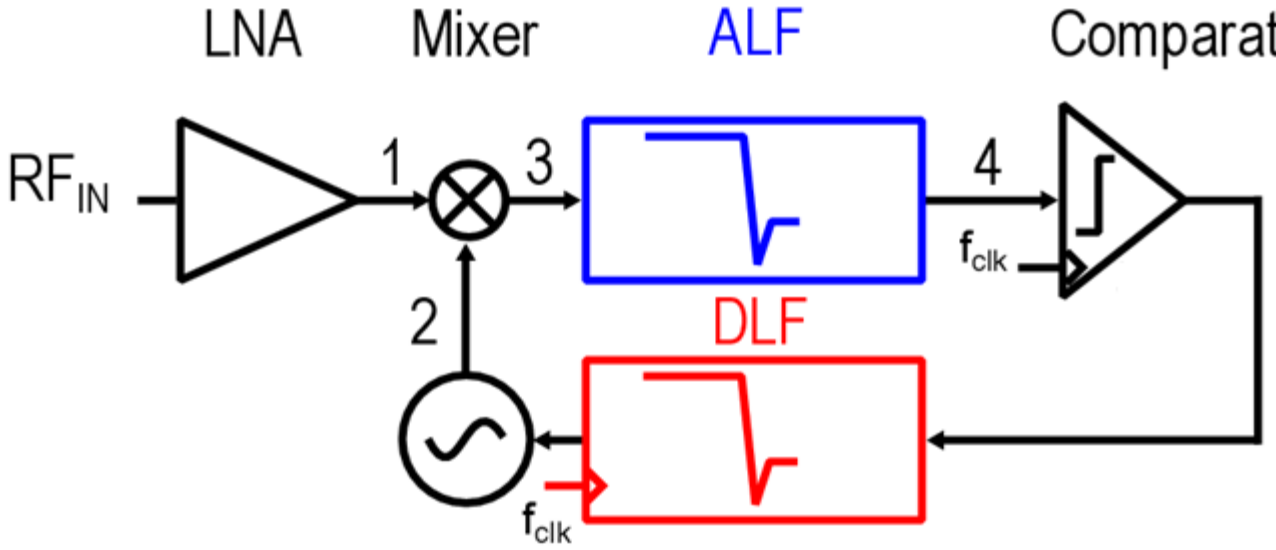
Digital-assisted automatic calibrations



Problem	Solution
DC offset error	DC offset calibration
Coarse frequency offset error	Coarse frequency offset calibration (CFO)
Dynamic frequency error	Automatic frequency calibration (AFC)

Outline

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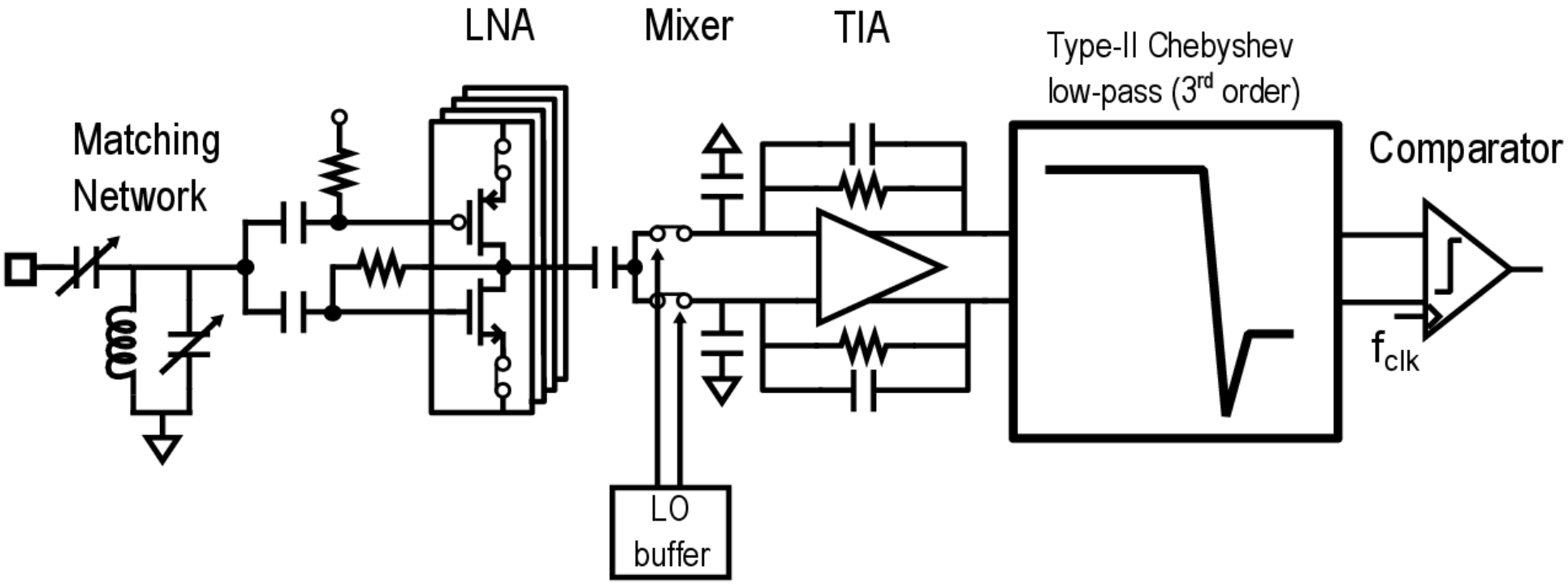
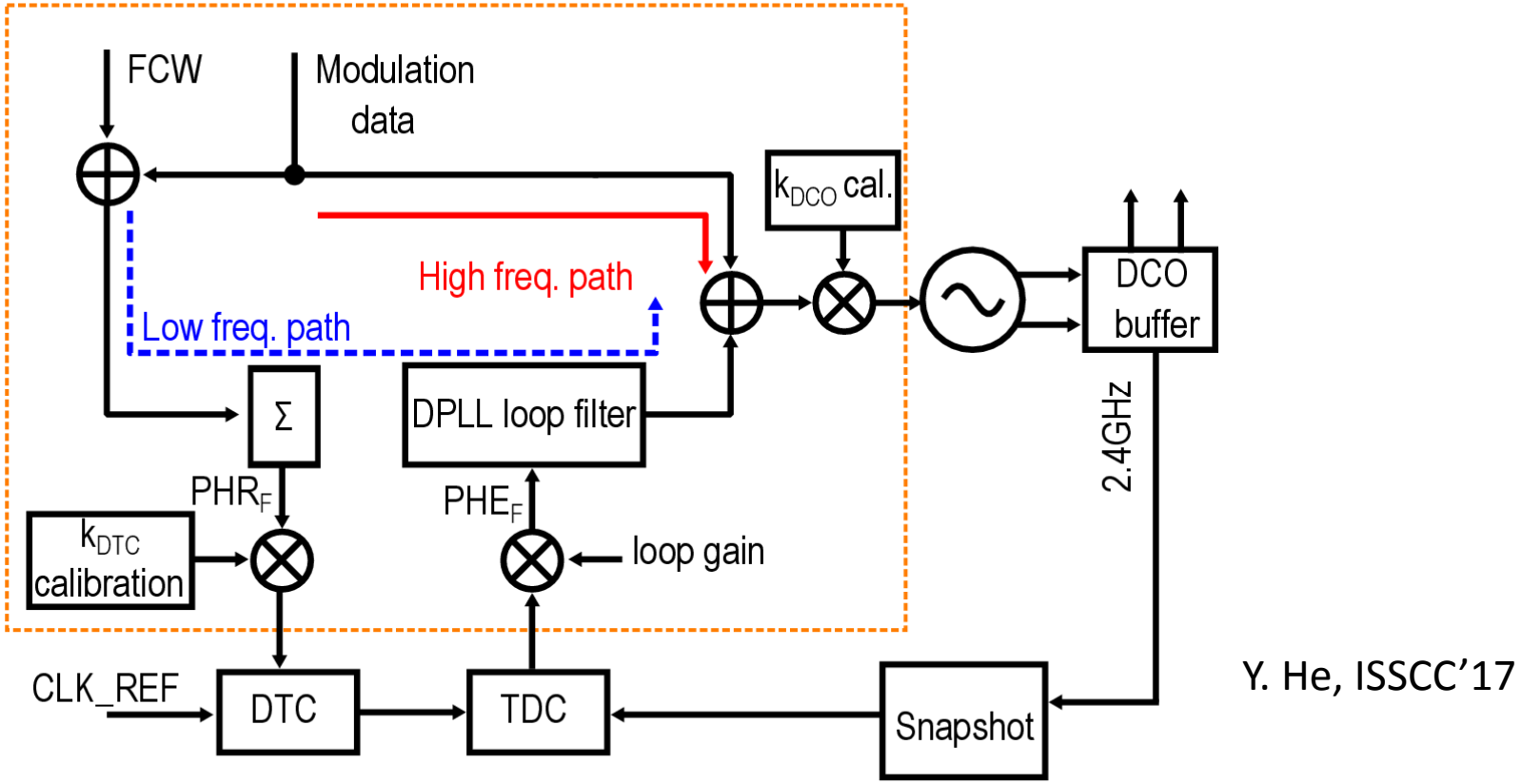
RX architecture



- To ensure 0.8V operation
  - Inverter-based LNTA to maximize gain with low-power
  - Passive mixer with low-pass at TIA input forms bandpass profile to enhance Out-Of-Band (OOB) blocker performance
  - 1b ADC

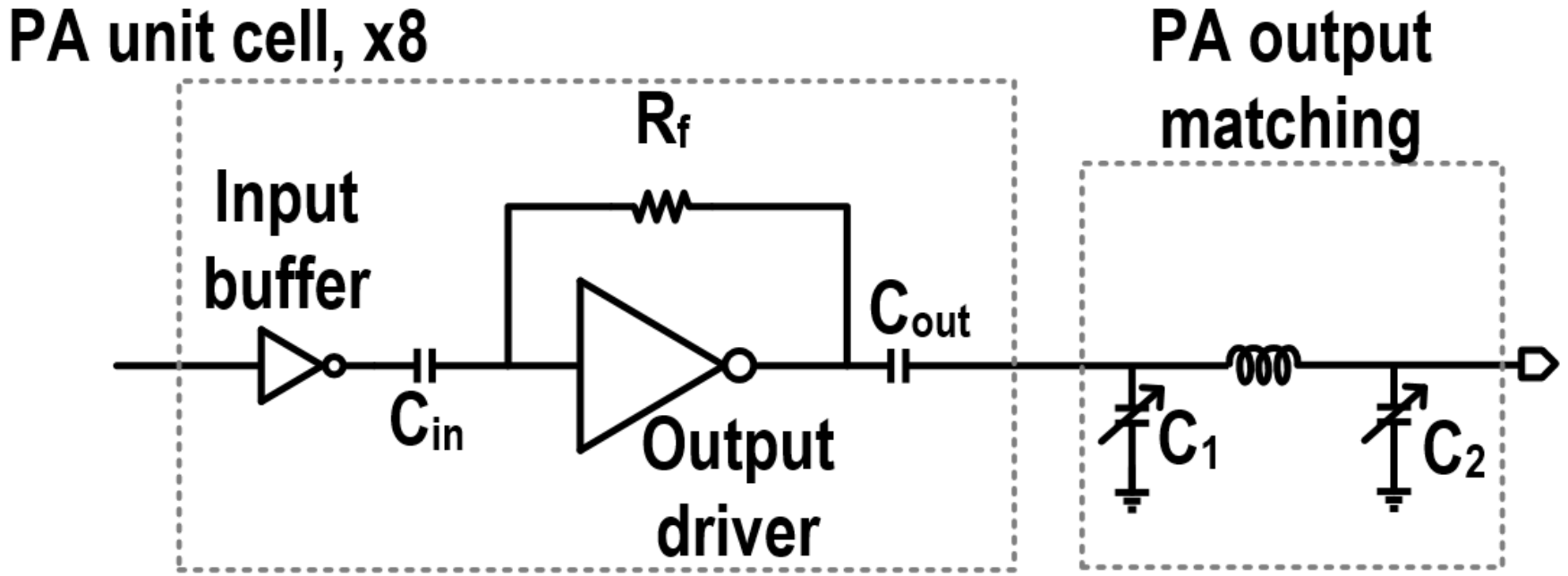
Digital TX: ADPLL



Y. He, ISSCC'17

- Divide-less snapshot 415μW DPLL
- Low supply voltage and small area
- Enables the K_{dco} calibration reuse between RX/TX

Digital TX: Class-D PA



A. Ba, RFIC'14

- Digitally reconfigurable output power
- Max. 1.8dBm output power with 30% efficiency
- On-chip matching

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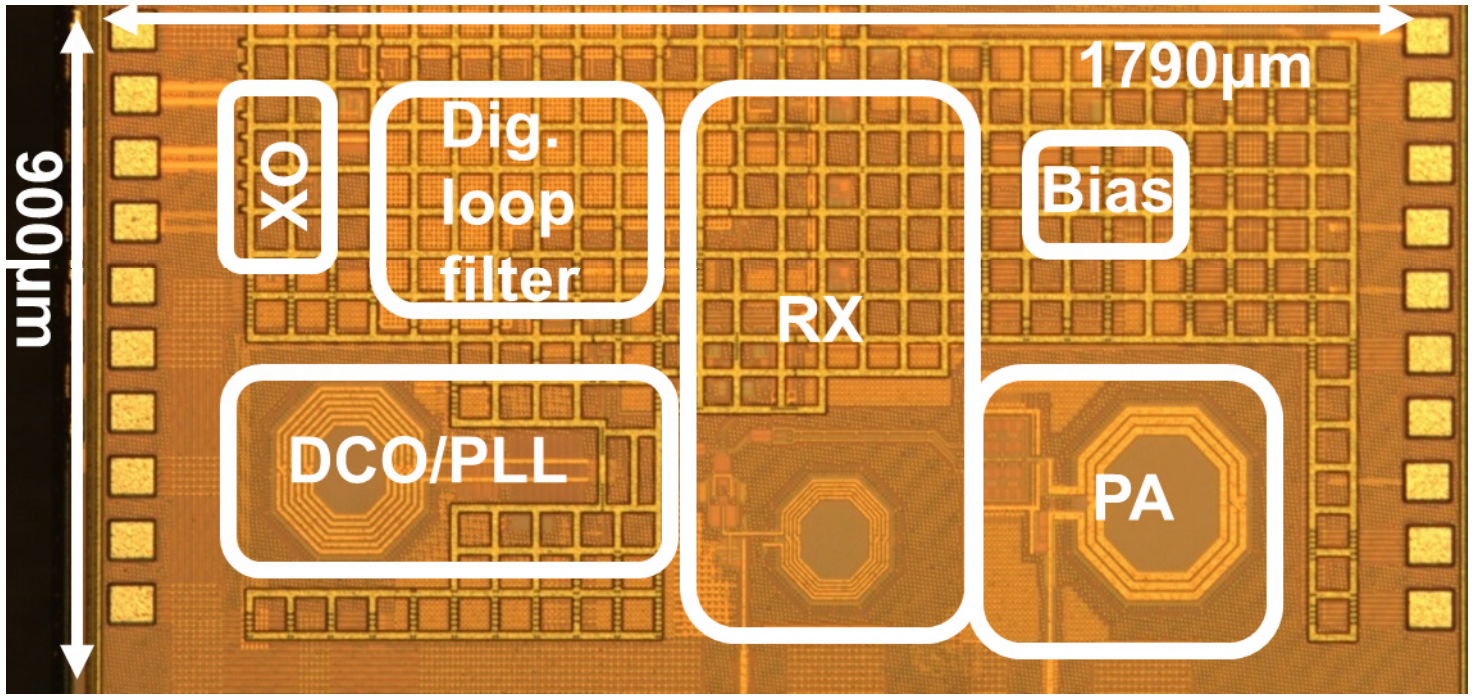
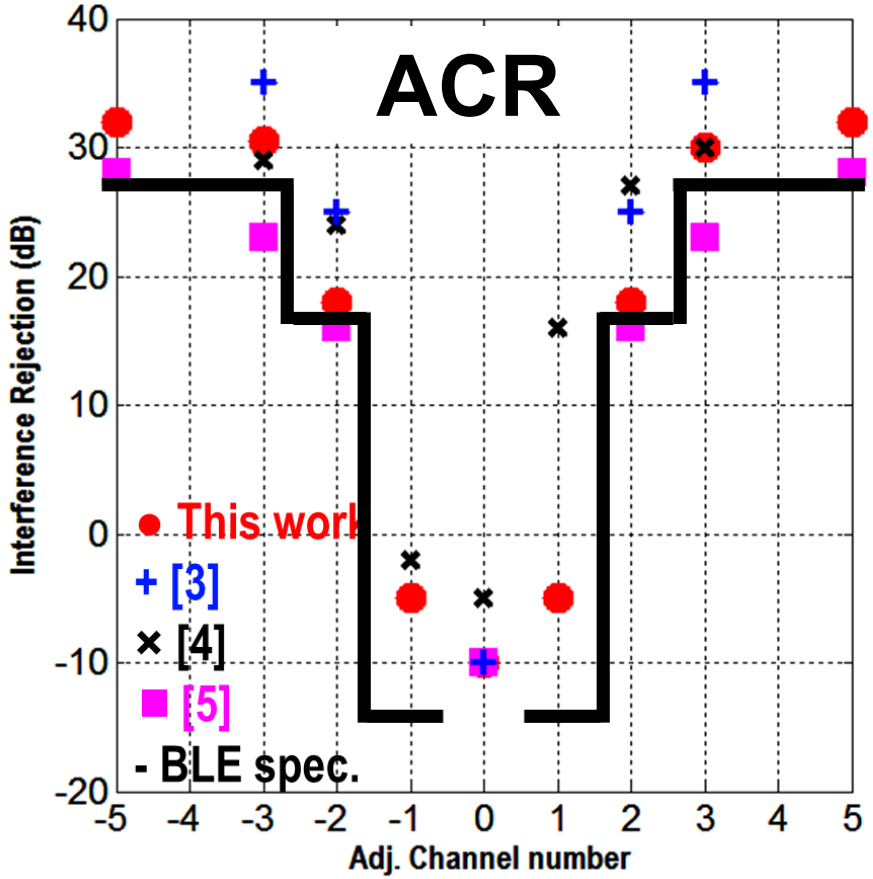
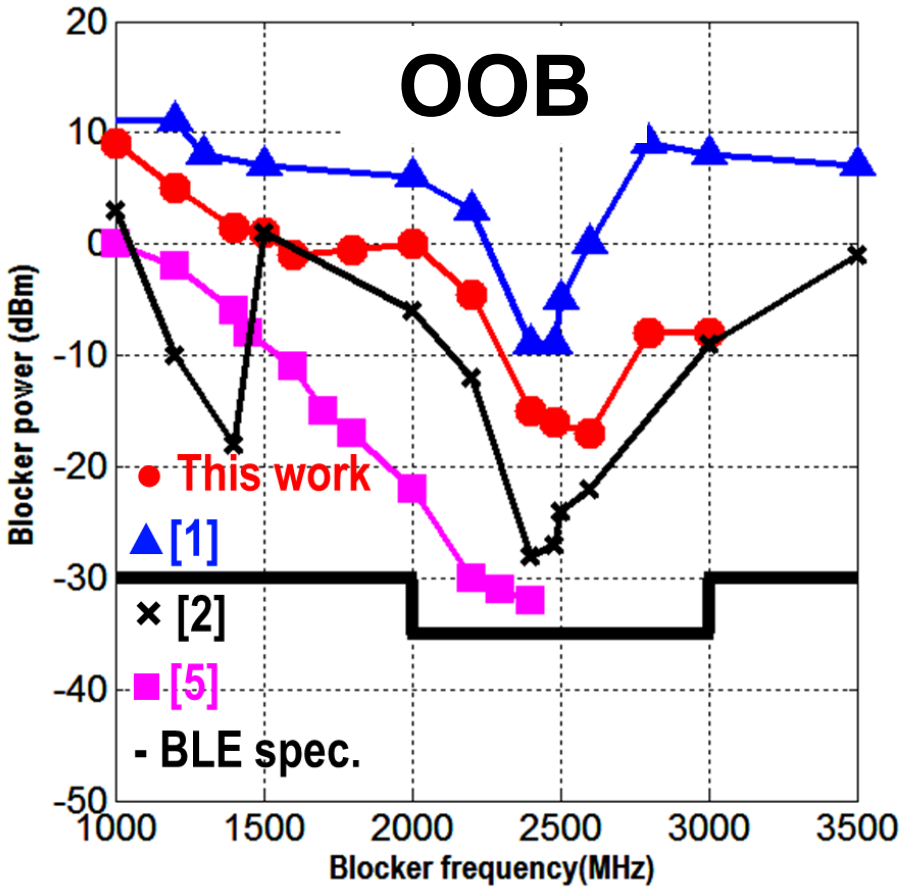
Die photo



- 40nm CMOS
- Small core area (including on-chip matching): 0.8mm^2
  - 3 on-chip inductors
- All circuits measured at 0.8V supply

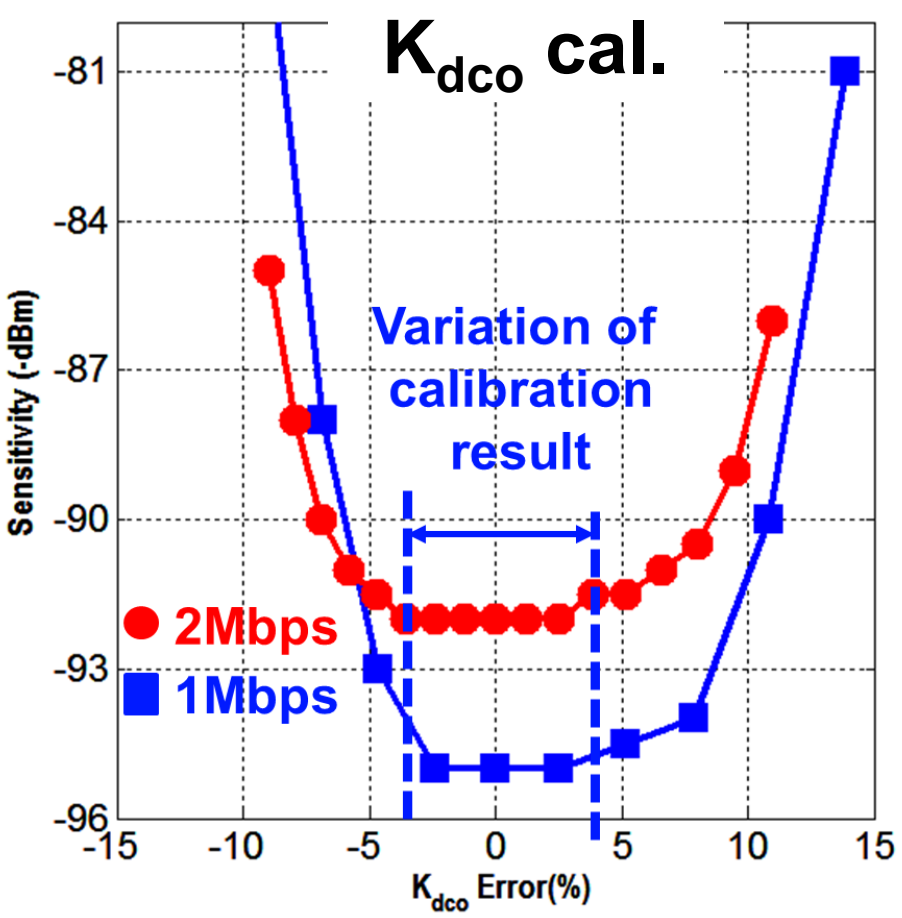
Blocker performance (ACR, OOB)

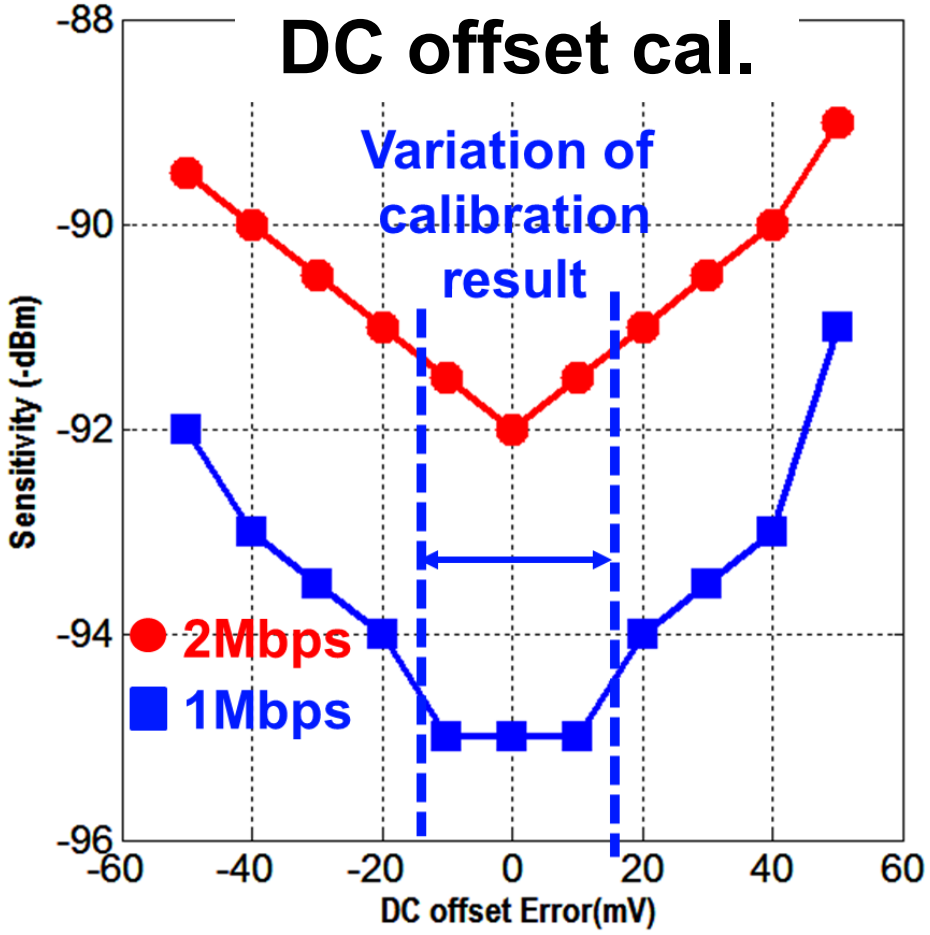




- With -67dBm GFSK desired input signal
- 2~7dB ACR improvement compared to prior-art
- On-par OOB performance without image issue

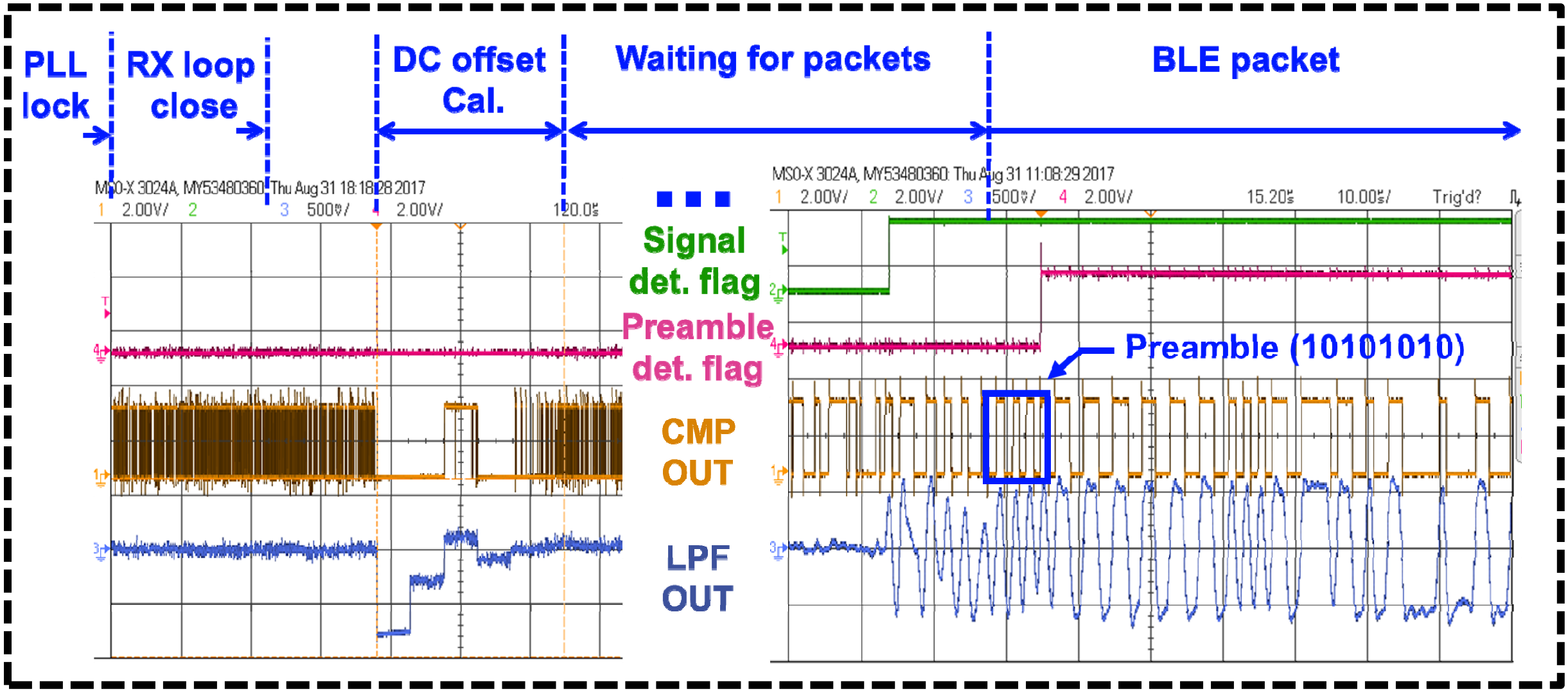
Sensitivity performance





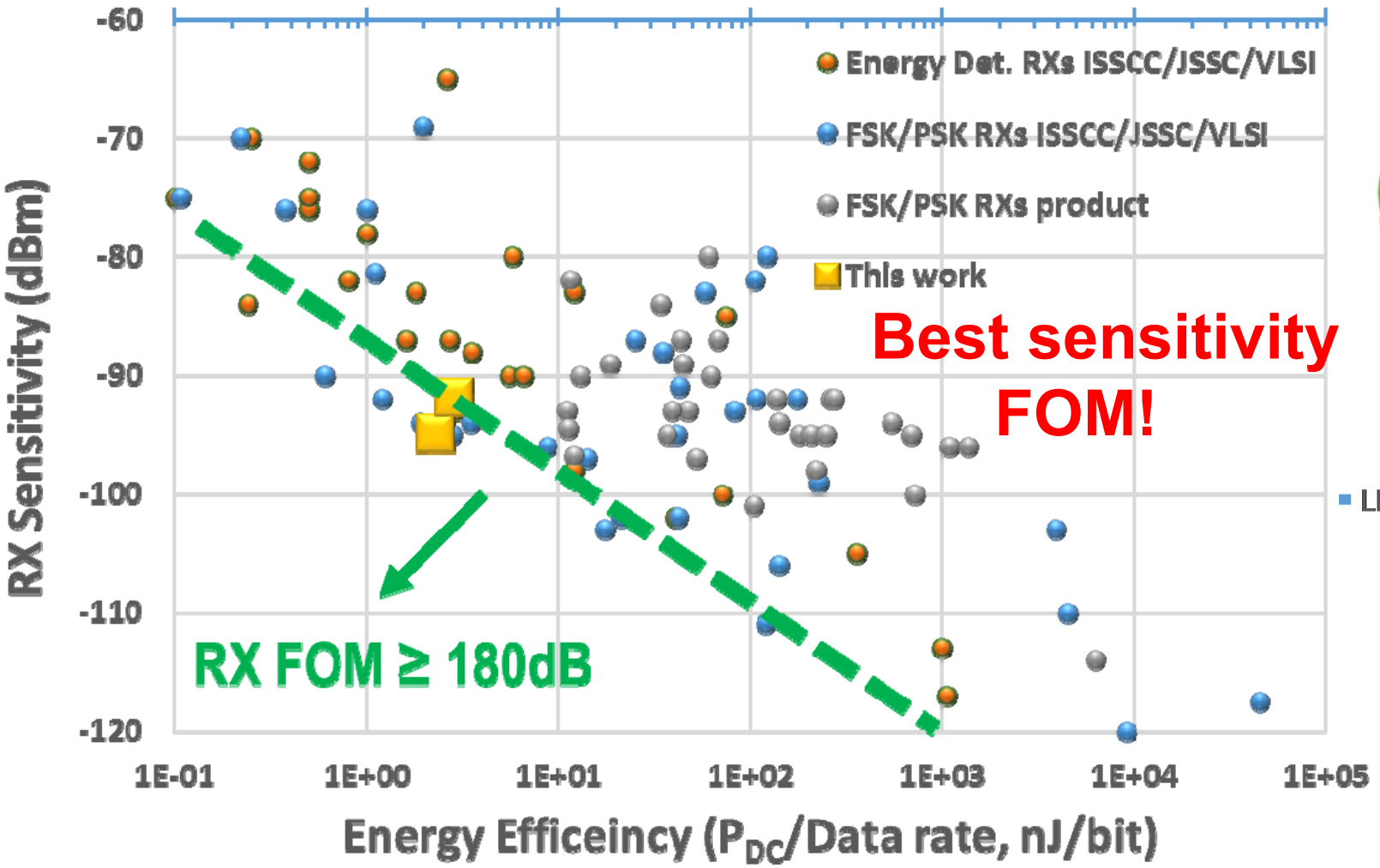
- -95dBm/-92dBm at 1Mbps/2Mbps
- Automatic calibration ensures the performance

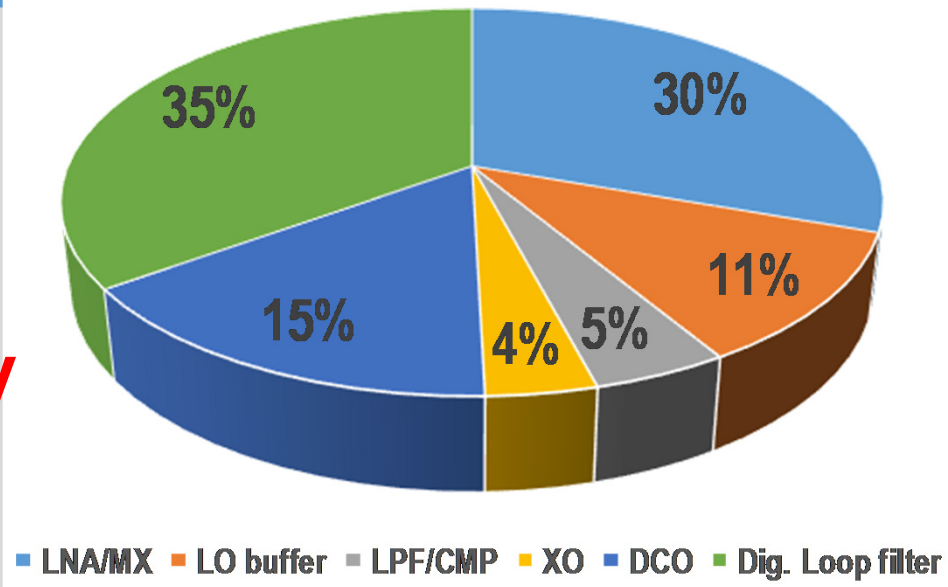
Packet-based operation in real time



- DBB enabled packet-based operation

Power consumption





RX power (max. gain): 2.3mW@0.8V

FOM = -sensitivity-10×log(P_{DC}/Data rate)

Performance summary

	This work		[1]J. Prummel ISSCC'15	[2] T. Sano ISSCC'15	[3] X. Wang ESSCIRC'16		F.W. Kuo JSSC'17
Standards	BLE	BT5	BLE	BLE	BLE	BT5	BLE
Data rate	1Mbps	2Mbps	1Mbps	1Mbps	1Mbps	2Mbps	1Mbps
Supply voltage	0.8V		0.9V~3.3V	1.1V	1V		1V
Technology	40nm		55nm	40nm	40nm		28nm
Integration level	RX/TX/partial DBB		SoC	RX/TX	SoC		RX
RX architecture	Zero-IF phase-tracking		Low-IF	Sliding-IF Cartesian	Sliding-IF Cartesian		High-IF Discrete-Time
Image rejection.	No image		No image	70dB	35dB		42dB
RX ACR (2^{nd} /3^{rd})	18/30dB	18/29.5dB	-	32/-dB	>17/27dB		-
RX worst-case OOB	-17dBm		-9dBm	-28dBm	-		-25dBm
TX max. Pout	1.8dBm		2.3dBm	0dBm	1dBm		3dBm
TX Freq. Error	2%	1.4%	-		6%		2.67%
Radio area	0.8mm^2		2.9mm^2	1.1mm^2	1.6mm^2		1.9mm^2
RX sensitivity	-95dBm*	-92dBm*	-94.5	-94.5#	-93#	-85#	-95#
RX FOM$_{SEN}$**	181.4dB	180.4dB	174dB	172dB	179dB	170dB	180.6dB
Power cons.							
RX font-end	2.3mW	2.9mW	11.2mW	6.3mW	5.6mW		2.75mW
TX front-end	6.1mW	6.1mW	10.1mW	7.7mW	9.4mW		3.7mW##
RX DBB	0.74mW	1.1mW		-	0.6mW		

* Based on BER,
# Based on PER,
** RX FOM=-sensitivity-10×log(P_{DC}/Data rate),
at 0dBm output power

Conclusions

- A BT5/BLE radio in 40nm CMOS is presented using
  - Single-channel phase-tracking RX with a hybrid loop filter
  - ADPLL-based FM interface
  - Digital TX

- Featuring
  - **BT5**-compliant
  - Lowest supply voltage **0.8V**
  - Best RX Figure-Of-Merit (FOM) **181.4dB**
  - Small core area **0.8mm^2**

A 0.45V Sub-mW All-Digital PLL in 16nm FinFET for Bluetooth Low Energy (BLE) Modulation and Instantaneous Channel Hopping using 32.768kHz Reference

Min-Shueh Yuan[1], Chao-Chieh Li[1], Chia-Chun Liao[1], Yu-Tso Lin[1], Chih-Hsien Chang[1], Robert Bogdan Staszewski[2]

[1]TSMC, Hsinchu, Taiwan

[2]University College Dublin, Dublin 4, Ireland

Outline

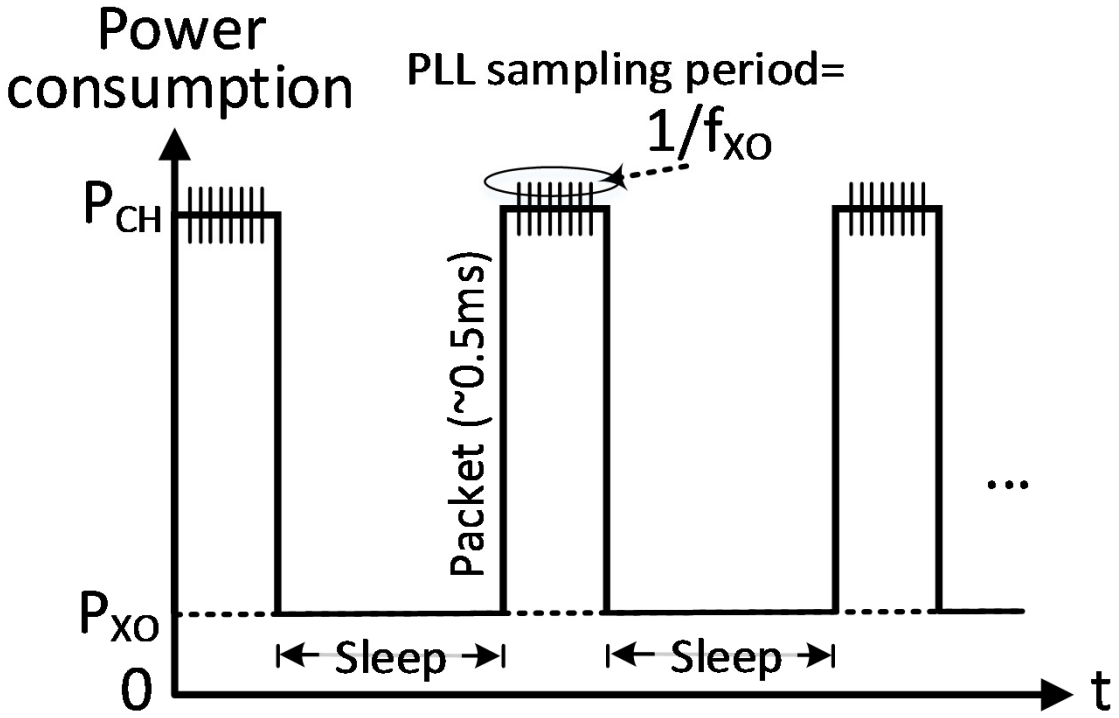
- Motivation
  - Focus on frequency synthesizer for Bluetooth Low Energy (BLE) in the most advanced CMOS (i.e., FinFET)
  - Elimination of crystal oscillator (for further energy reduction)
  - 0.45V operation (for energy harvesting)
  - <1mW power consumption
- Proposed Structure
  - All-digital PLL (ADPLL) with combined 2-point modulation and channel hopping
- Measurement Results
- Conclusion

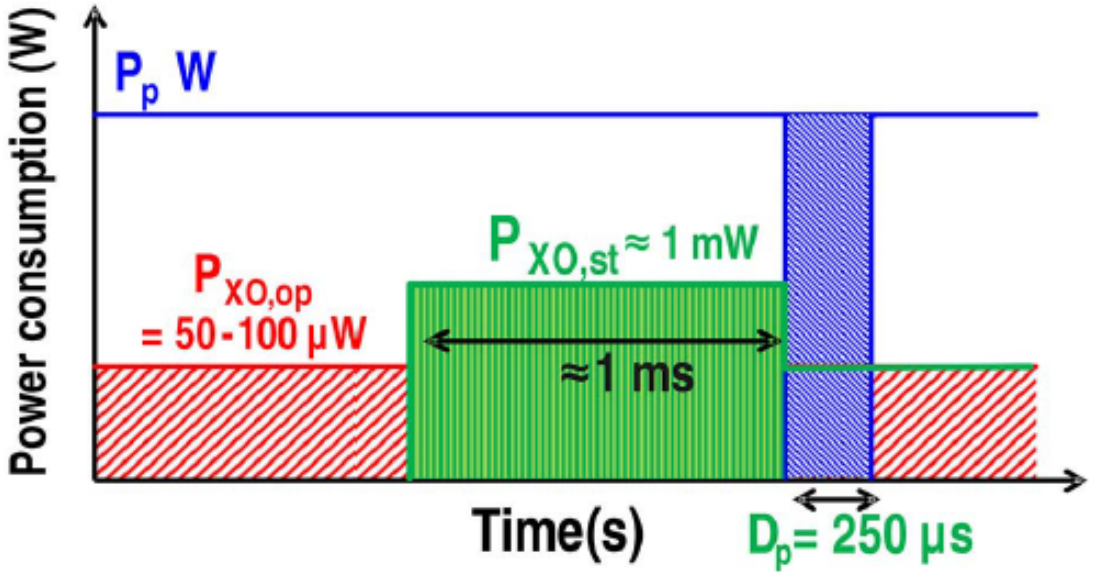
Current Paradigm

- Frequency reference: crystal oscillator (XO) of tens of MHz
- Wide PLL bandwidth of >100kHz to quickly settle DCO to a new channel and suppress low-frequency DCO phase noise
- ~1V supply voltage with high power consumption

Crystal Oscillator at Low Duty-cycle

- Burns ~100uW during continuous operation
- Hence, must shut down periodically
- Restarting is energy intensive: ~1mW over ~1ms





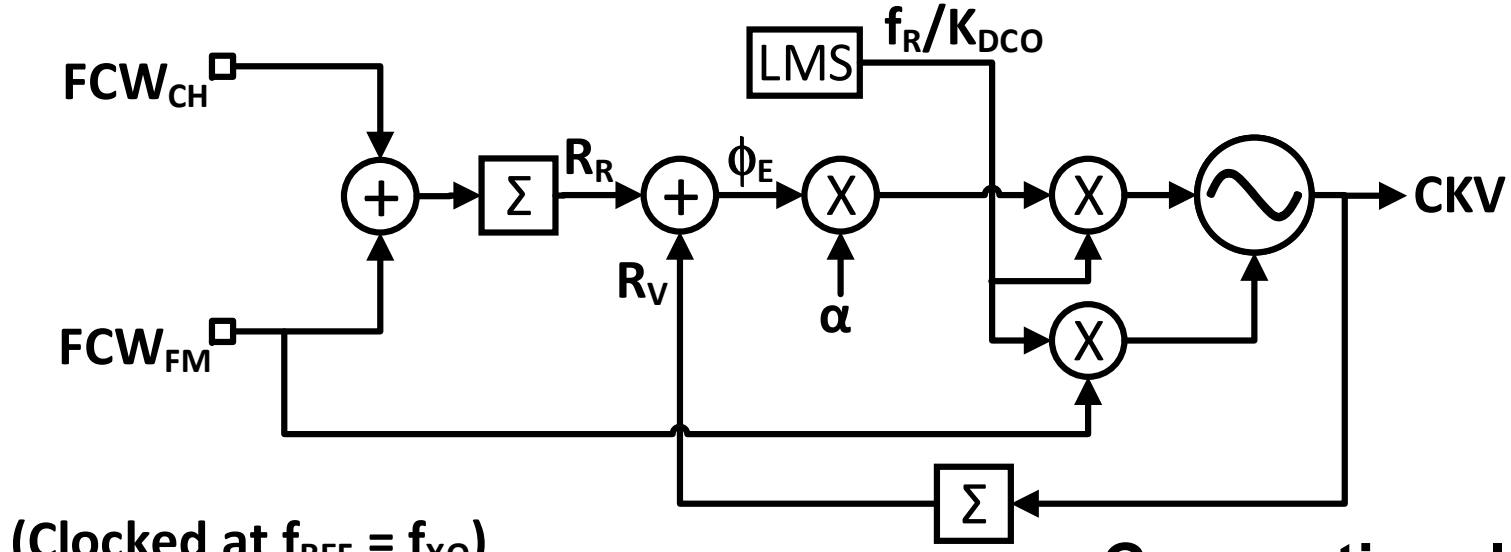
[5] R. Thirunarayanan, et al. IEEE TMTT

New Paradigm

- Eliminating XO by resorting to 32.768kHz real-time clock (RTC)
  - NEVER shut down
  - Ubiquitous in all IoT hosts for TX/RX scheduling
- But, 2 new challenges:
  - Slow settling due to ~1kHz PLL bandwidth
    - Comparable to entire BLE packet of ~0.5ms
  - Difficulty of precise frequency hopping and modulation

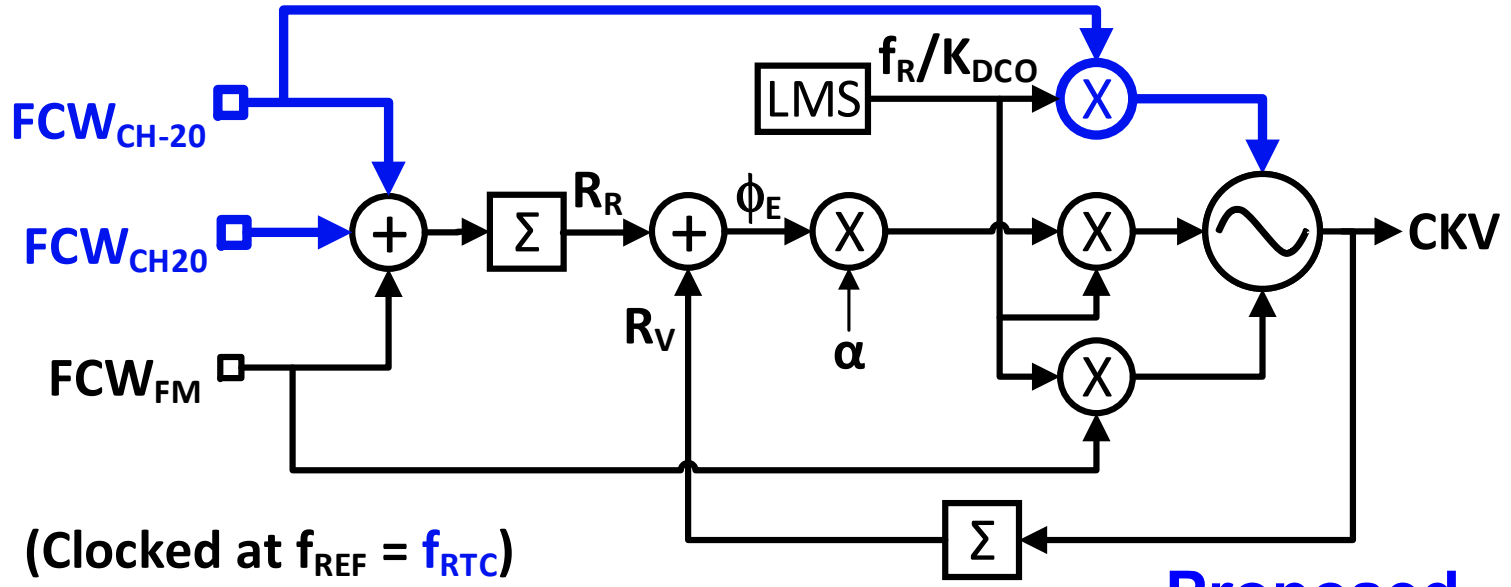
Proposed New Paradigm

- Replace conventional channel settling with band settling
- Close-loop locking on middle CH20 after power up and staying there
- Instantaneously hop the DCO resonance via a 2-point modulation



(Clocked at $f_{REF} = f_{XO}$)
(e.g., f_{XO} = 8...40MHz)

Conventional

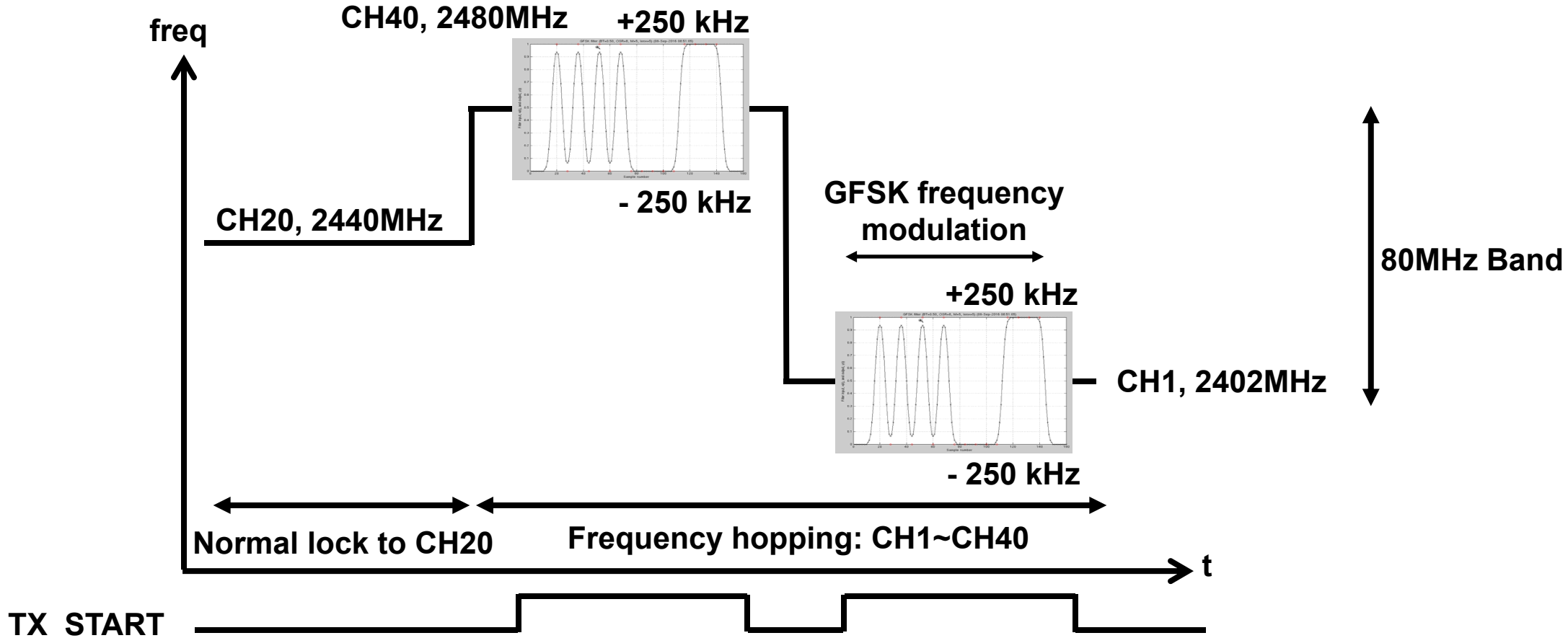


(Clocked at $f_{REF} = f_{RTC}$)
(e.g., f_{RTC} = 32.768kHz)

Proposed

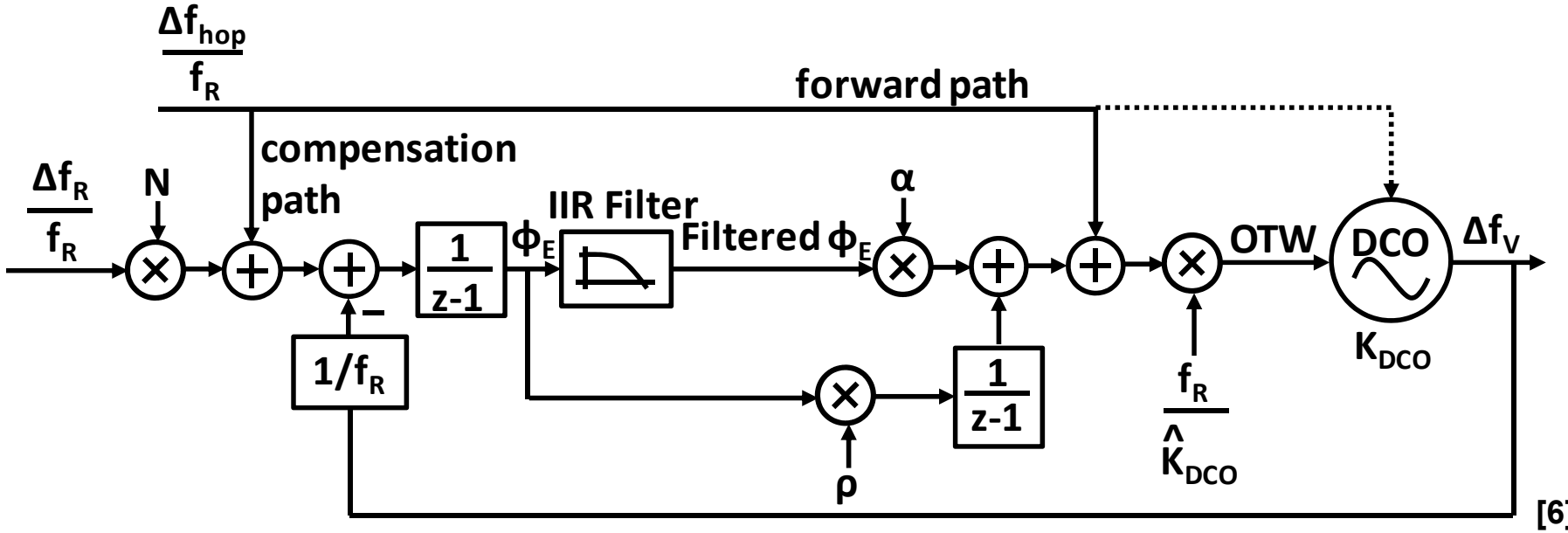
Acquisition of BLE Channel Hopping and Modulation

- 80MHz band span with 2MHz of channel separation
- Modulation index of 0.5



2-point Modulation (Background)

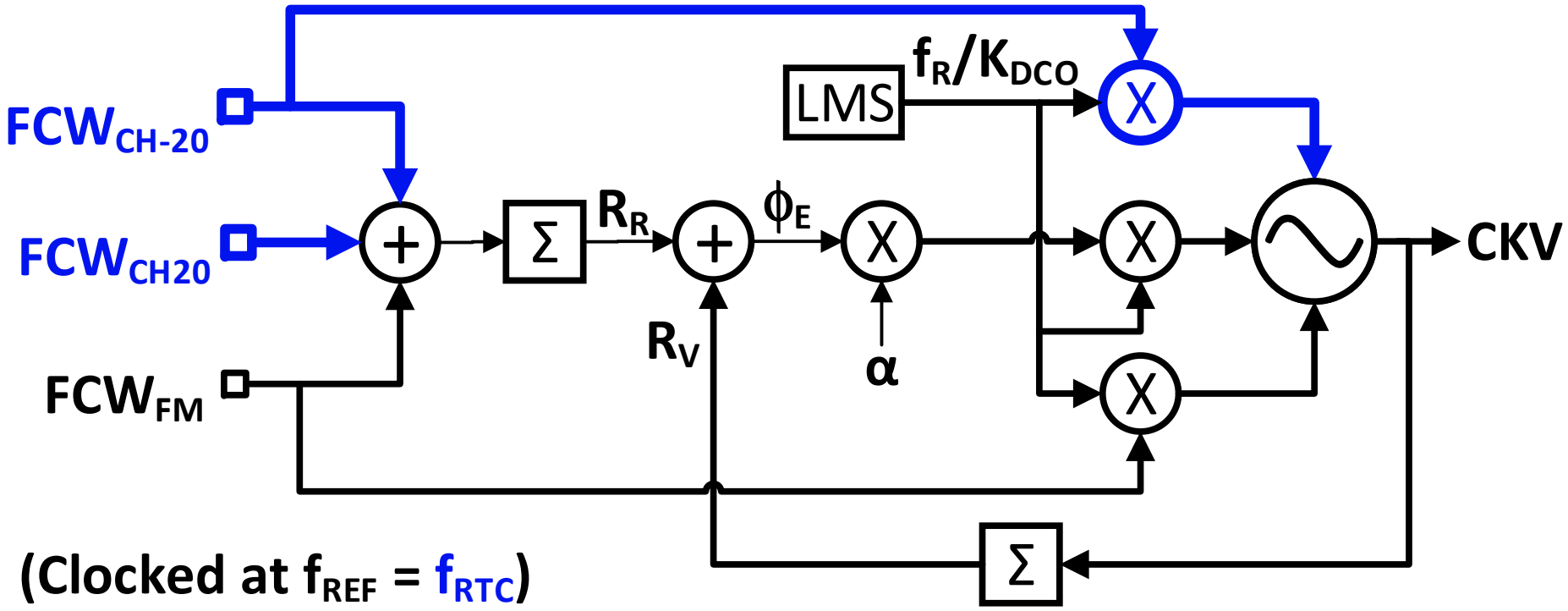
- Most popular technique for short-range wireless
- Modulating data fed directly into DCO
- Compensative data fed into phase detector
- Requires knowledge of DCO gain (K_{DCO})
  - K_{DCO} accuracy of few % needed for "ALL PASS" modulation



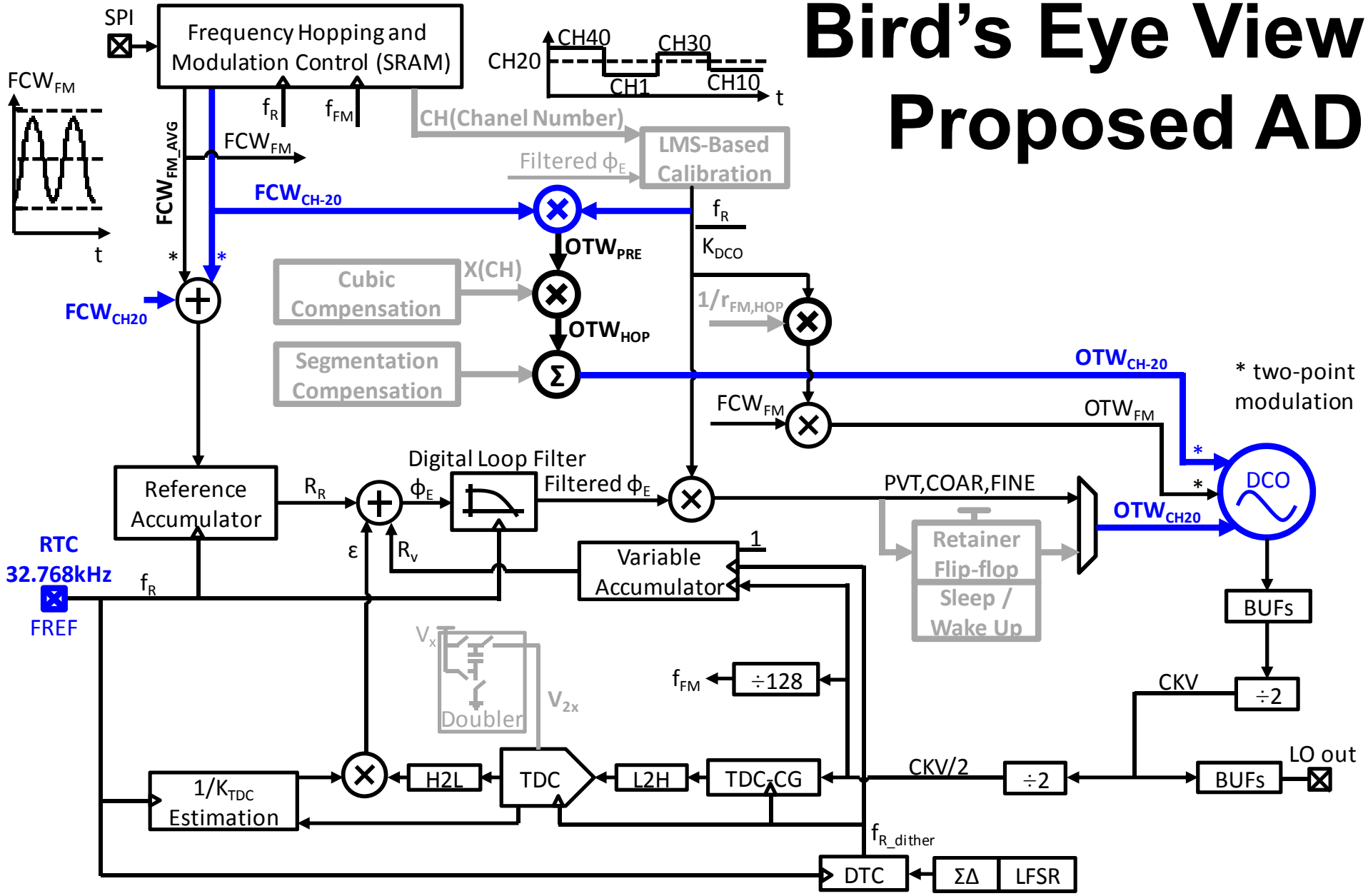
[6] R. B. Staszewski, et al. IEEE TCAS-II

How to Leverage 2-point Modulation for Instantaneous Channel Hopping ?

- Lock to middle CH20 (2440MHz) after power up and stay there
- Instantaneously hop DCO resonance via 2-point modulation

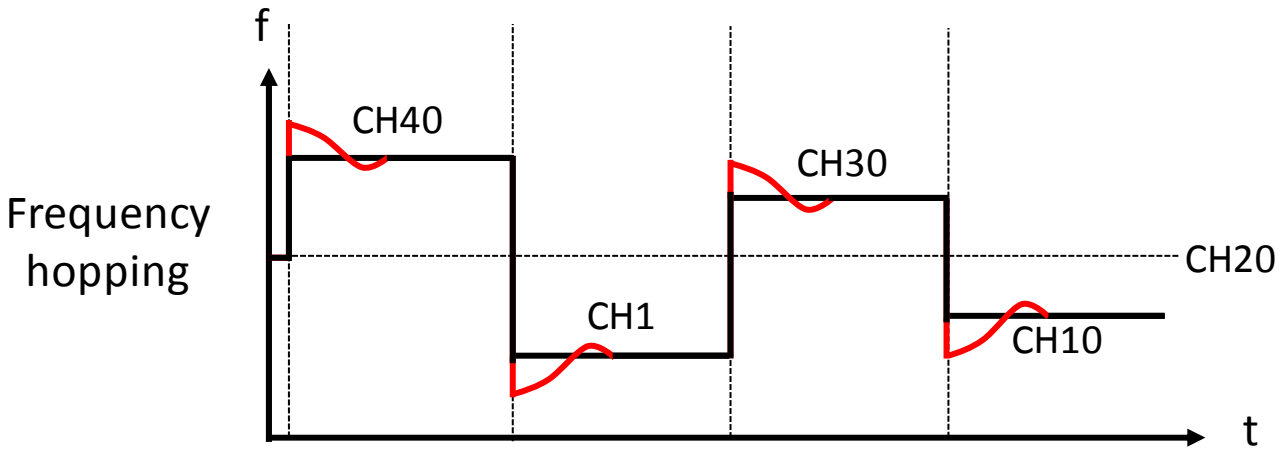


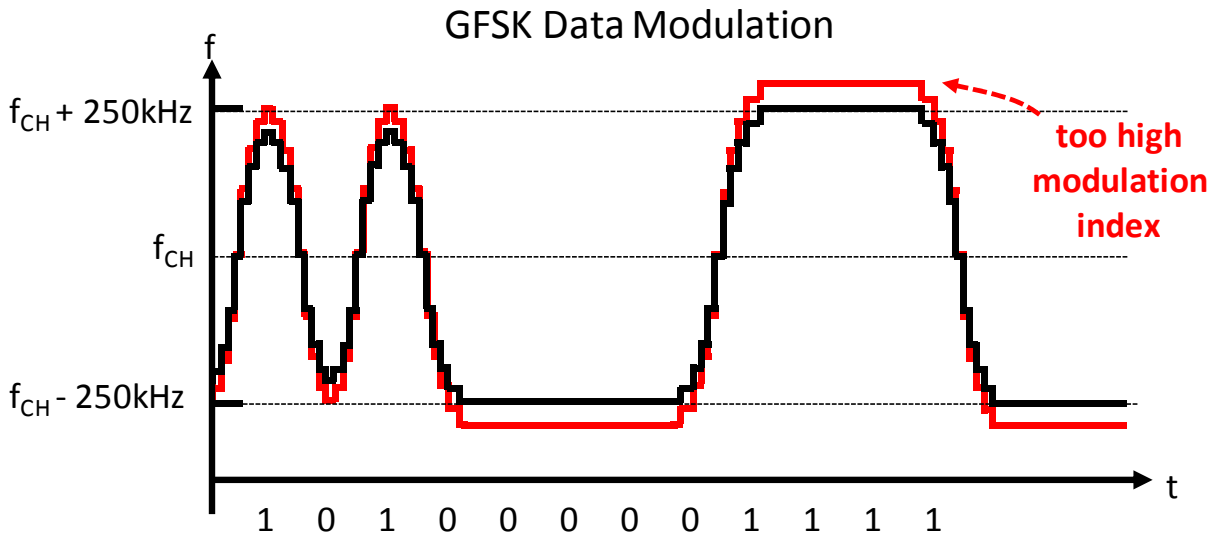
Bird's Eye View of the Proposed ADPLL



If f_R / K_{DCO} over Estimated…

- Longer hopping settling due to large hopping frequency error
- Modulation index too large



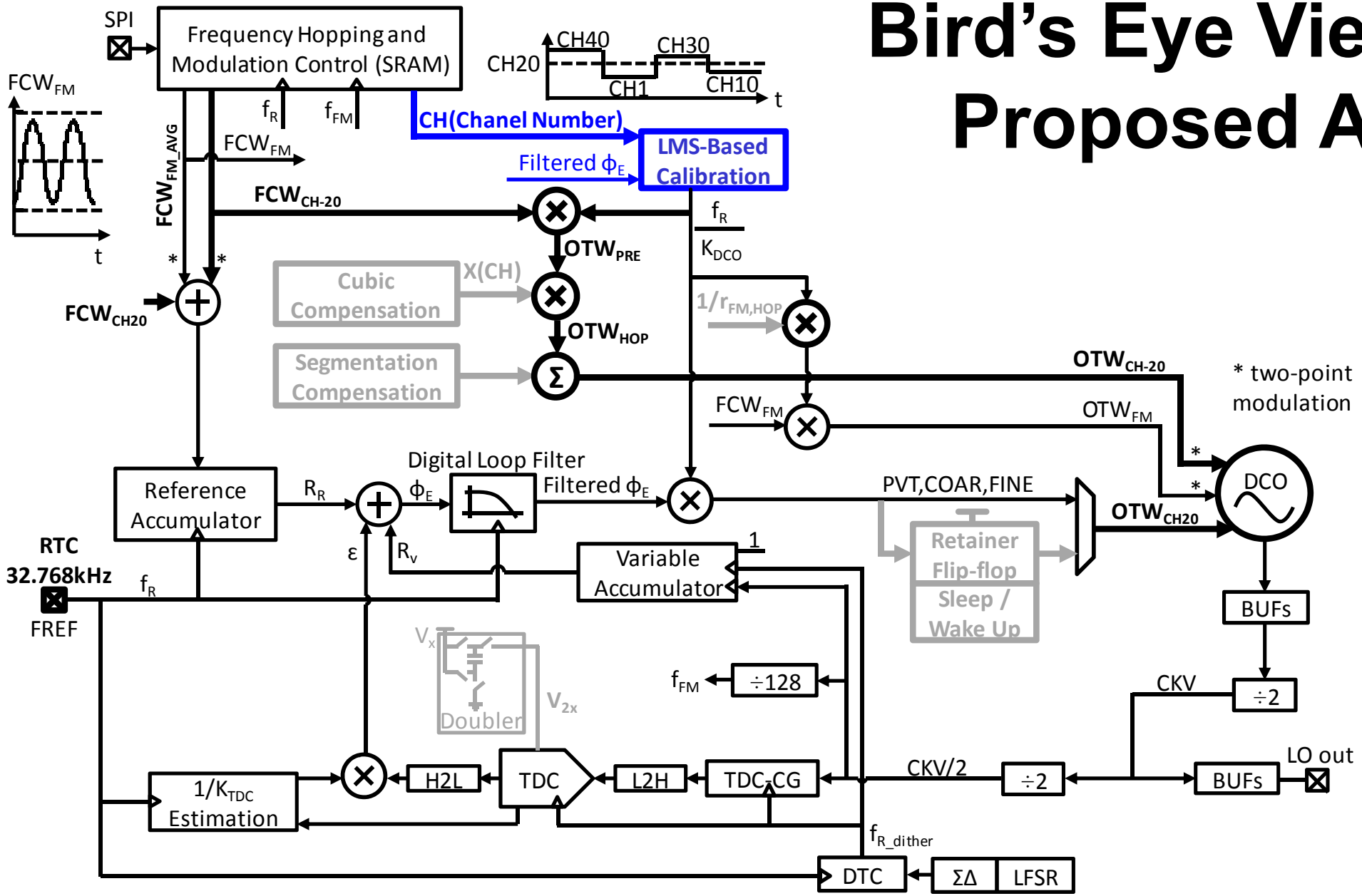


Frequency Accuracy of Hopping and Modulation

- Hopping frequency range from CH20
  - $(CH\text{-}20) * \Delta f_{CH}\ (=2MHz) = OTW_{CH\text{-}20} * K_{DCO}$
  - $OTW_{CH\text{-}20} = (CH\text{-}20) * \Delta f_{CH} / K_{DCO}$
    $= [(CH\text{-}20) * \Delta f_{CH} / f_R] * (f_R / K_{DCO}) = FCW_{CH\text{-}20} * (f_R / K_{DCO})$
- GFSK modulation range of $\pm$250kHz
  - $OTW_{FM} = FCW_{FM} * (f_R / K_{DCO})$

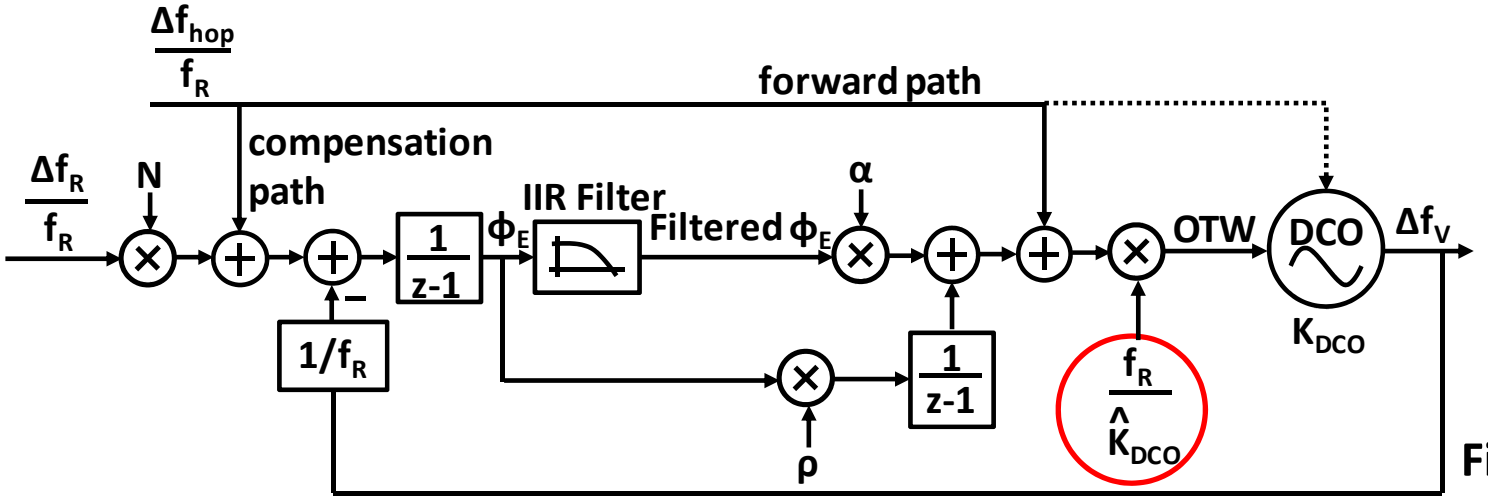
Precise K_{DCO} is a MUST
for precise hopping and modulation !
Currently, previous packet information thrown away.
Why not learn K_{DCO} from previous packets ?

Bird's Eye View of the Proposed ADPLL

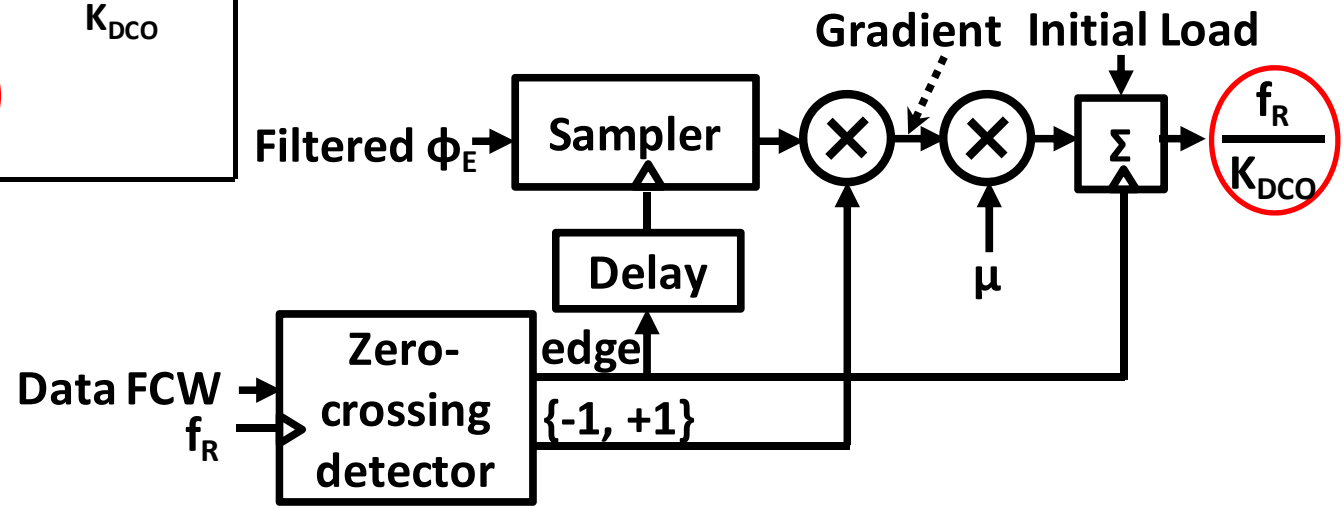


LMS-Based Calibration of DCO Gain (Background)

☐ Adapt K_{DCO} forcing filtered Φ_E to zero



[6] R. B. Staszewski, et al. IEEE TCAS-II

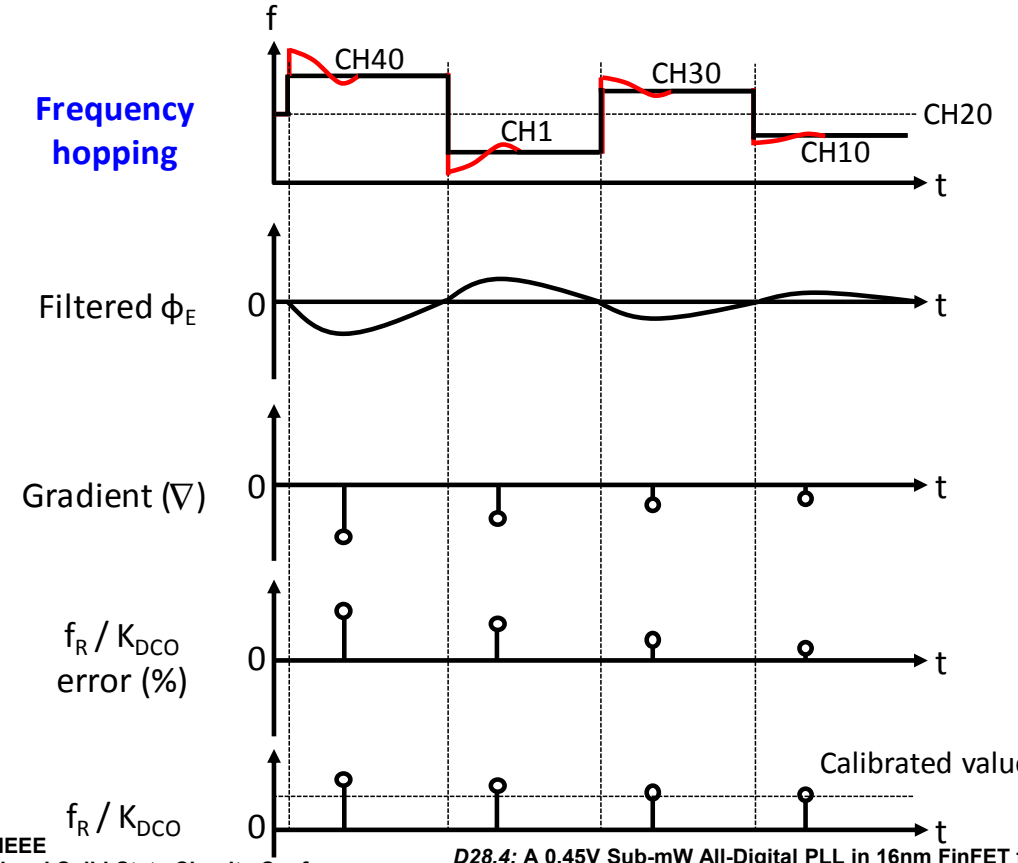


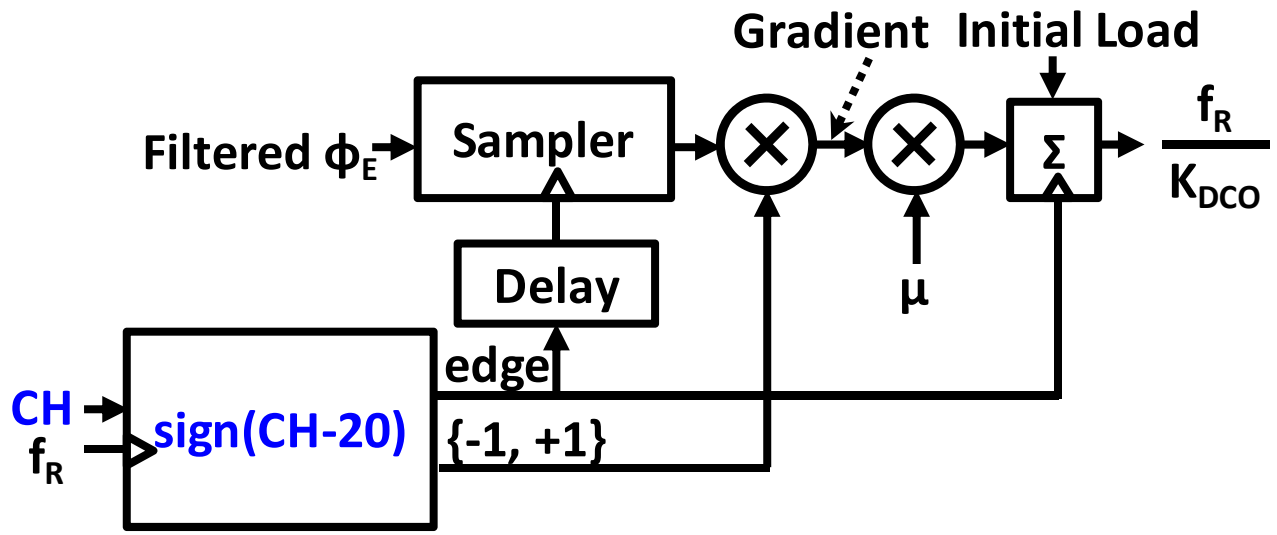
$$f_R / K_{DCO}[n] = f_R / K_{DCO}[n-1] + \mu * \nabla[n]$$

$$\nabla[n] = (\text{filtered } \phi_E[n]) * \text{sign(FCW)}$$

DCO Gain Calibration via Hopping Perturbation

- Leverage hopping perturbation as the modulating data applied to LMS loop
- Adapted K_{DCO} of hopping tuning bank on the middle CH20 of 2440MHz

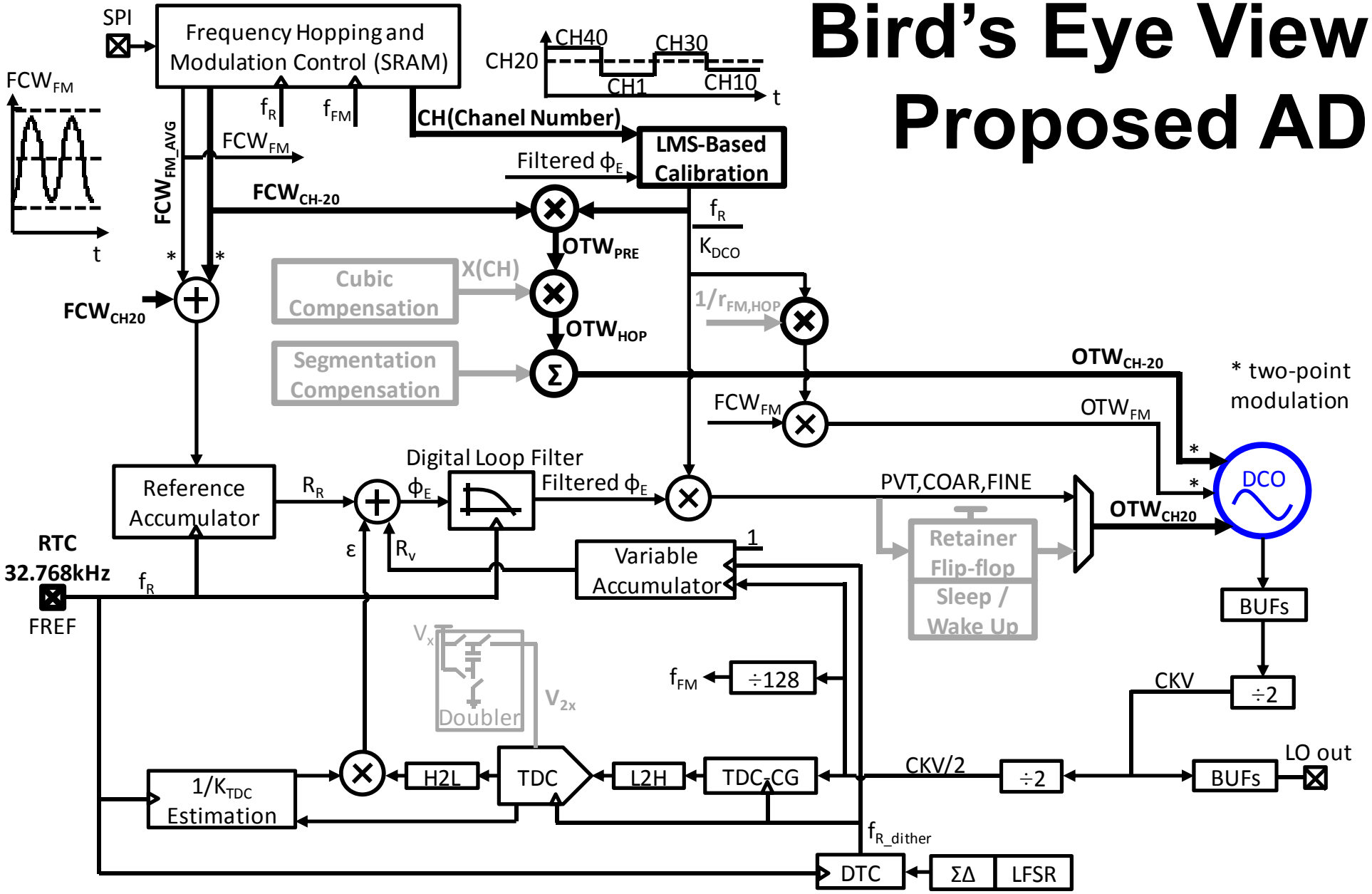




$$f_R / K_{DCO}[n] = f_R / K_{DCO}[n-1] + \mu * \nabla[n]$$

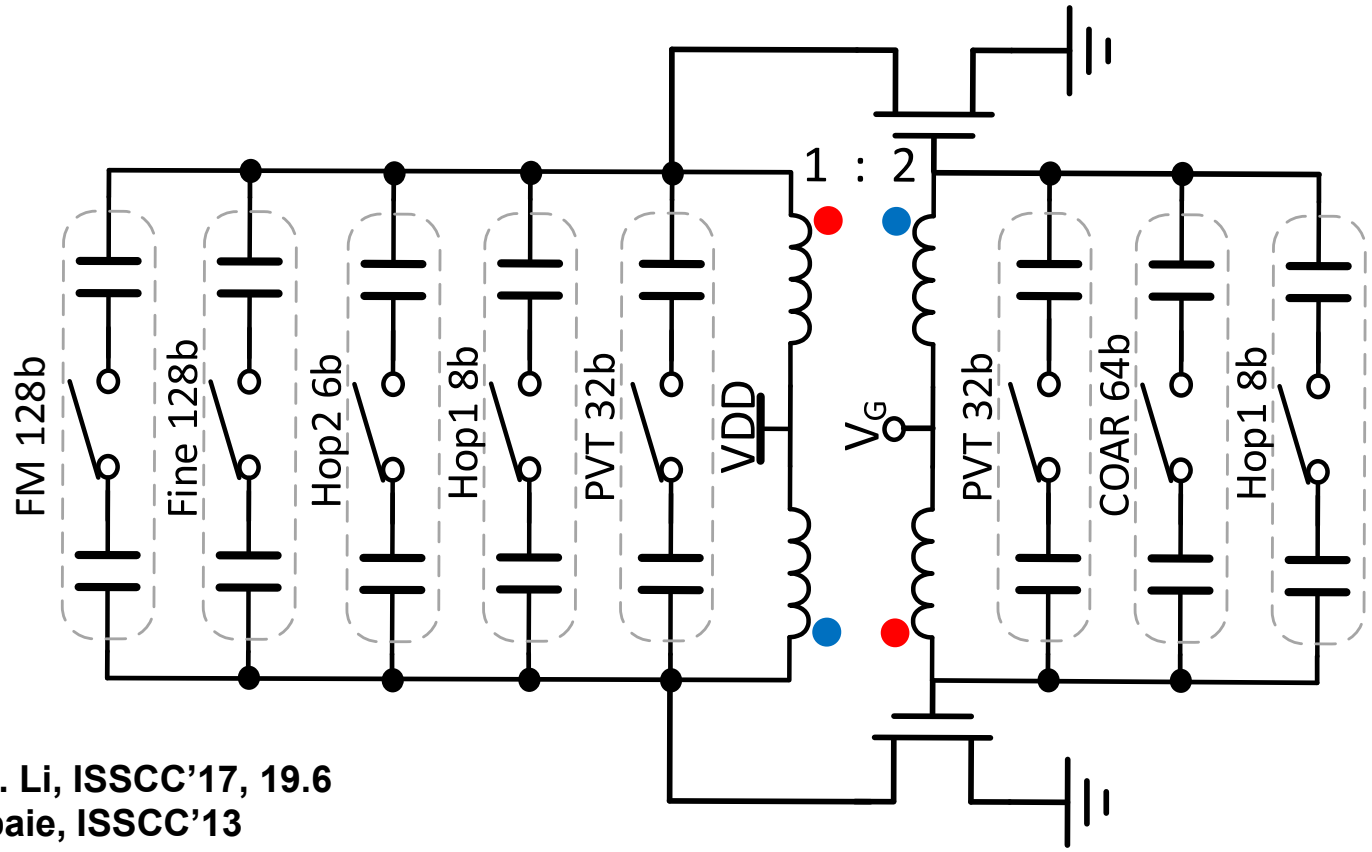
$$\nabla[n] = (\text{filtered } \phi_E[n]) * \text{sign}(CH[n] - 20)$$

Bird's Eye View of the Proposed ADPLL



Transformer-Based DCO

- 1:2 transformer for passive voltage gain
- Impedance transformation to generate finer resolution



$$f_{DCO} = \frac{1}{2\pi\sqrt{LC}}$$

C.C. Li, ISSCC'17, 19.6
Babaie, ISSCC'13

Transformer-Based DCO

- 1:2 transformer for passive voltage gain
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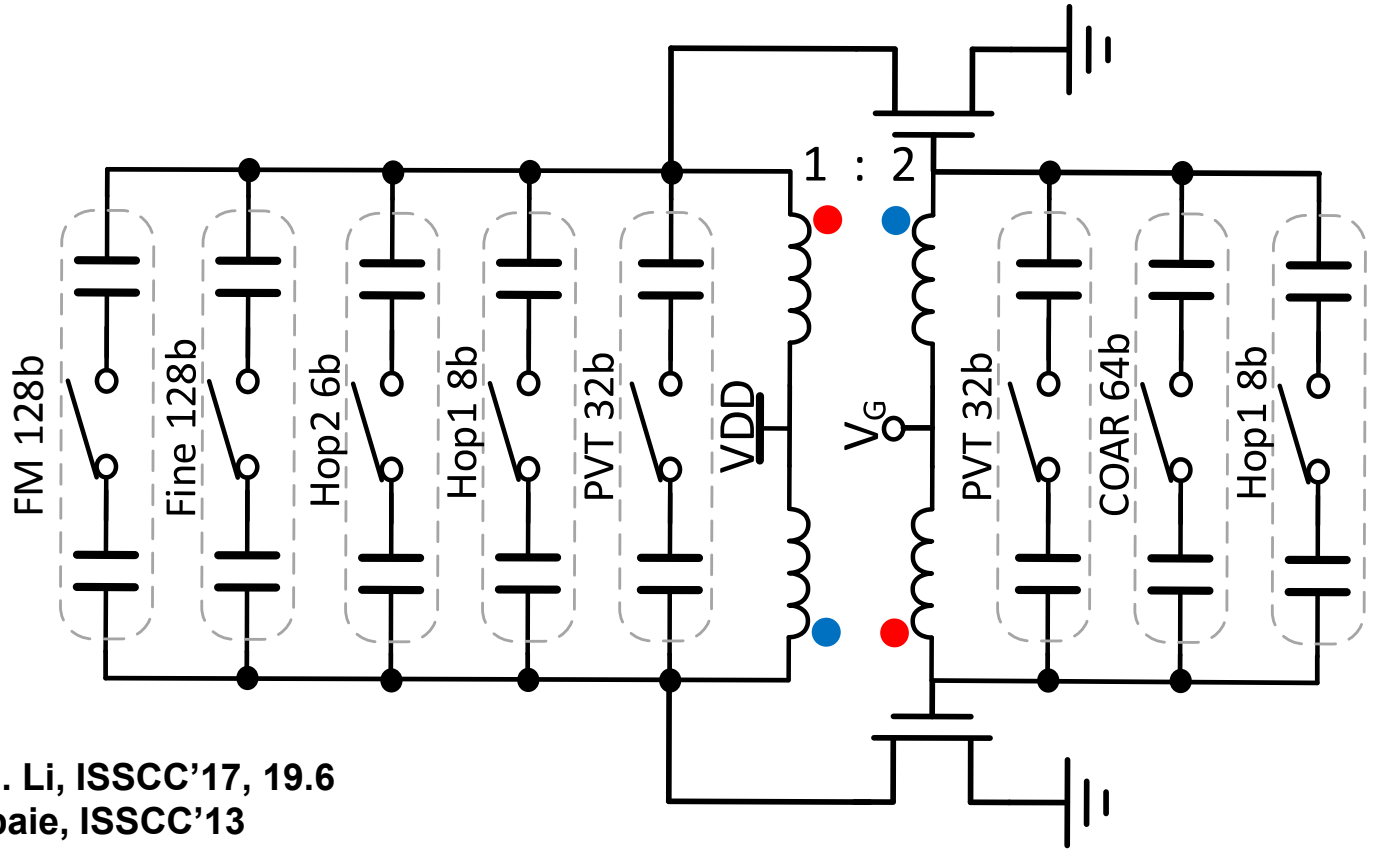

$$f_{DCO} = \frac{1}{2\pi\sqrt{LC}}$$

$$\Delta f = \frac{1}{2\pi\sqrt{L\Delta C}}$$

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Babaie, ISSCC'13

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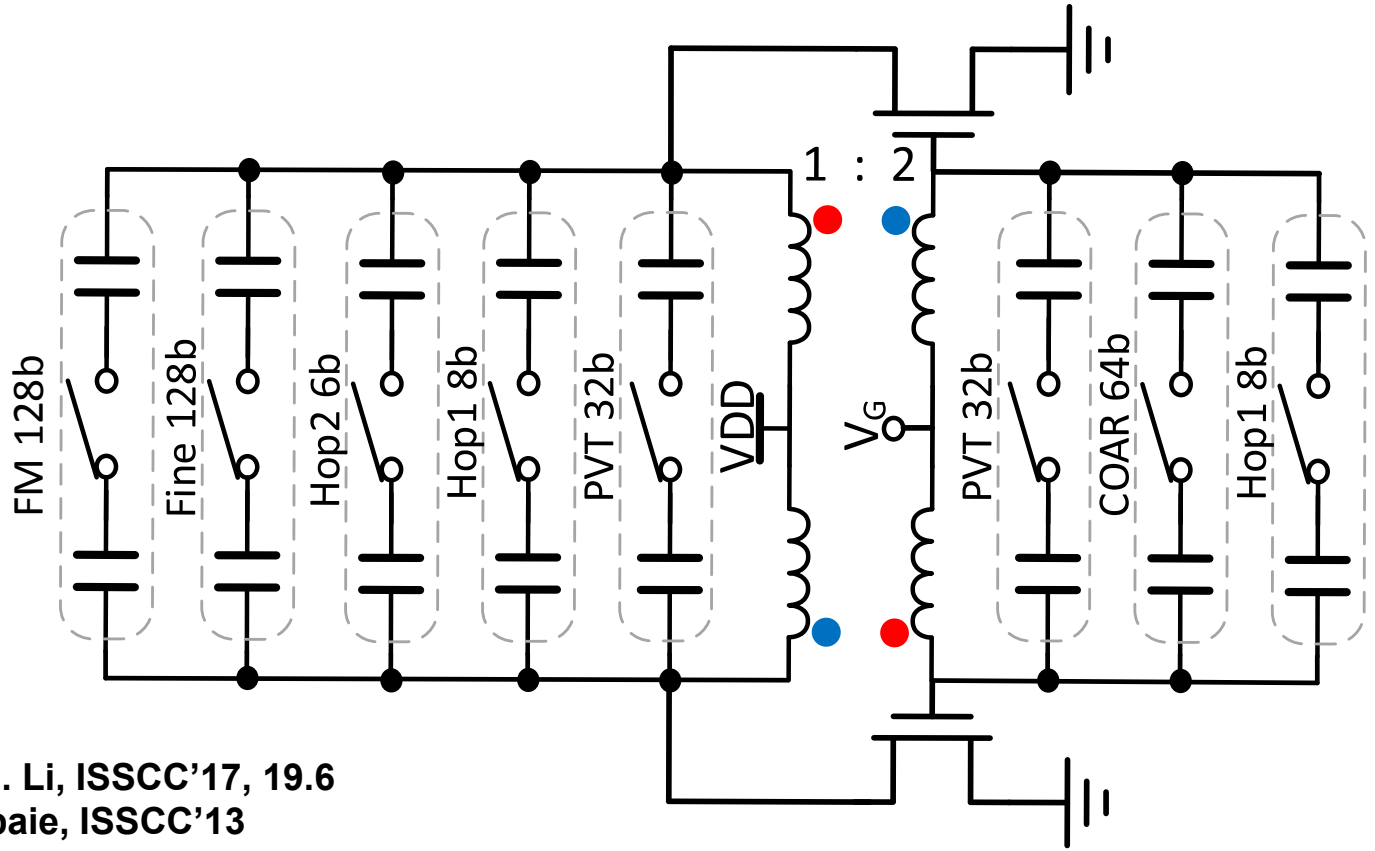


C.C. Li, ISSCC'17, 19.6
Babaie, ISSCC'13

$$f_{DCO} = \frac{1}{2\pi\sqrt{LC}}$$

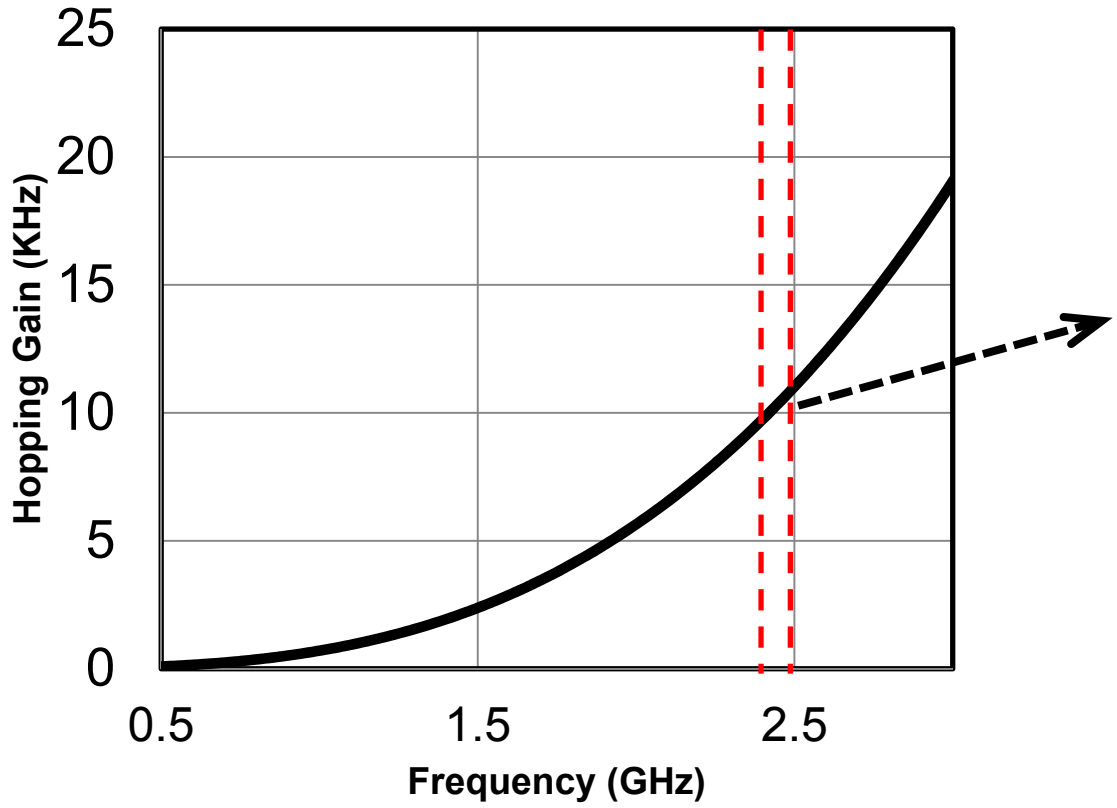
$$\Delta f = \frac{1}{2\pi\sqrt{L\Delta C}}$$

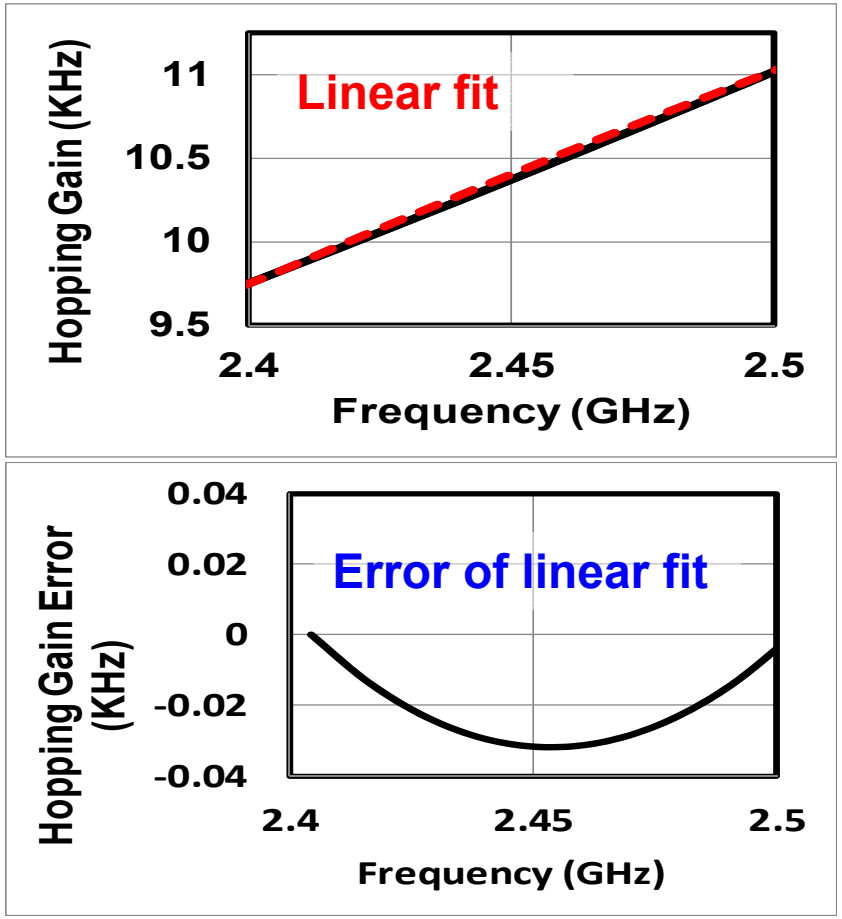
$$\frac{df}{dC} = \frac{-f}{2C}$$

$$\Delta f(f) = -2\pi^2(L\cdot\Delta C)f^3$$

Cubic Factor of DCO Gain vs. Frequency

- Cubic curve model at wide frequency span
- Almost linear DCO gain variation for BLE 80MHz band span





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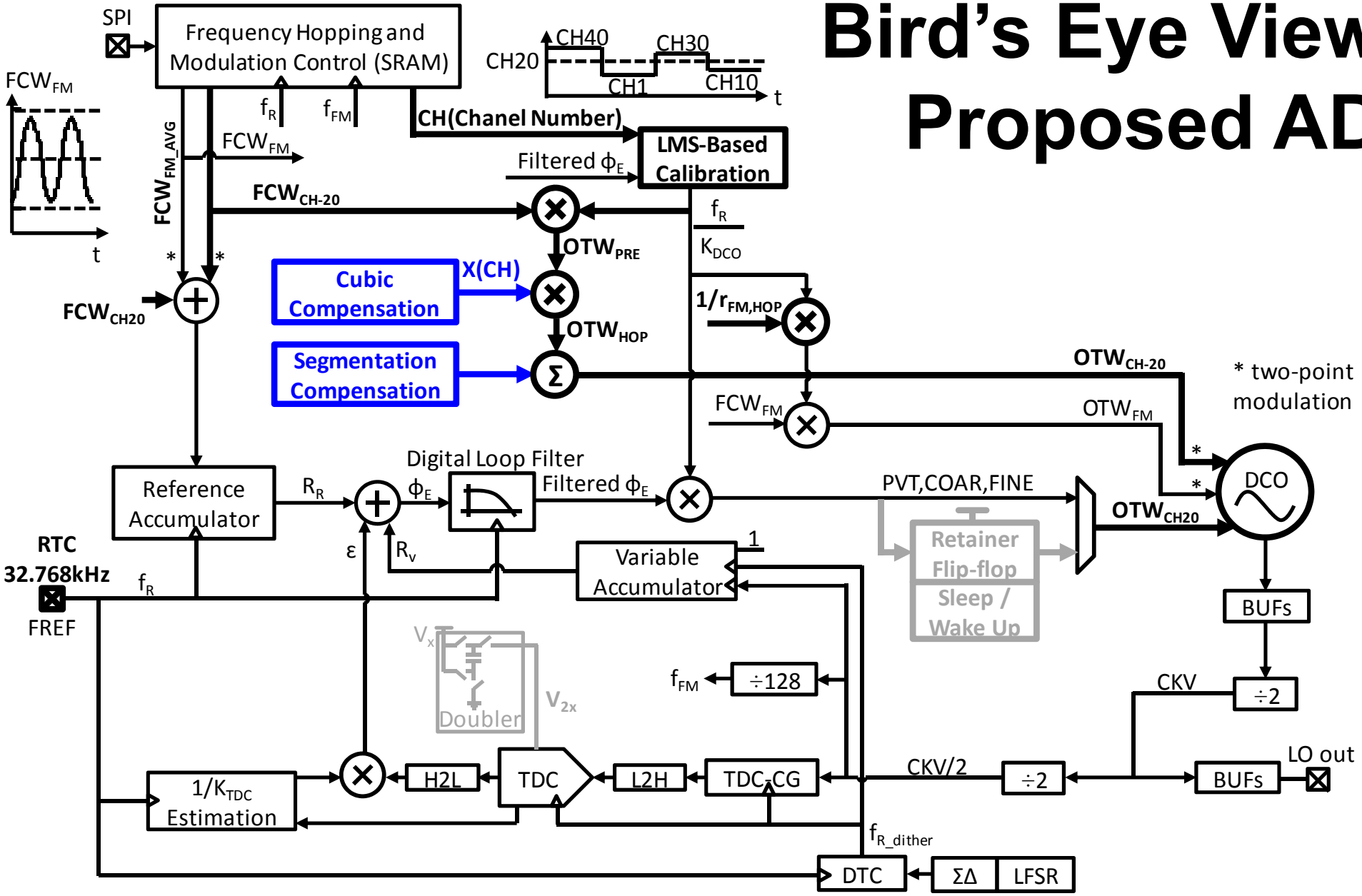
  - $OTW_{CH\text{-}20} = (CH\text{-}20) * \Delta f_{CH} / K_{DCO}$

    $= [(CH\text{-}20) * \Delta f_{CH} / f_R] * (f_R / K_{DCO}) = X * FCW_{CH\text{-}20} * (f_R / K_{DCO})$

- GFSK modulation range of $\pm$250kHz
  - $OTW_{FM} = Y * FCW_{FM} * (f_R / K_{DCO})$

To compensate the K_{DCO} non-linearity effects by multiplying FCW with a reverse factor to get an "Effective Flat" DCO gain over frequency range !!

Bird's Eye View of the Proposed ADPLL



Compensation for Cubic DCO Gain Variation

- Almost linear $K_{DCO}(CH)$ variation compared to $K_{DCO,\ CH20}$
- Compensated by reverse linear factor of X(CH)

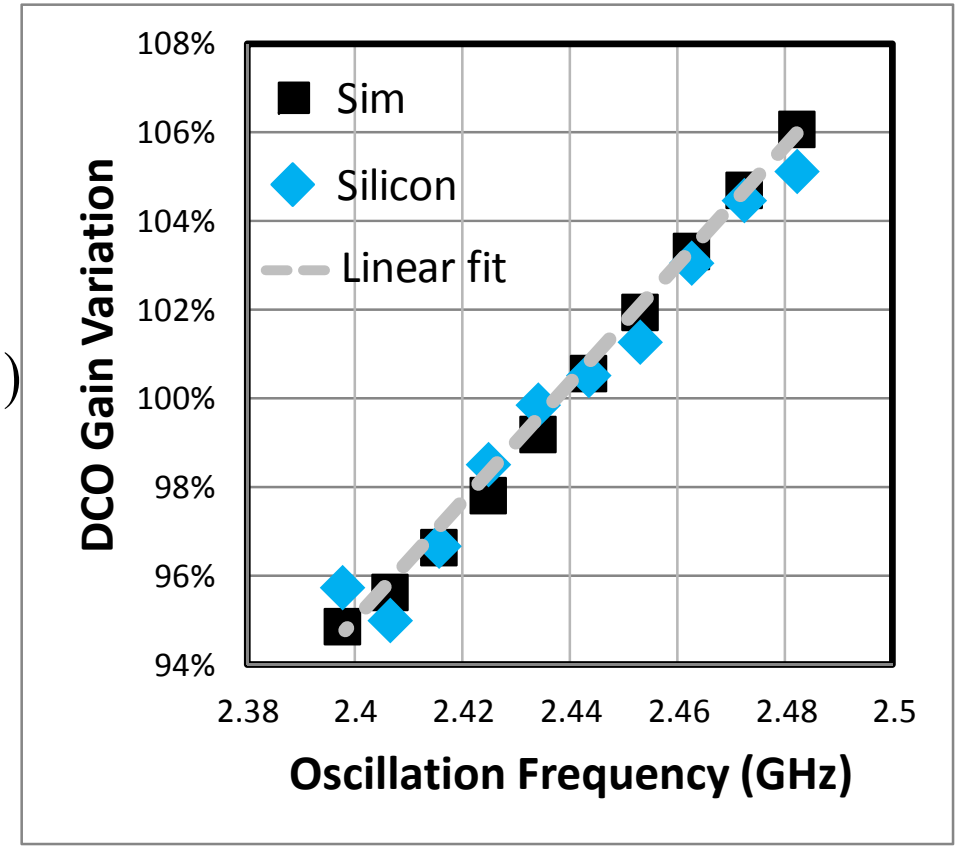
$$K_{DCO}(f) = 2\pi^2 (L \cdot \Delta C^T) f^3$$

$$\frac{dK_{DCO}(f)}{df} = 6\pi^2 (L \cdot \Delta C^T) f^2 = 3\frac{K_{DCO}(f)}{f}$$

$$K_{DCO}(CH) \cong K_{DCO,CH\ 20} + \frac{dK_{DCO}(f_{CH\ 20})}{df}(f_{CH} - f_{CH\ 20})$$

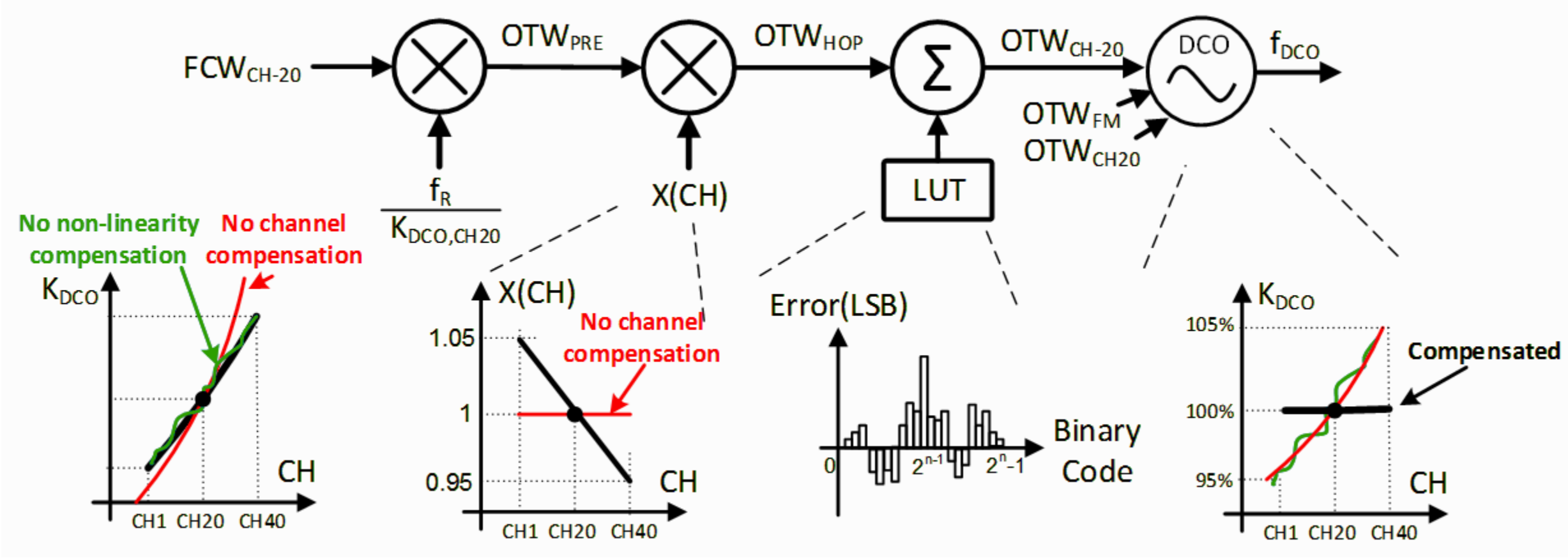
$$= K_{DCO,CH\ 20}\left(1 + 3\frac{f_{CH} - f_{CH\ 20}}{f_{CH\ 20}}\right)$$

$$X(CH) = \frac{1}{[1 + 3(f_{CH} - f_{CH\ 20})/f_{CH\ 20}]}$$

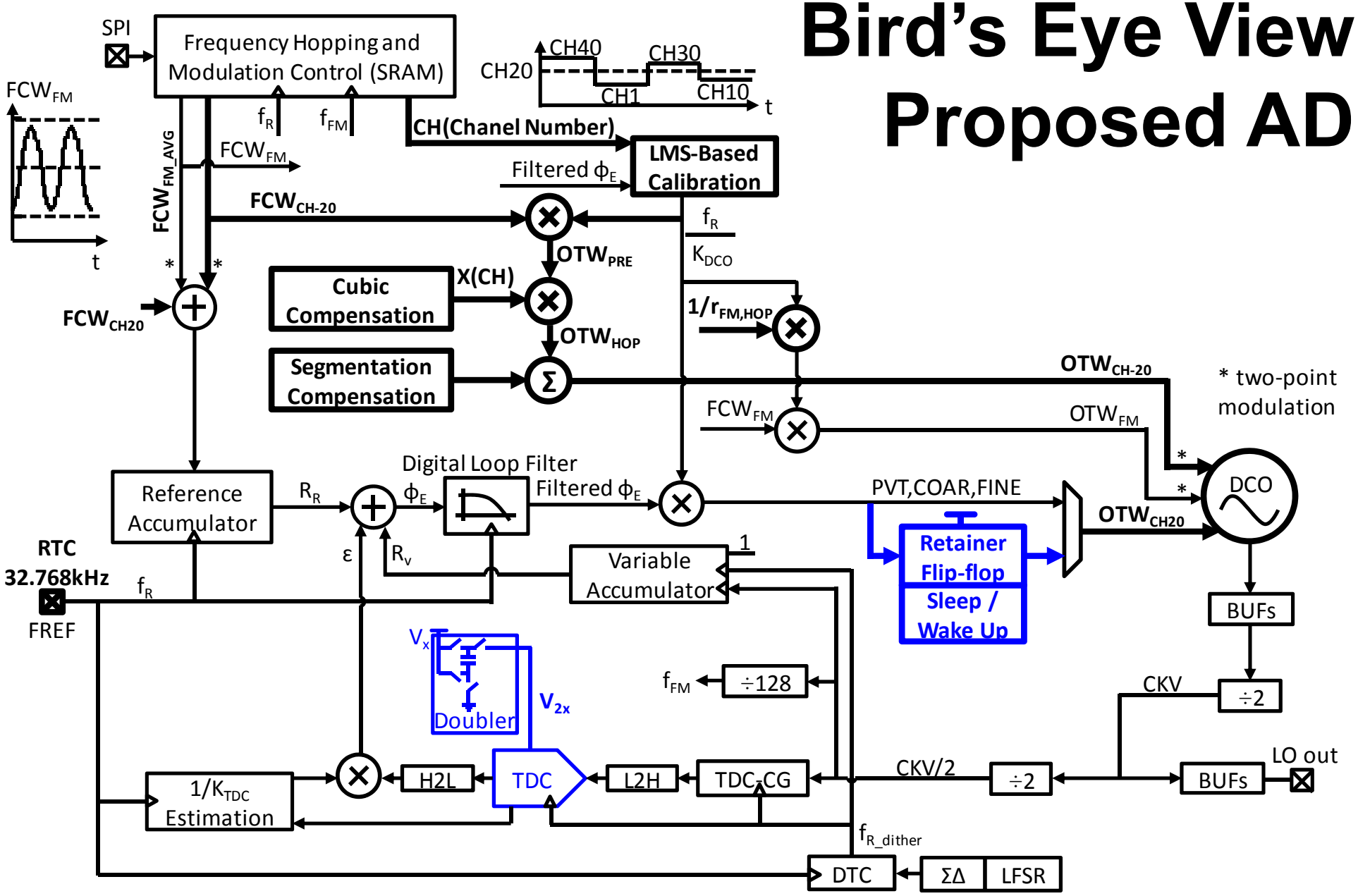


K_{DCO} Non-linearity Compensation Schemes

- Cubic compensation with linear factor X(CH)
- Segmentation technique compensates binary-weighted mismatch error

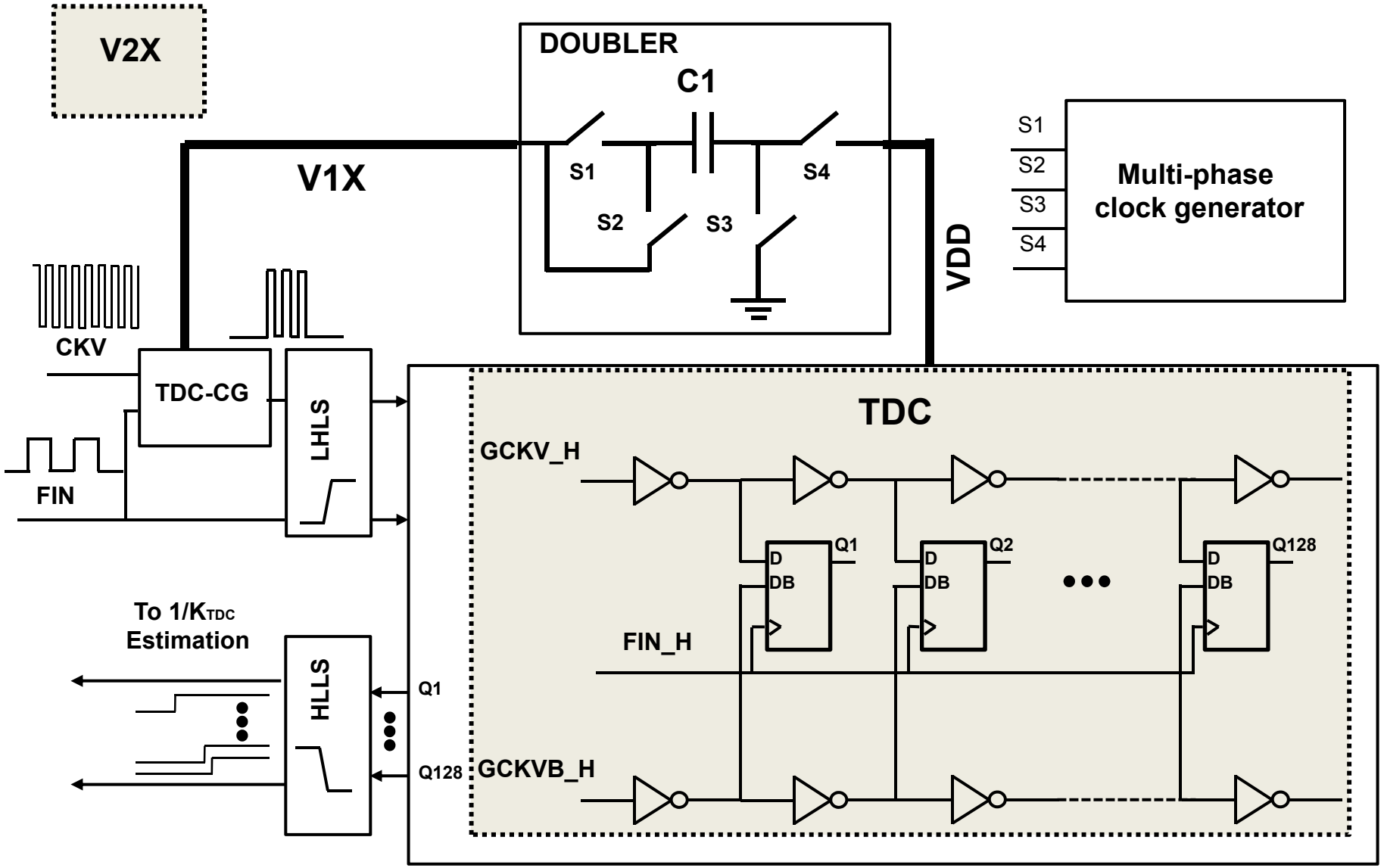


Bird's Eye View of the Proposed ADPLL

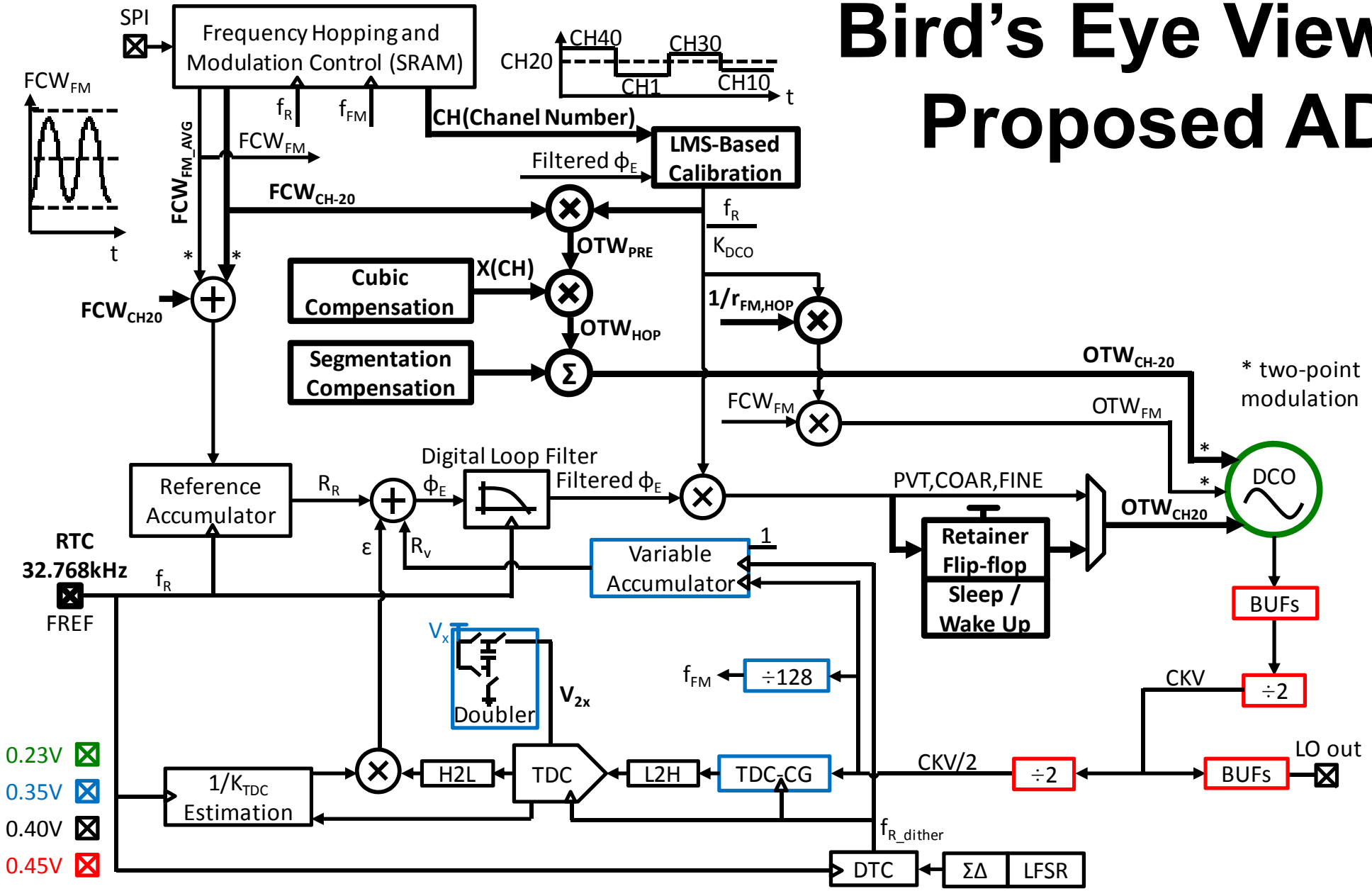


Voltage-doubler for TDC

- ADLL logic runs at sub-threshold of 0.4V
- TDC resolution enhanced by the voltage-doubler
  - 11.8ps resolution on V1X of 0.35V

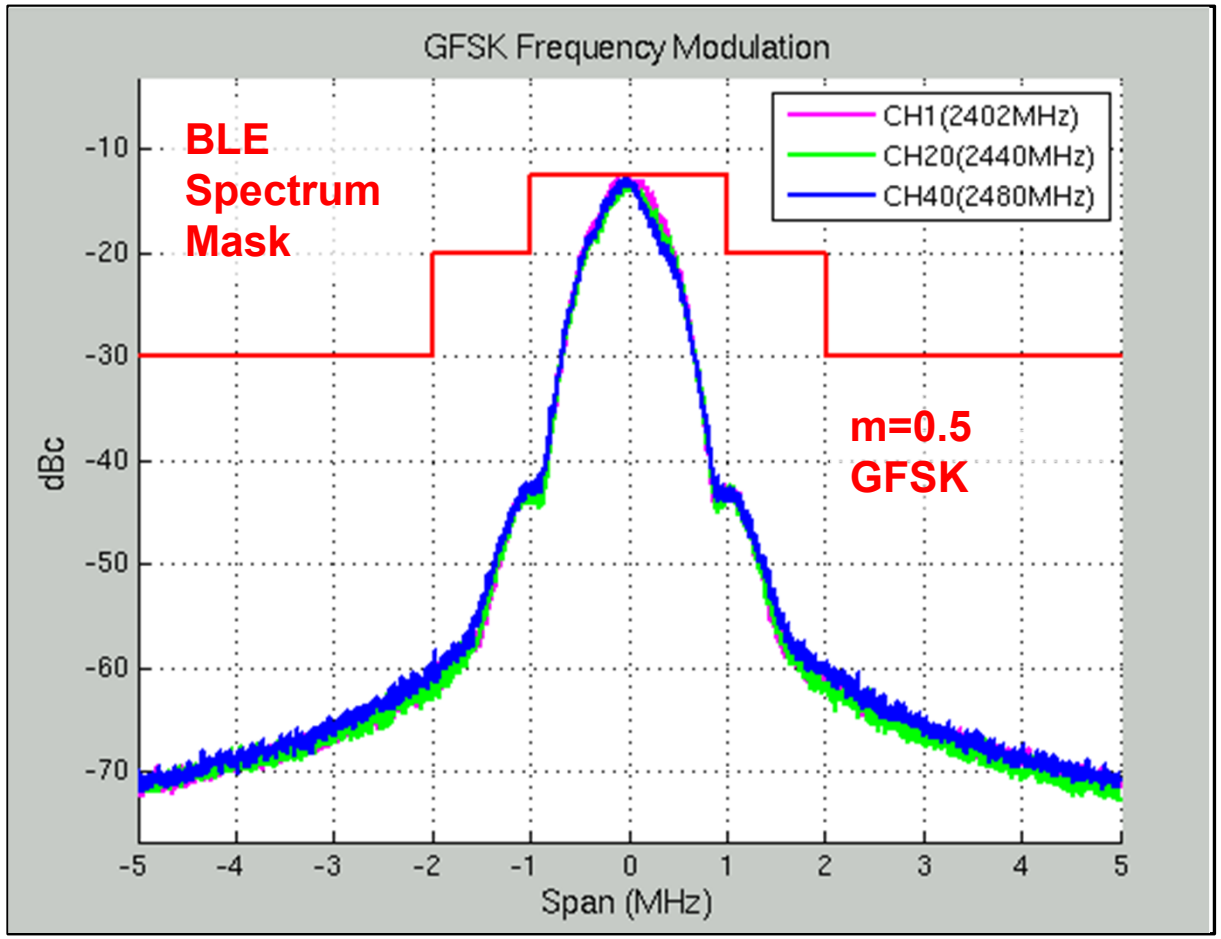


Bird's Eye View of the Proposed ADPLL

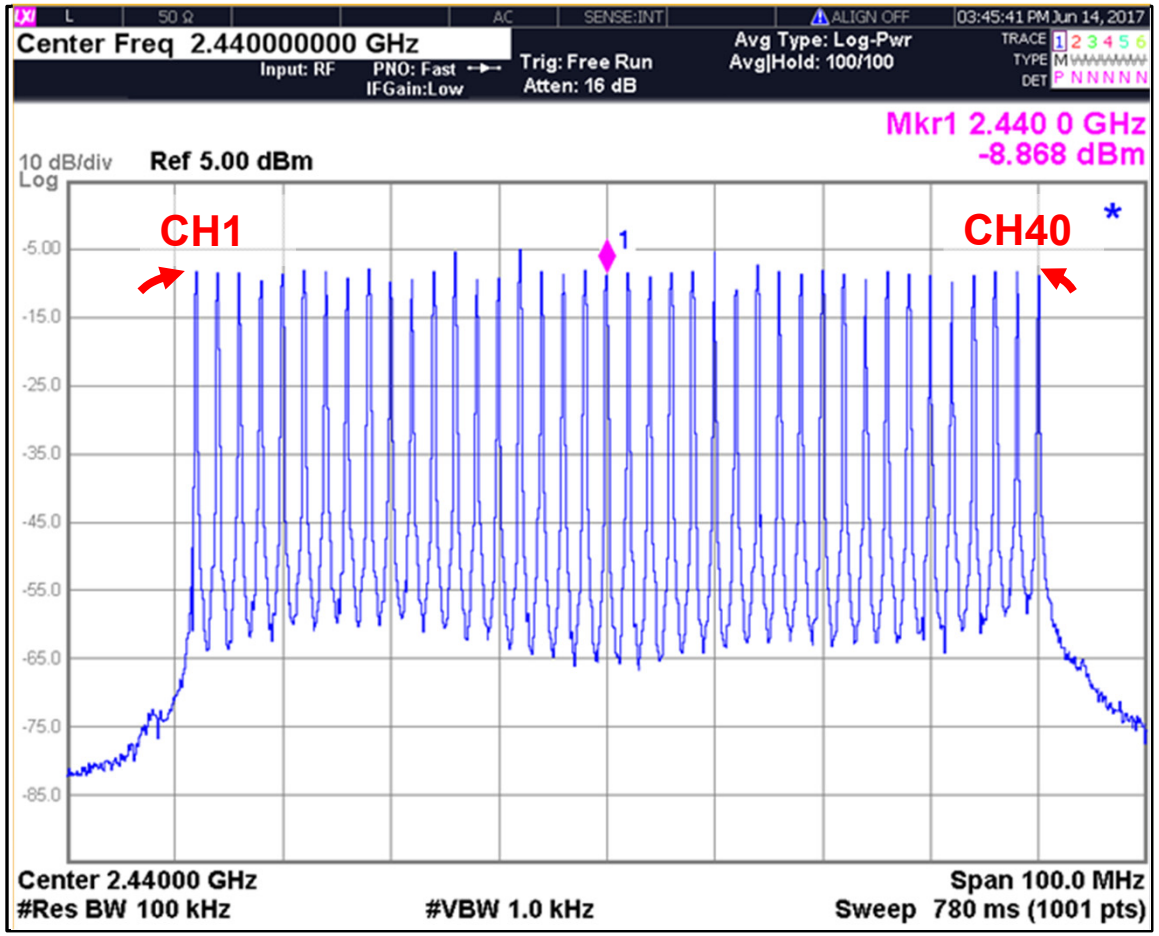


Measured Spectra of GFSK and Full-band Hopping

(3 extreme channels)

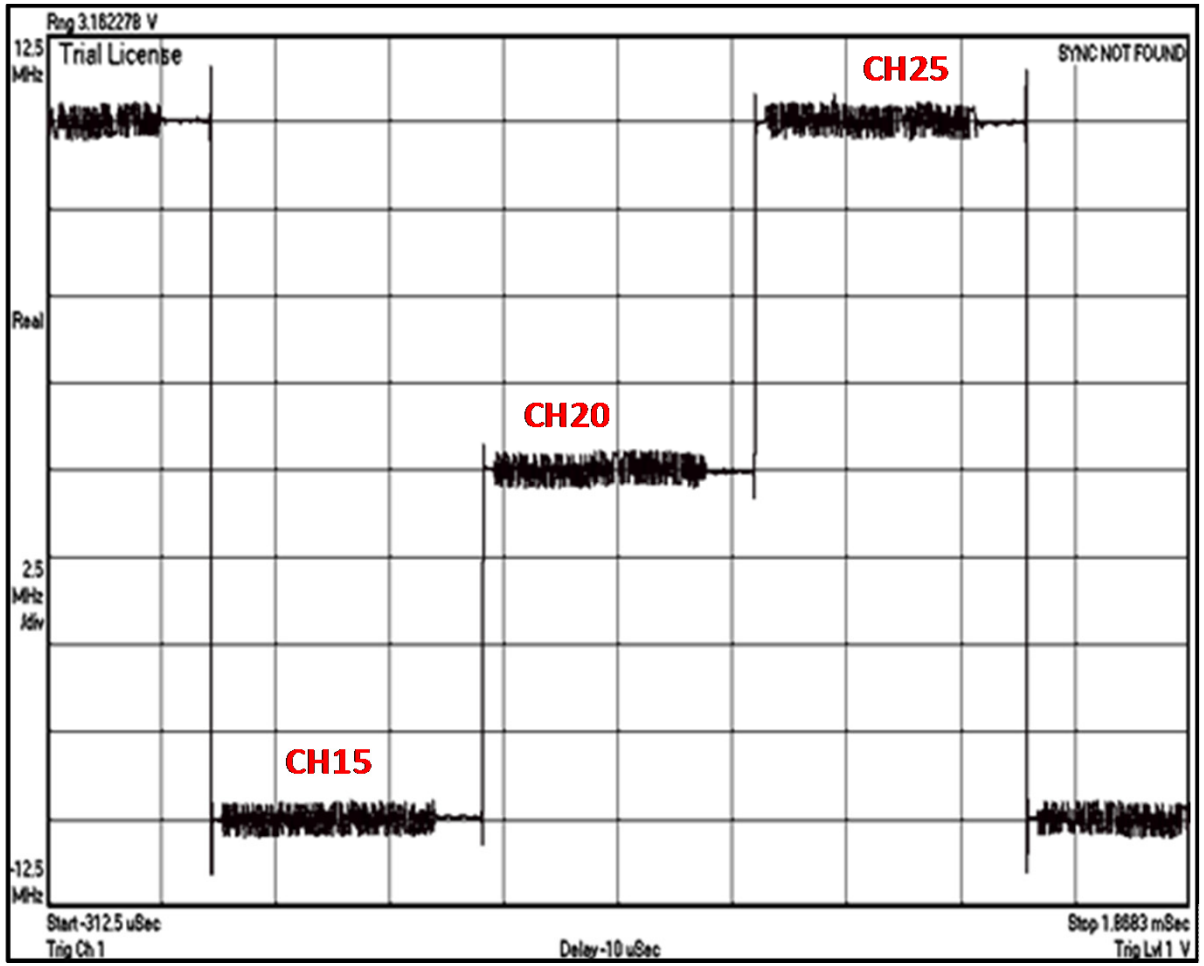


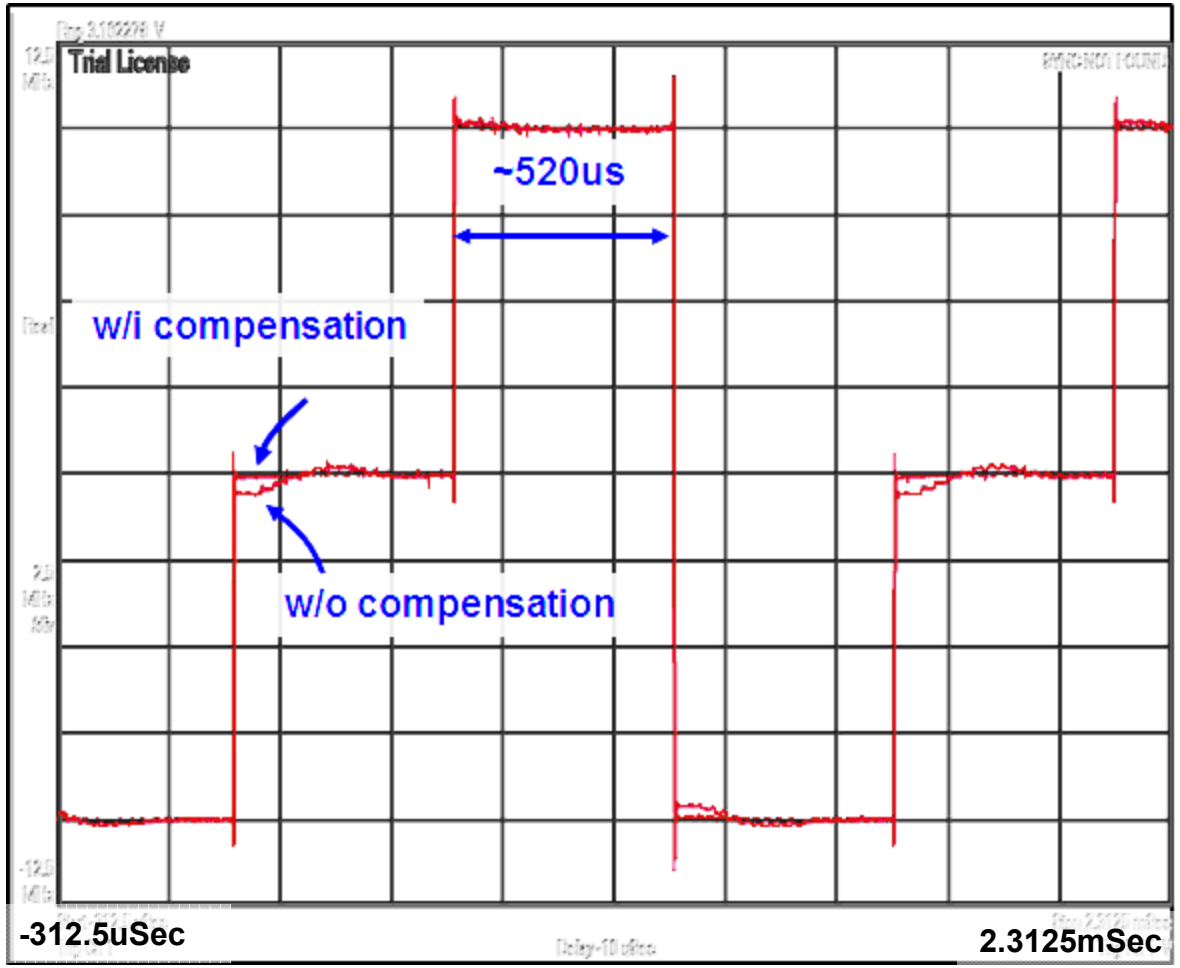
(All 40 channels)



Measured 3-Channel Hopping

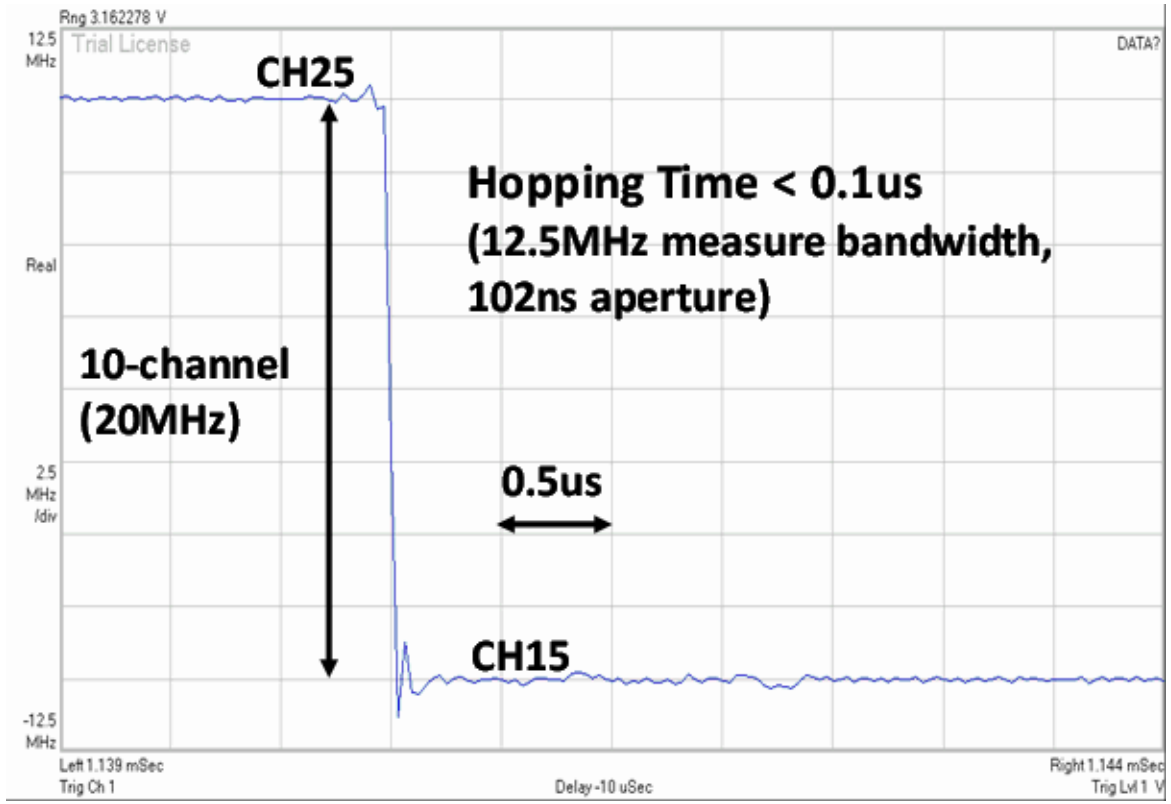
- Settling w/i and w/o DCO compensations

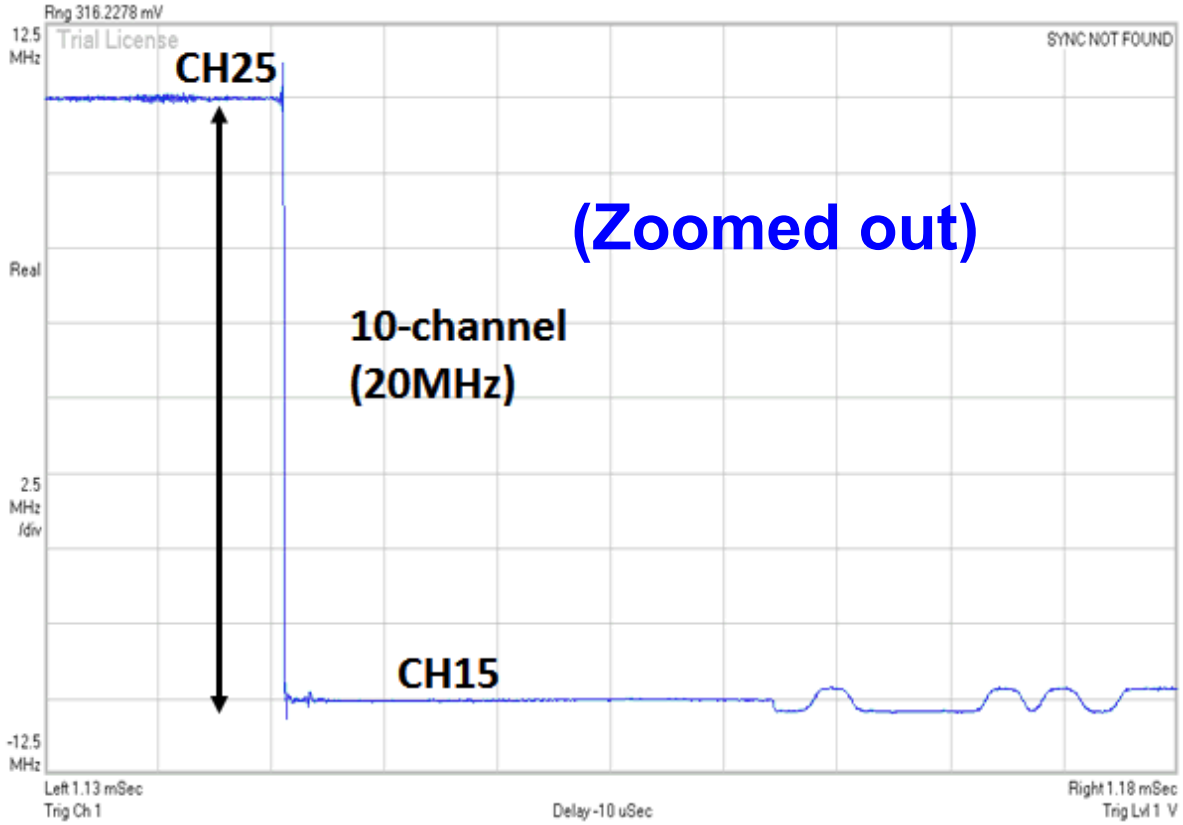




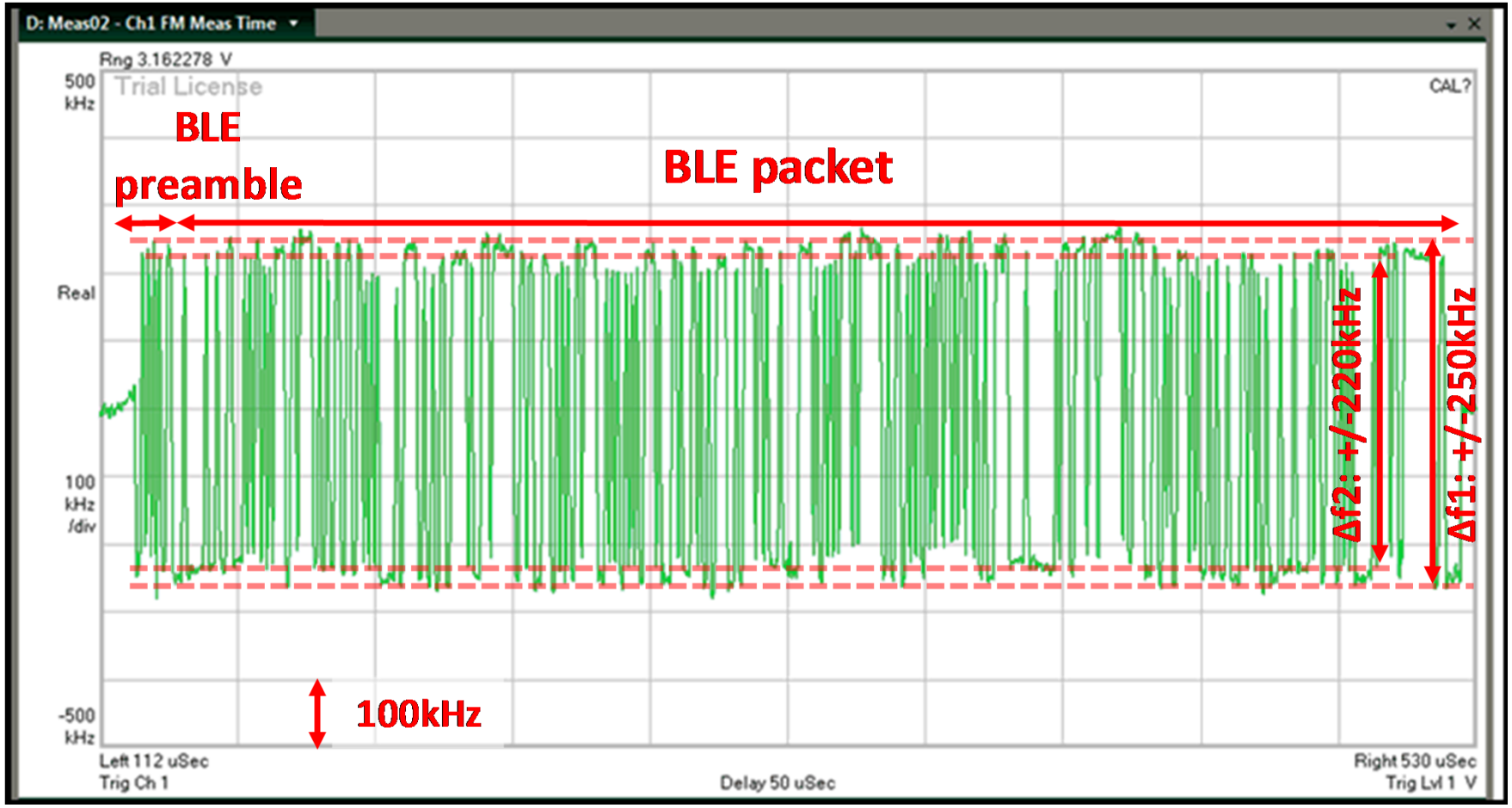
Measured Near-Instantaneous Hopping

- Settling time <0.1us
  - Limited only by test equipment time aperture



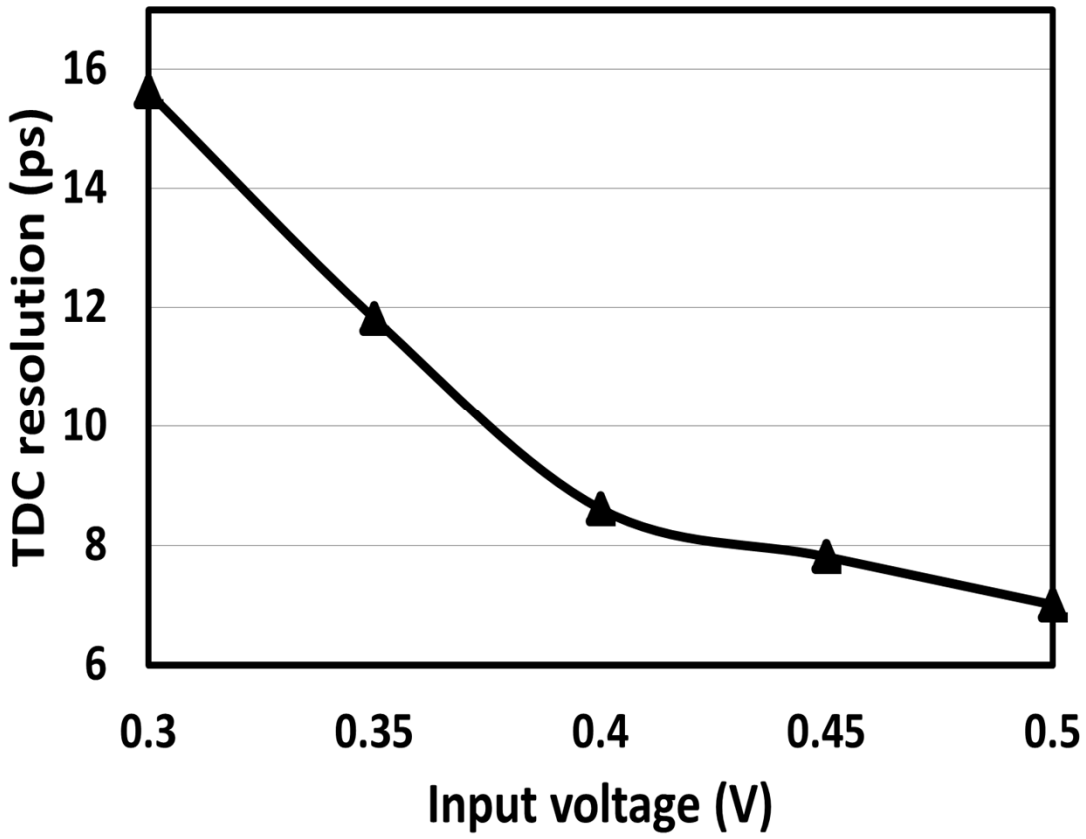


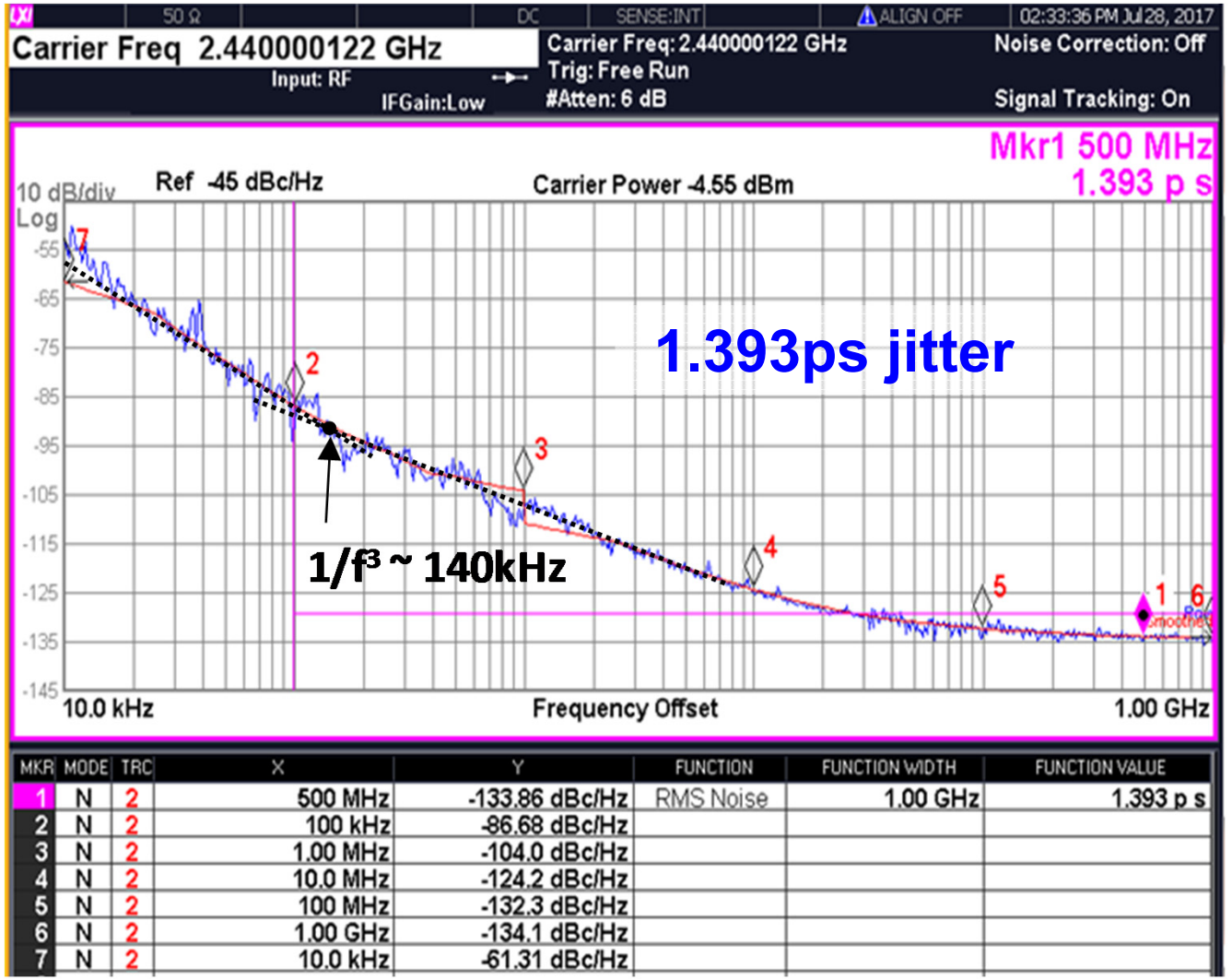
Measured Demodulated TX BLE Packet and its Frequency Deviation



Measured TDC Resolution and Phase Noise

- $1/f^3$ corner is ~ 140kHz

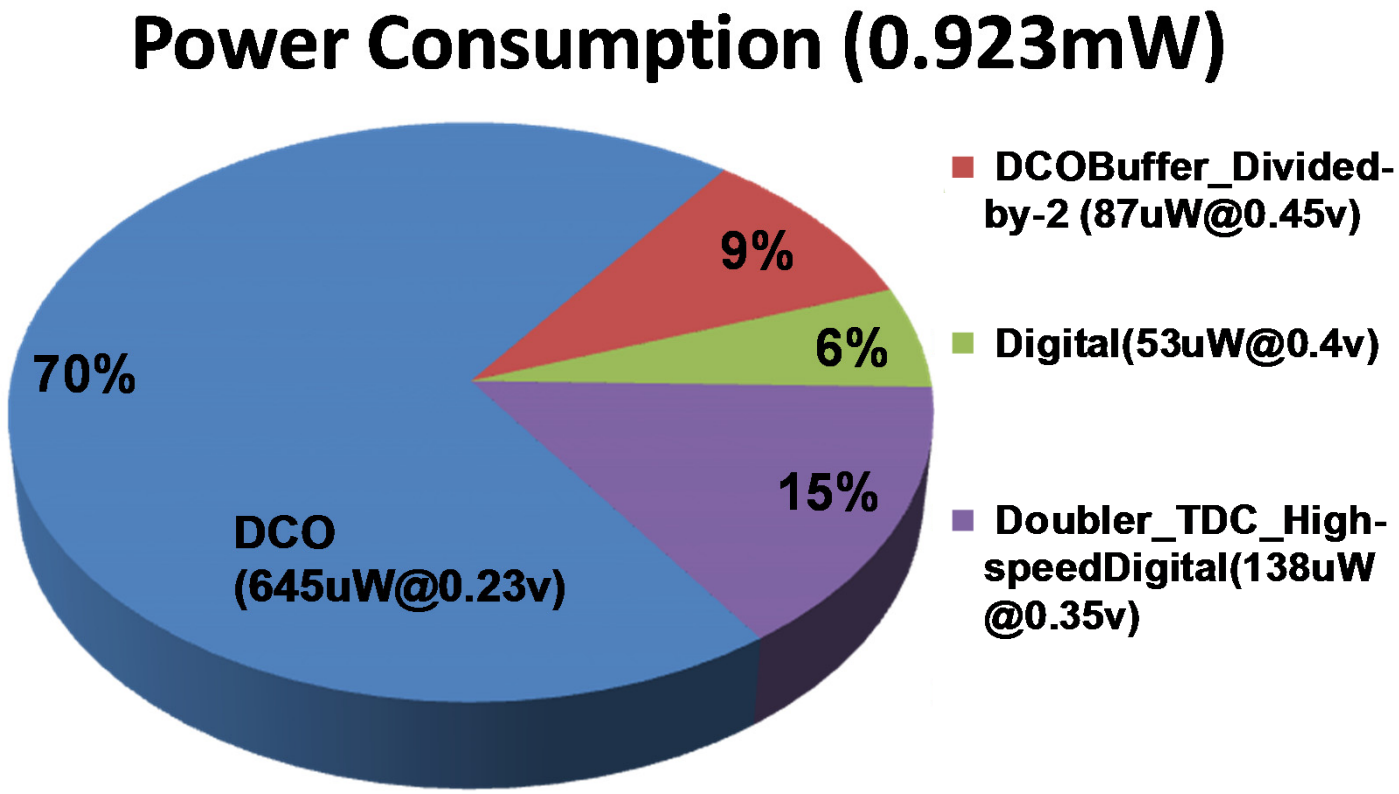




MKR	MODE	TRC	X	Y	FUNCTION	FUNCTION WIDTH	FUNCTION VALUE
1	N	2	500 MHz	-133.86 dBc/Hz	RMS Noise	1.00 GHz	1.393 p s
2	N	2	100 kHz	-86.68 dBc/Hz			
3	N	2	1.00 MHz	-104.0 dBc/Hz			
4	N	2	10.0 MHz	-124.2 dBc/Hz			
5	N	2	100 MHz	-132.3 dBc/Hz			
6	N	2	1.00 GHz	-134.1 dBc/Hz			
7	N	2	10.0 kHz	-61.31 dBc/Hz			

Power Consumption

- ADPLL logic at 32kHz now consumes the least power
- Further power reduction must come from DCO
- No power wasted for crystal oscillator !



Performance Table

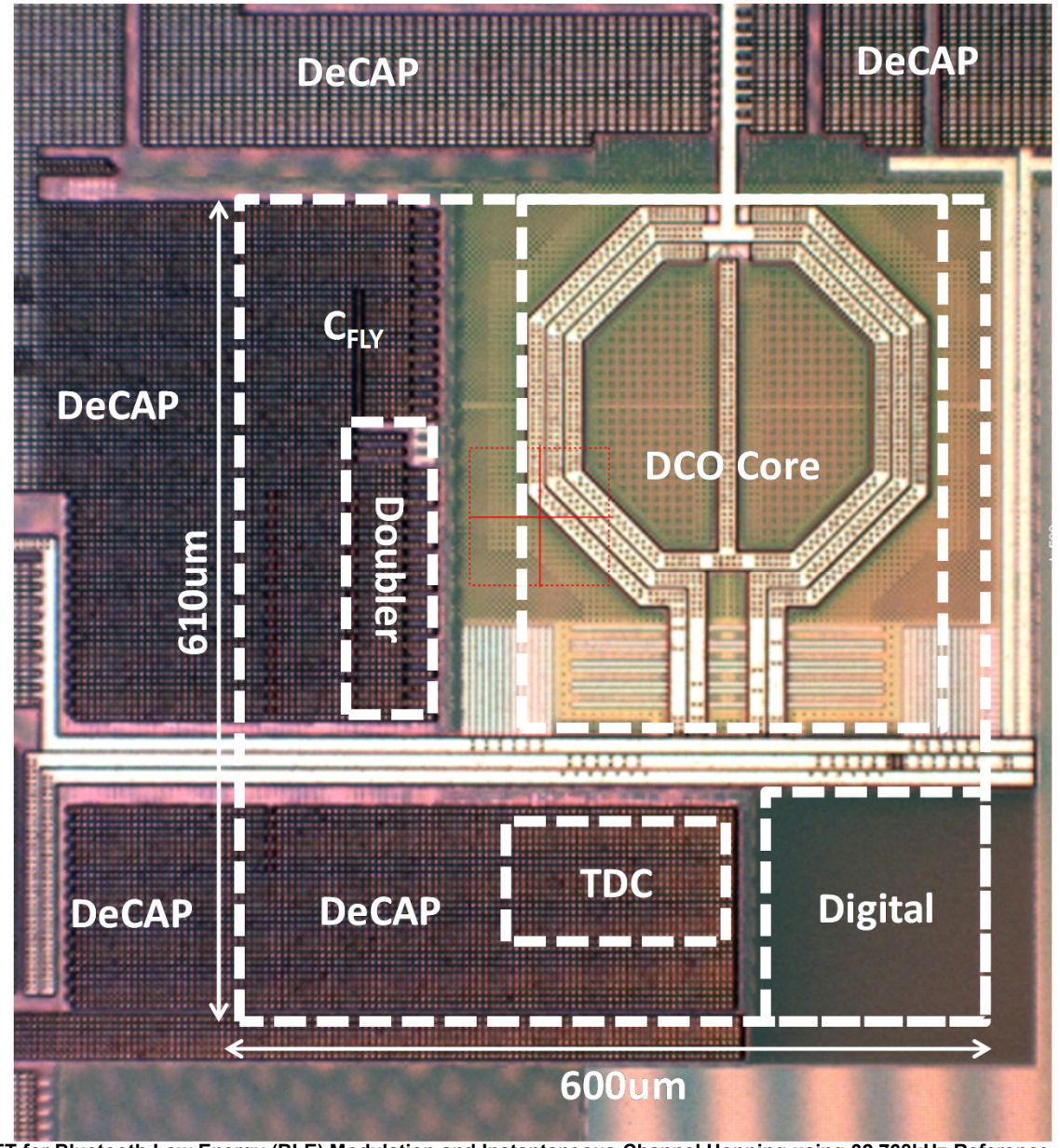
	This work	[1] JSSC'17	[2] ISSCC'17	[3] ISSCC'13	[4] ISSCC'12
Architecture	ADPLL TDC	ADPLL TDC	ADPLL TDC+DTC	ADPLL TDC	Analog CP-PLL
Technology	16nm FinFET	28nm	40nm	40nm	90nm
VDD(V)	< 0.45	1	1	1.3	1.2
Reference(MHz)	0.032	5-40	N/A	26	24
Output(GHz)	2.1-2.5	2.05-2.55	1.8-2.5	2.4	1.7-2.48
RMS Jitter (ps)	1.39**	1.23	1.98	0.98	2.66
Power (mW)	0.923	1.4	0.67	4.55	1.1
FOM*	-237.5	-236.7	-236	-233.6	-231
Core Area (mm^2)	0.24	0.24	0.18	0.075	0.75
Channel Hopping Settling Time(us)	< 0.1	15	11	N/A	< 40
TDC Resolution(ps)	7.8@0.45v 11.8@0.35v	12	N/A	7	N/A

*FoM=$10*\log[(\sigma^2_{jitter})*(P_{DC}/1mW)]$

** Integrated from 100kHz to 1GHz

Die Photo

- TSMC 16nm FinFET
- Core size is 0.024mm^2



Conclusion

- Proposed new paradigm: Elimination of conventional XO
  - Instead, use 32kHz real time clock
  - Reducing power, size and cost of IoT solution
- Near instantaneous channel hopping while maintaining the best-in-class performance at sub-mW power consumption
- Ultra-low voltage (0.45V) operation for BLE frequency synthesis of IoT application

Thanks for your attention !

A 0.2V Energy-Harvesting BLE Transmitter with a Micropower Manager Achieving 25% System Efficiency at 0dBm Output and 5.2nW Sleep Power in 28nm CMOS

Jun Yin [1], Shiheng Yang [1], Haidong Yi [1], Wei-Han Yu[1], Pui-In Mak [1] and Rui P. Martins [1,2]

1 – State-Key Laboratory of Analog and Mixed-Signal VLSI University of Macau, Macao, China

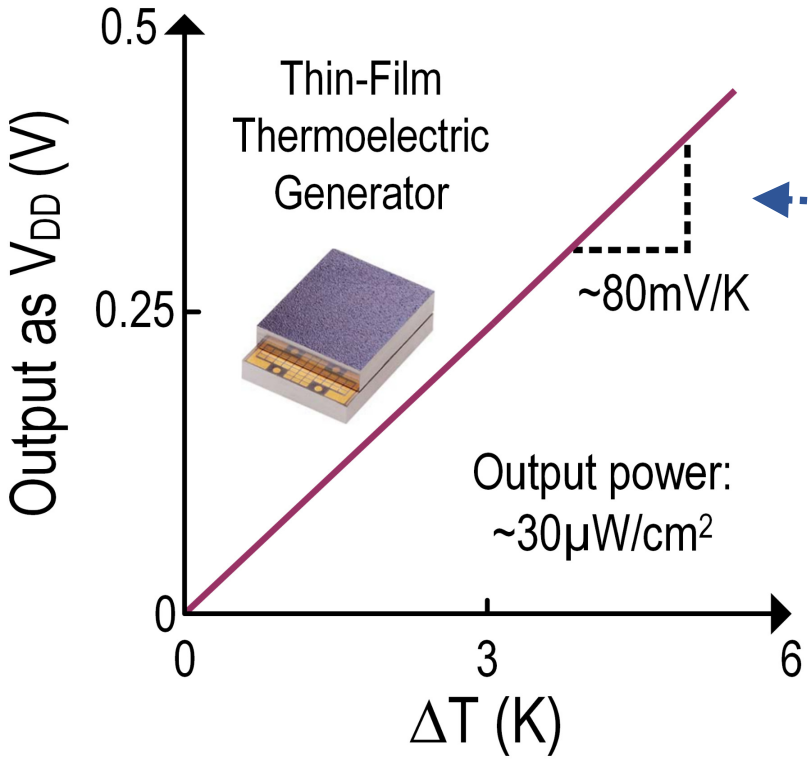
2 - Instituto Superior Técnico, University Lisboa, Portugal

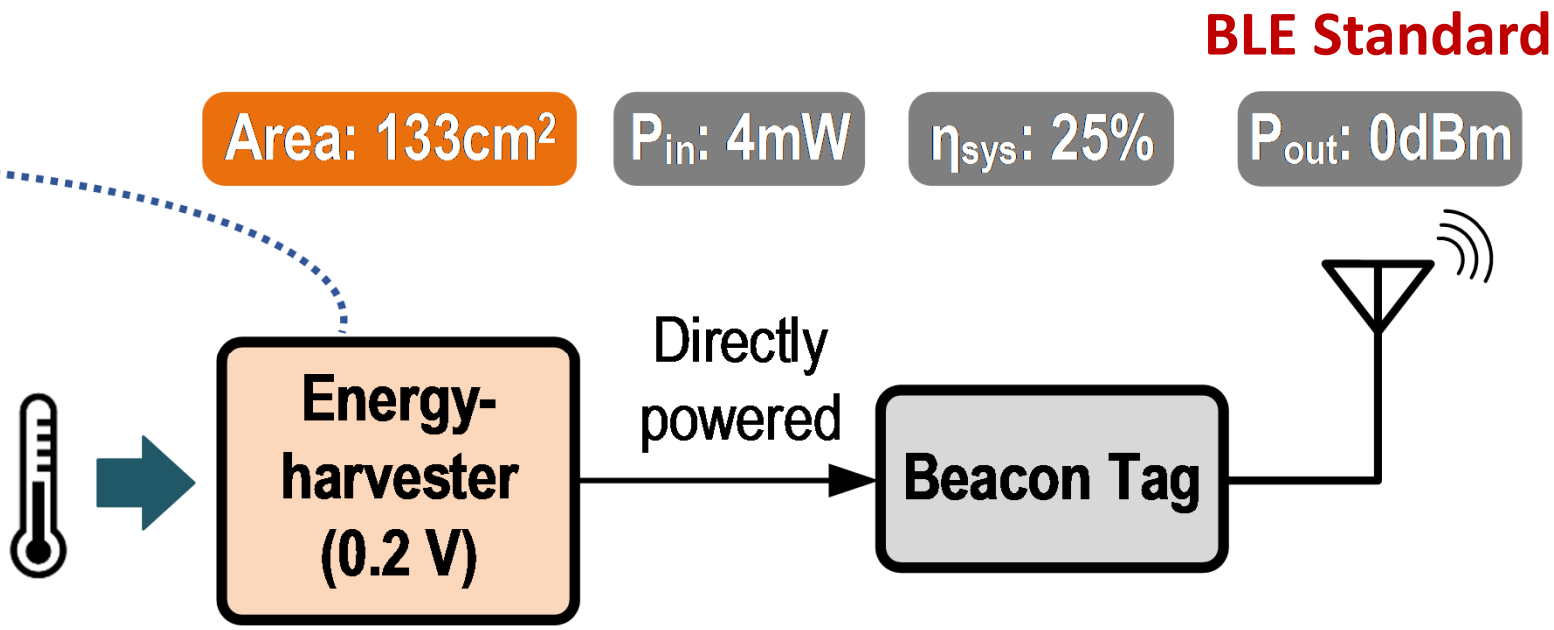
模擬與混合信號超大規模集成電路國家重點實驗室
State Key Laboratory of Analog and Mixed-Signal VLSI

Outline

- Introduction
- Proposed energy-harvesting BLE transmitter
  - **Micropower manager**
  - ULV gate-to-source-feedback **VCO**
  - ULV Class-E/F_2 **PA** with embedded 3rd-harmonic notching
  - ULV Type-I **PLL** with REF spur suppression
- Experimental results
- Conclusion

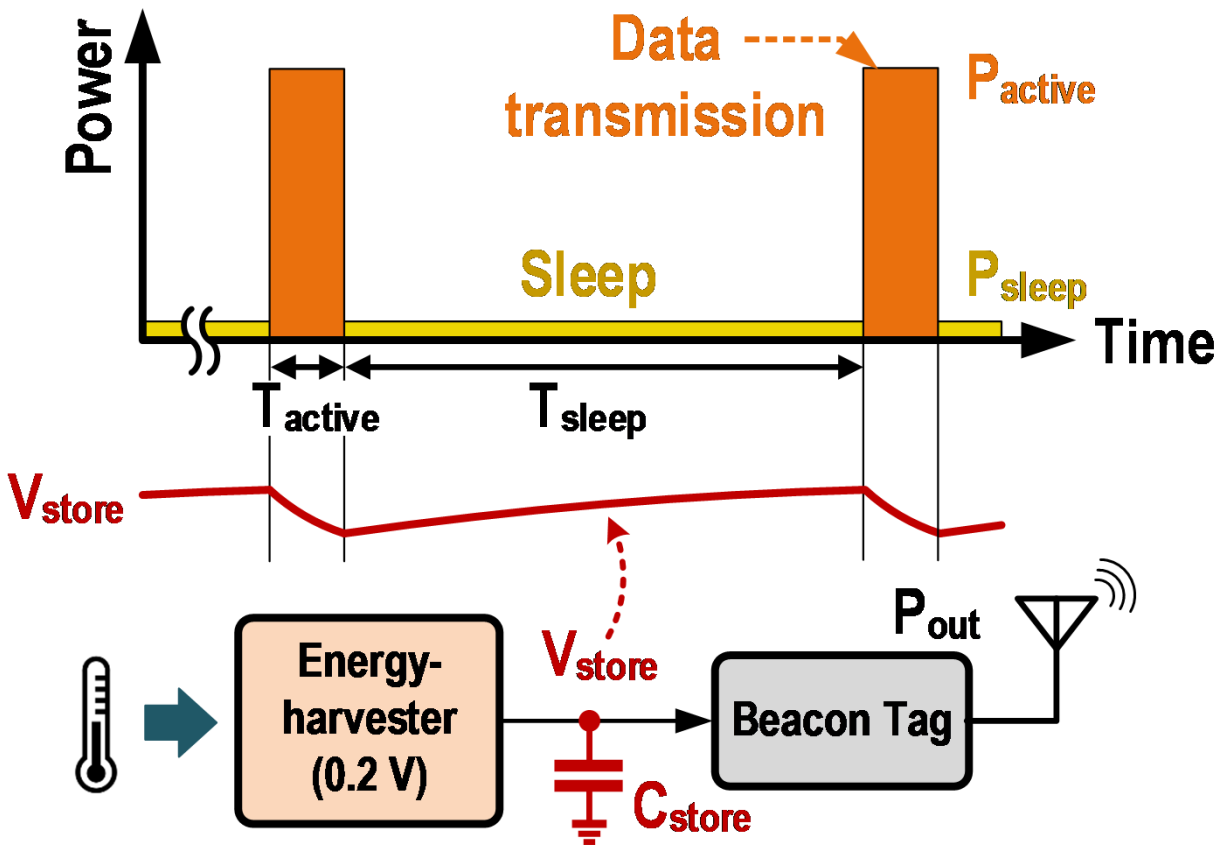
Energy-Harvesting for Wireless Sensor Tags

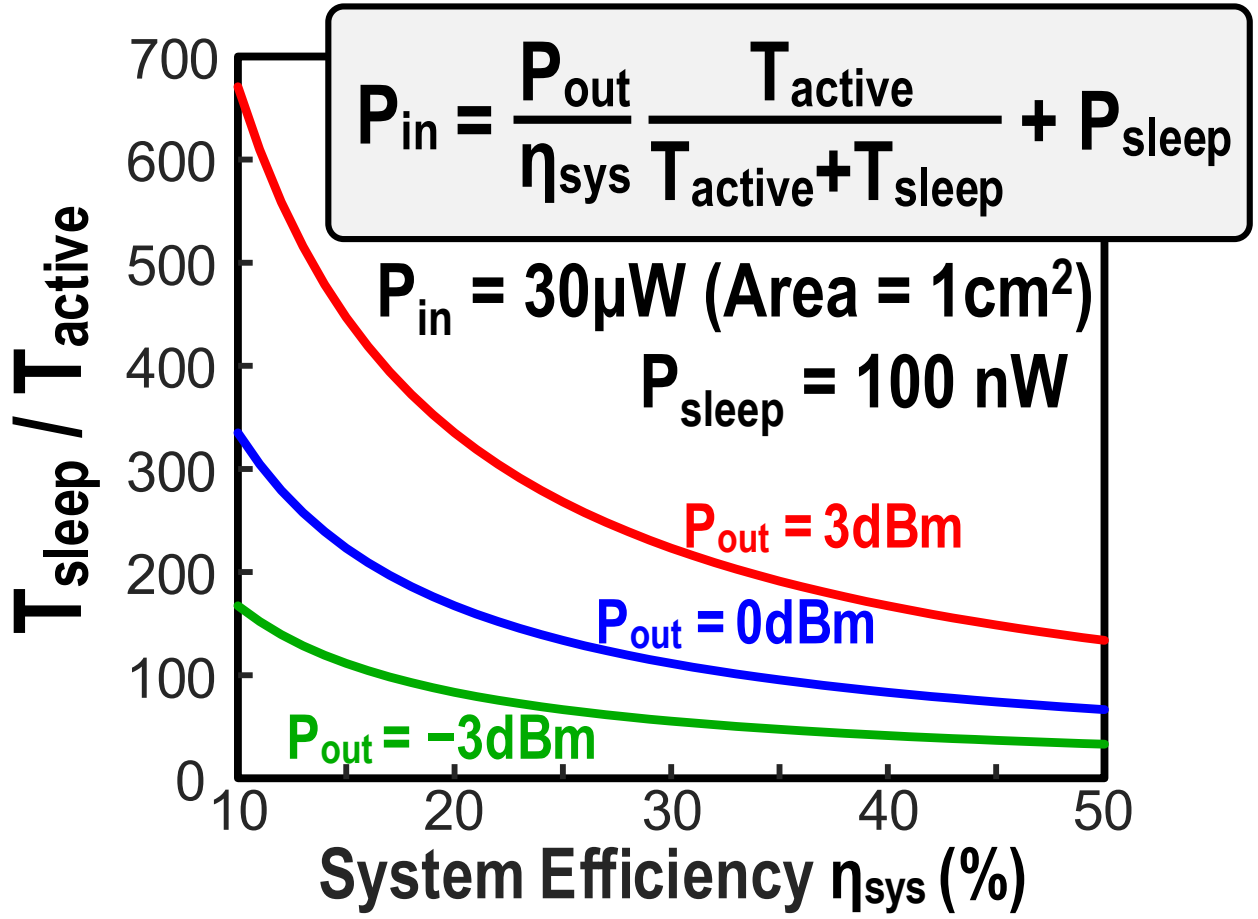




- Energy harvesting for high self-sustainability
- Large instantaneous power of transmitter → large harvester area

Duty-Cycling in ULP Radios (Power vs Latency)

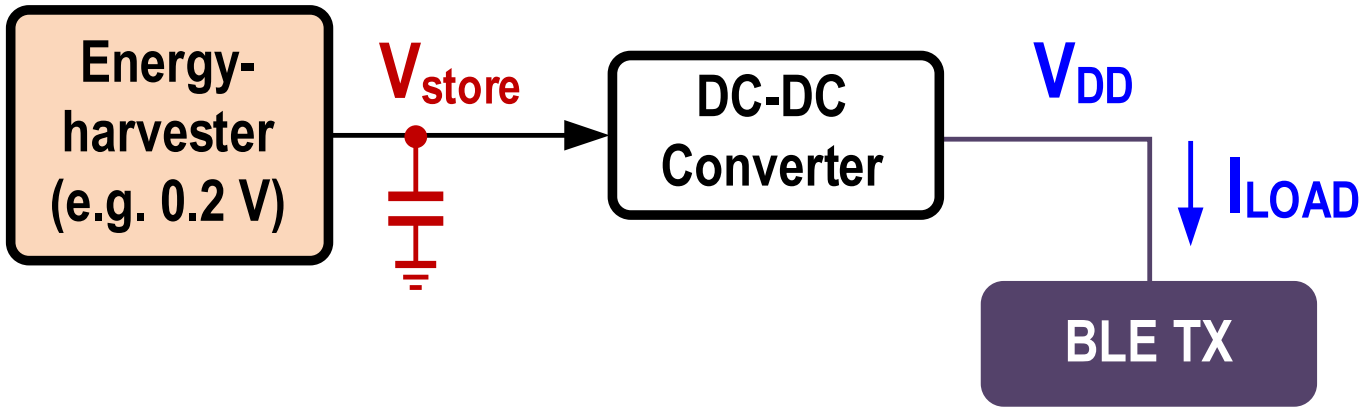




- Enquire a long sleep cycle to recover the power
- System Latency (T_{sleep} / T_{active}) be reduced by improving η_{sys}

Power Management Scheme

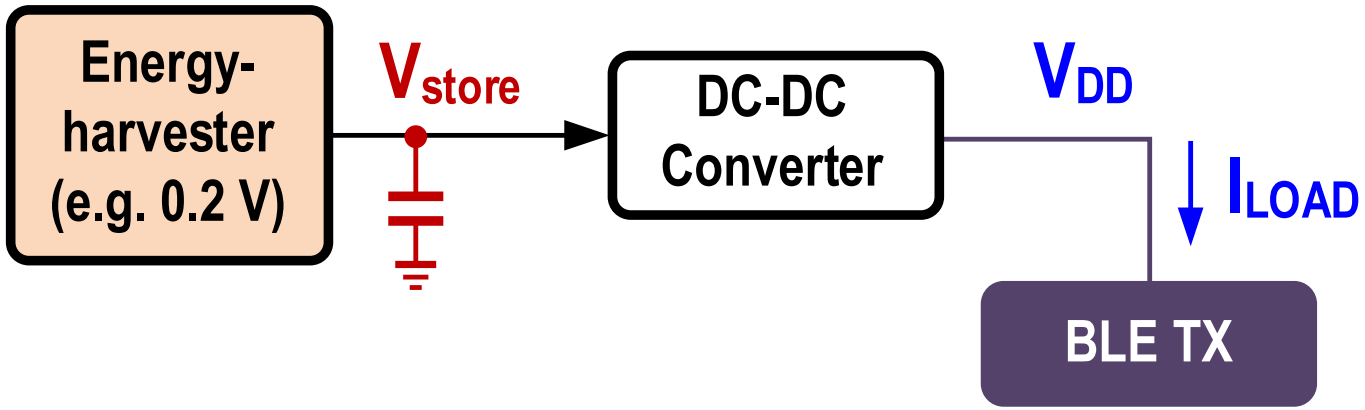
General Scheme



$$\eta_{sys} = \eta_{TX} \times \eta_{DC\text{-}DC}$$

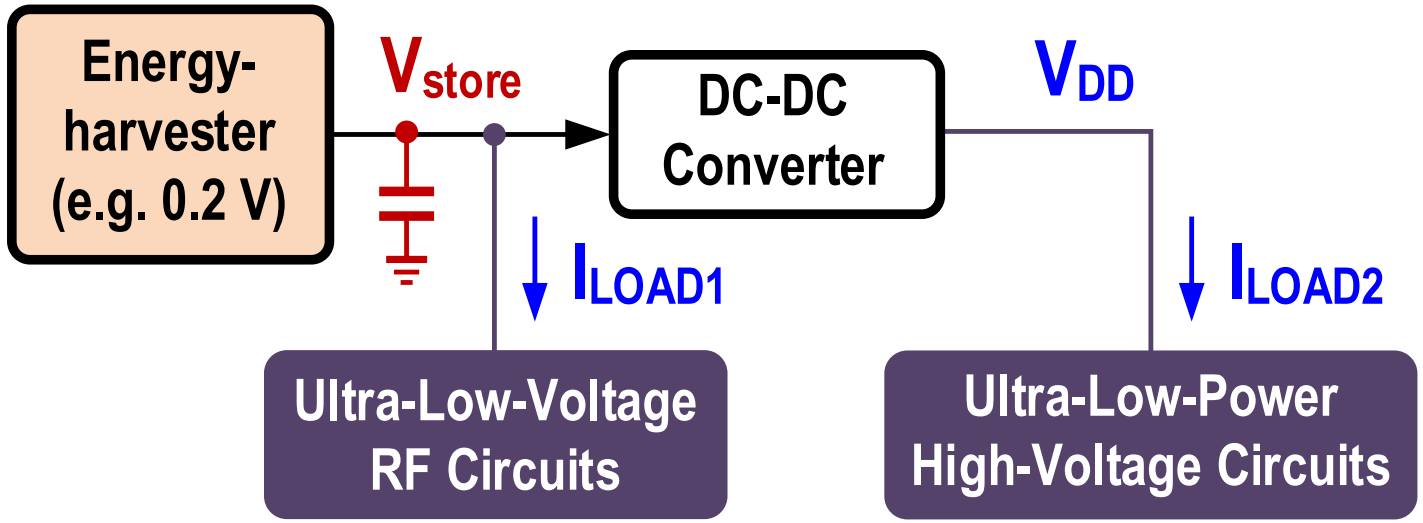
Power Management Scheme

General Scheme



$$\eta_{sys} = \eta_{TX} \times \eta_{DC\text{-}DC}$$

Proposed Scheme [W.-H. Yu et. al., ISSCC'17]

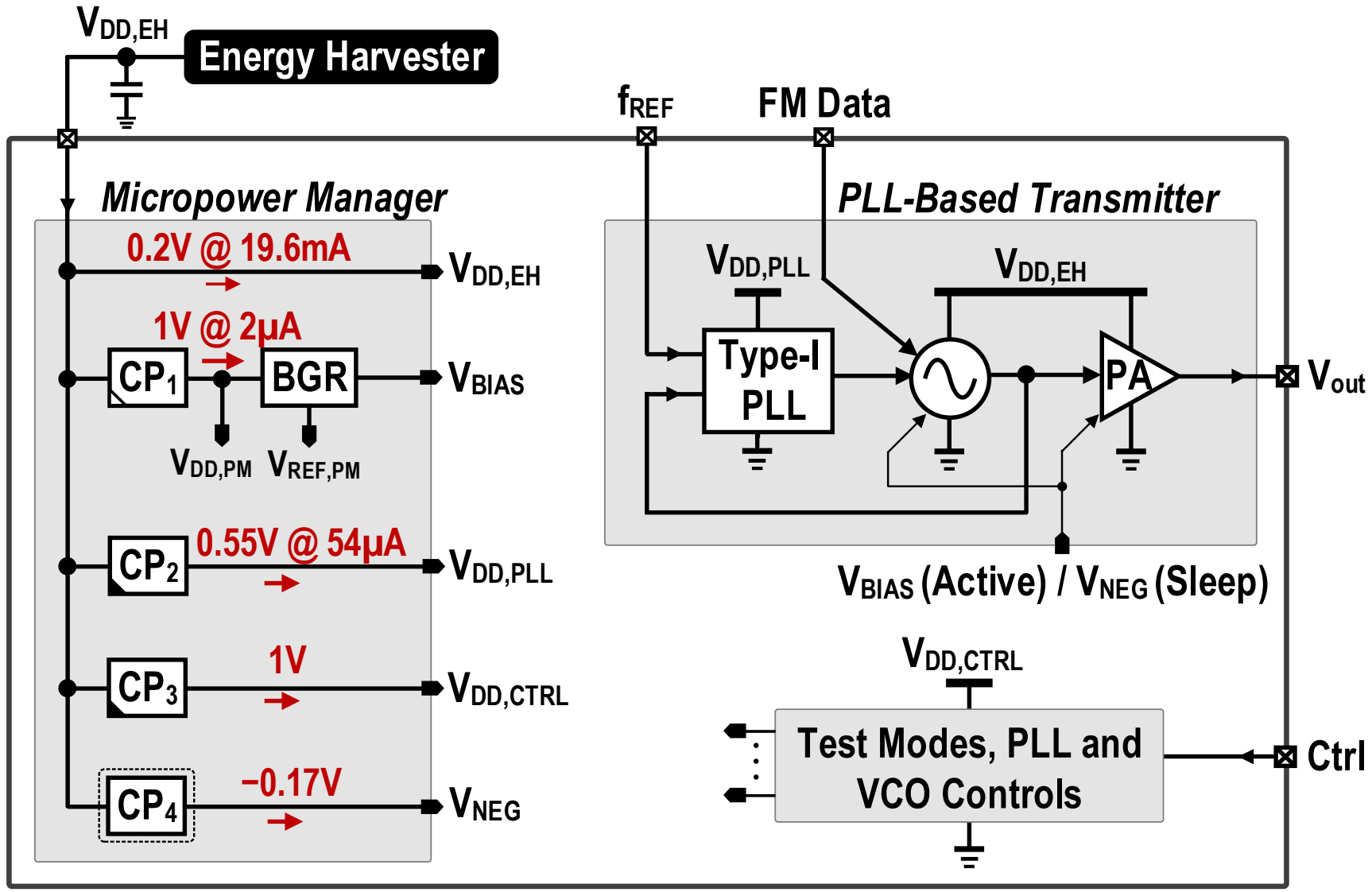


If $I_{LOAD1} >> I_{LOAD2}$

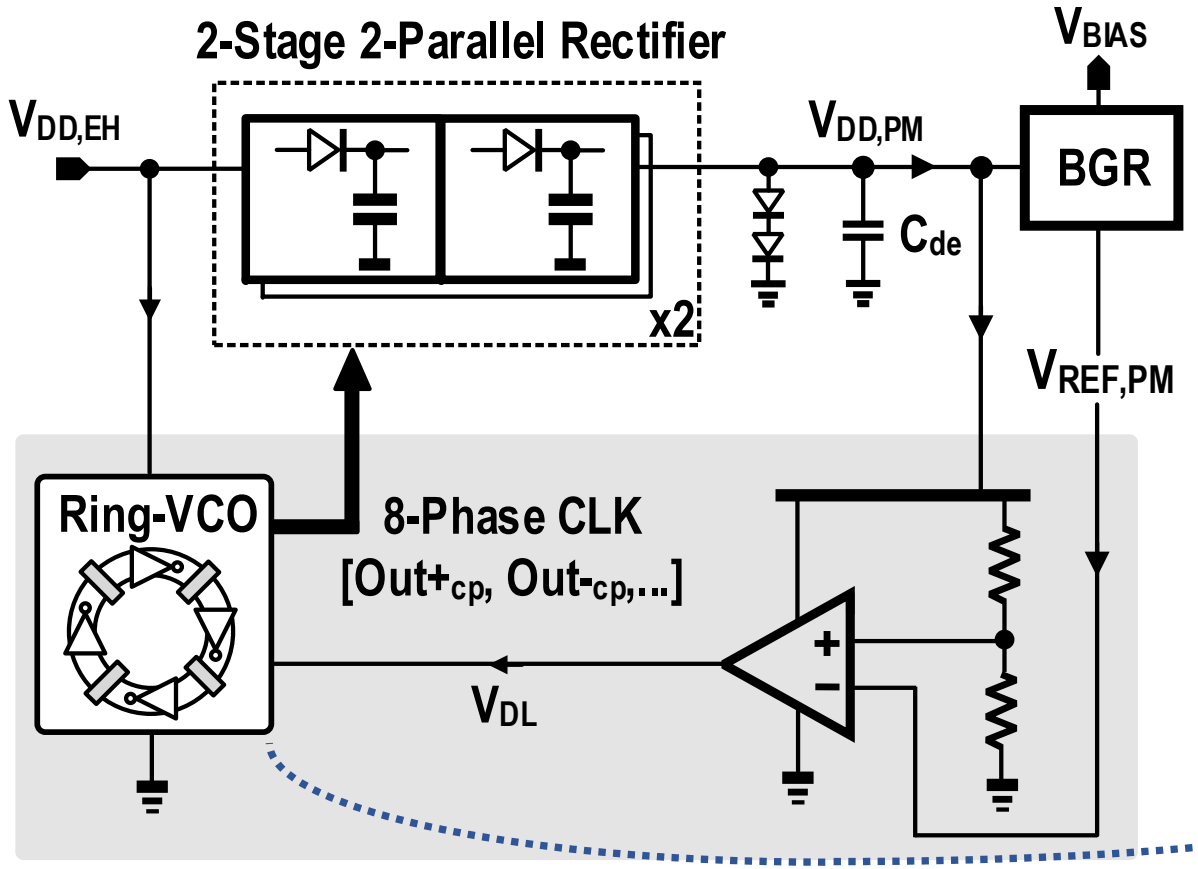
$$\eta_{sys} \approx \eta_{TX}$$

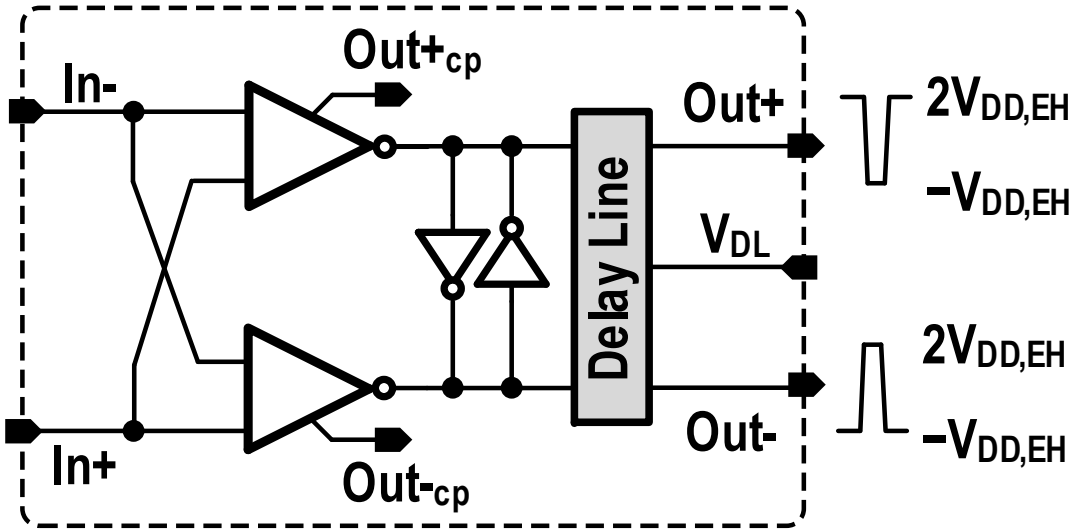
Proposed ULV BLE Transmitter

- 99% of power is directly provided by $V_{DD,EH}$
- CP_1 – CP_4 serve all internal bias and supplies for PLL and mode control



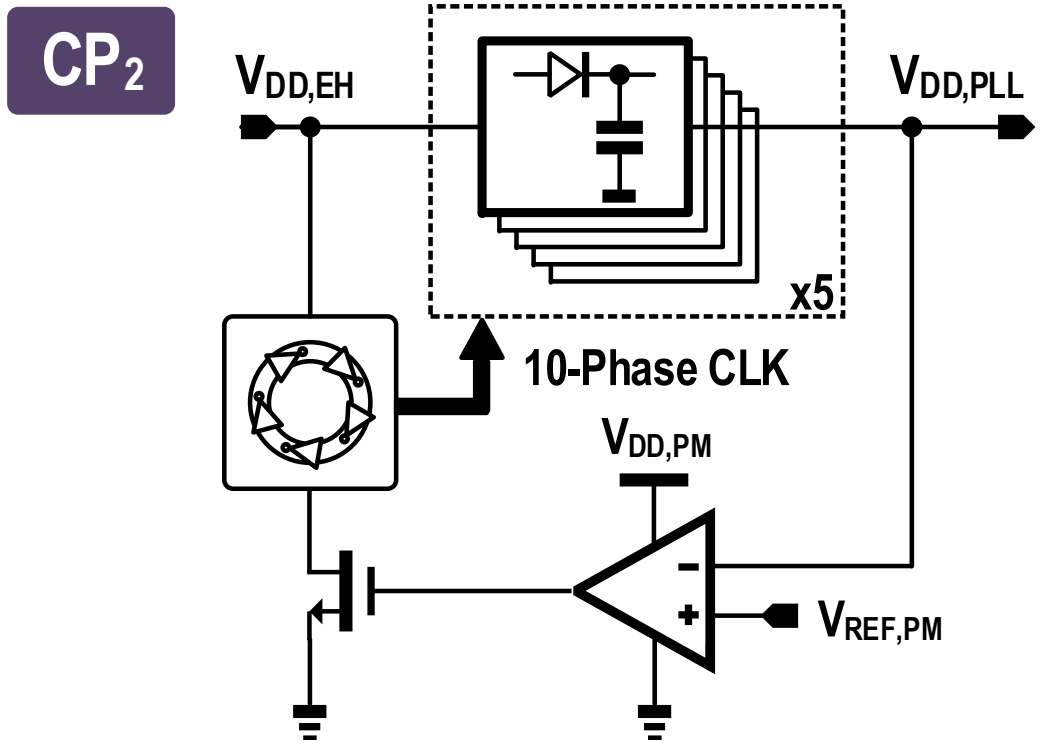
Micropower Manager (CP_1)

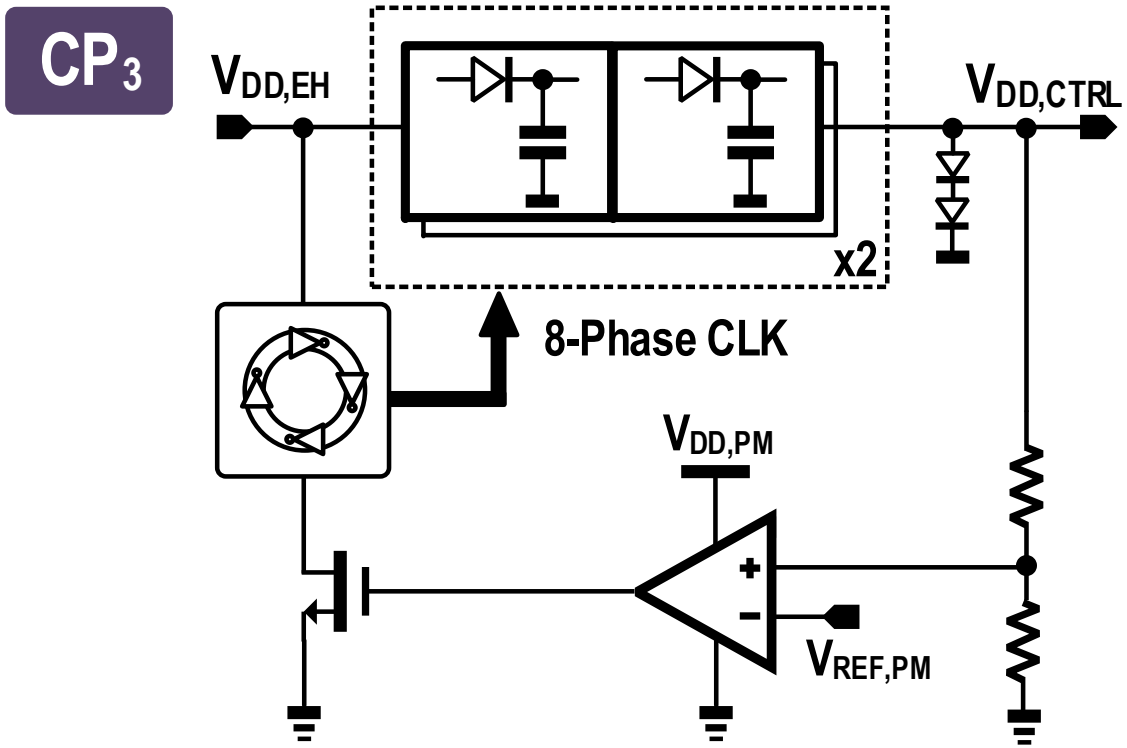




- $V_{DD,PM}$ and Power consumption are regulated by controlling the frequency (O/P swing) of the bootstrapped ring-VCO
- Multi-phase clock to reduce the switching ripple at $V_{DD,PM}$

Micropower Manager (CP_{2-3})

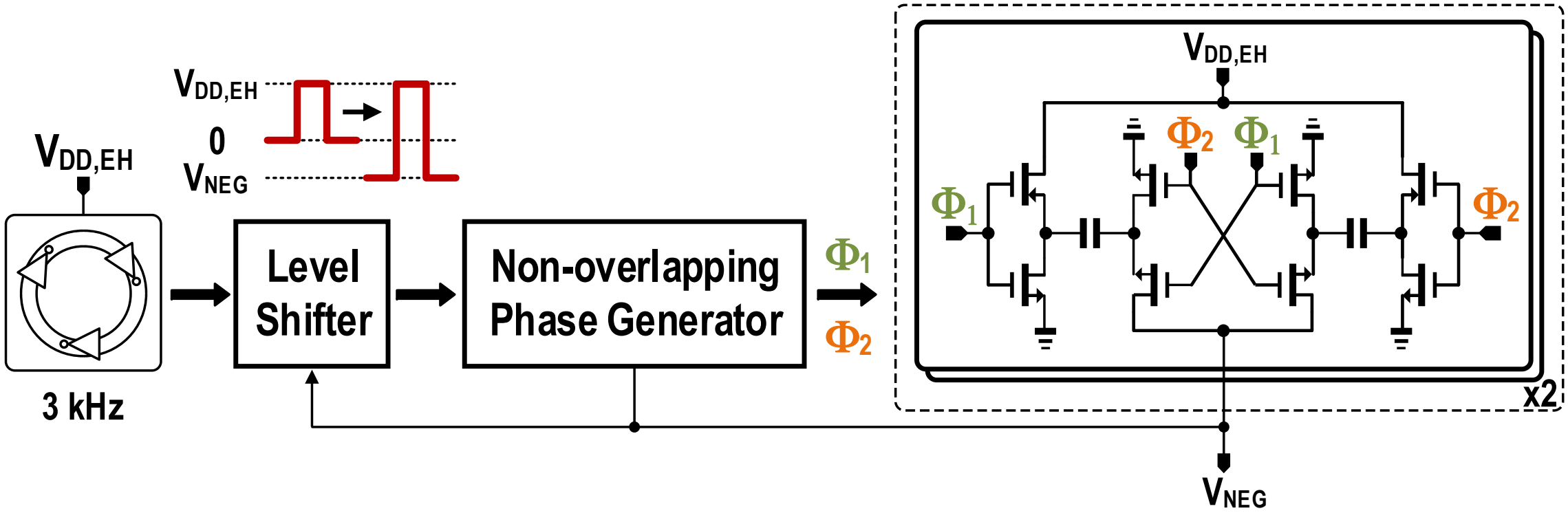




[W.-H. Yu et. al., ISSCC'17]

- $V_{DD,PLL}$ & $V_{DD,CTRL}$ are regulated by controlling the bias current (frequency and O/P swing) of the ring-VCOs

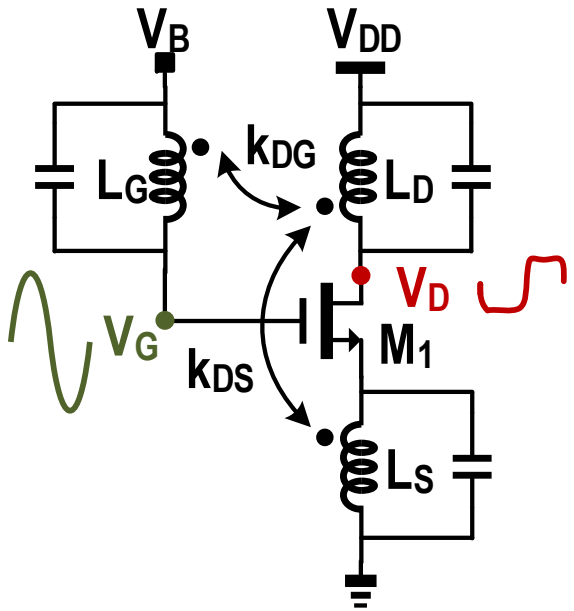
Proposed Always-On CP_4 for Negative Voltage



- The leakage current of VCO and PA is reduced from 2.58μA (V_{NEG}= 0V) to 27nA (V_{NEG}= −0.17V)

ULV VCO – Prior Art

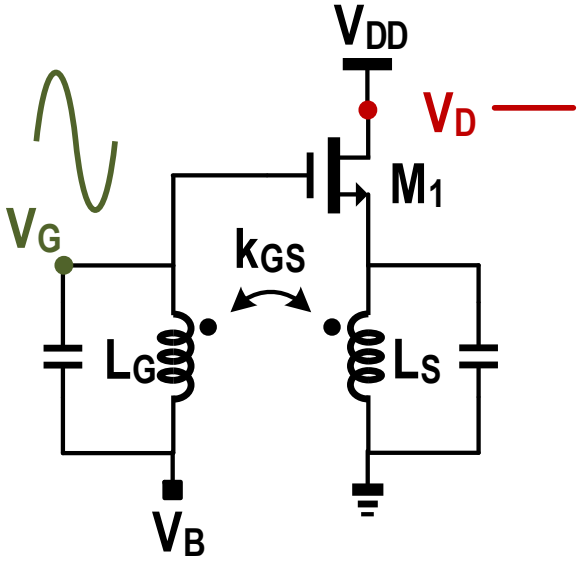
Trifilar-Coil VCO

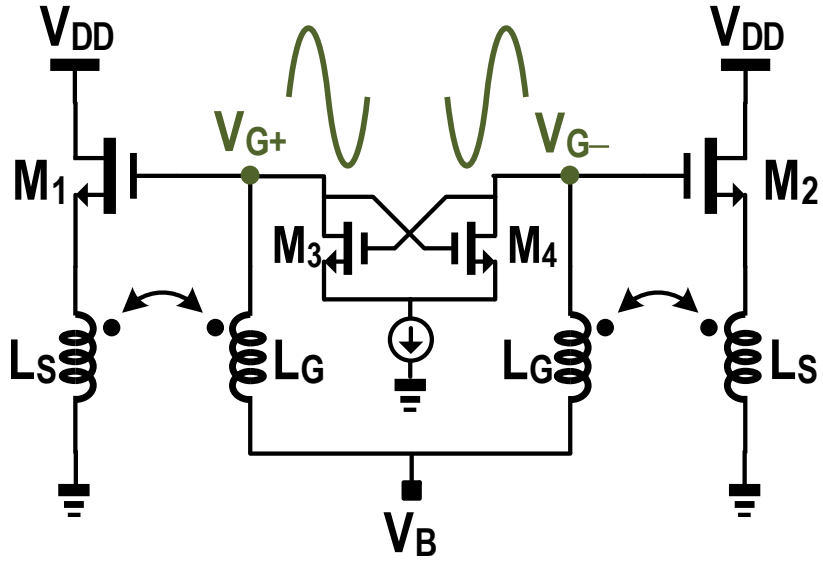


[C. –C. Li et. al., ISSCC'17]

- Trifilar-Coil DCO
  - ☺ Large loop gain, good phase noise, low frequency pushing
  - ☹ M_1 enters deep triode region at low V_{DD}

Gate-to-Source Feedback VCO

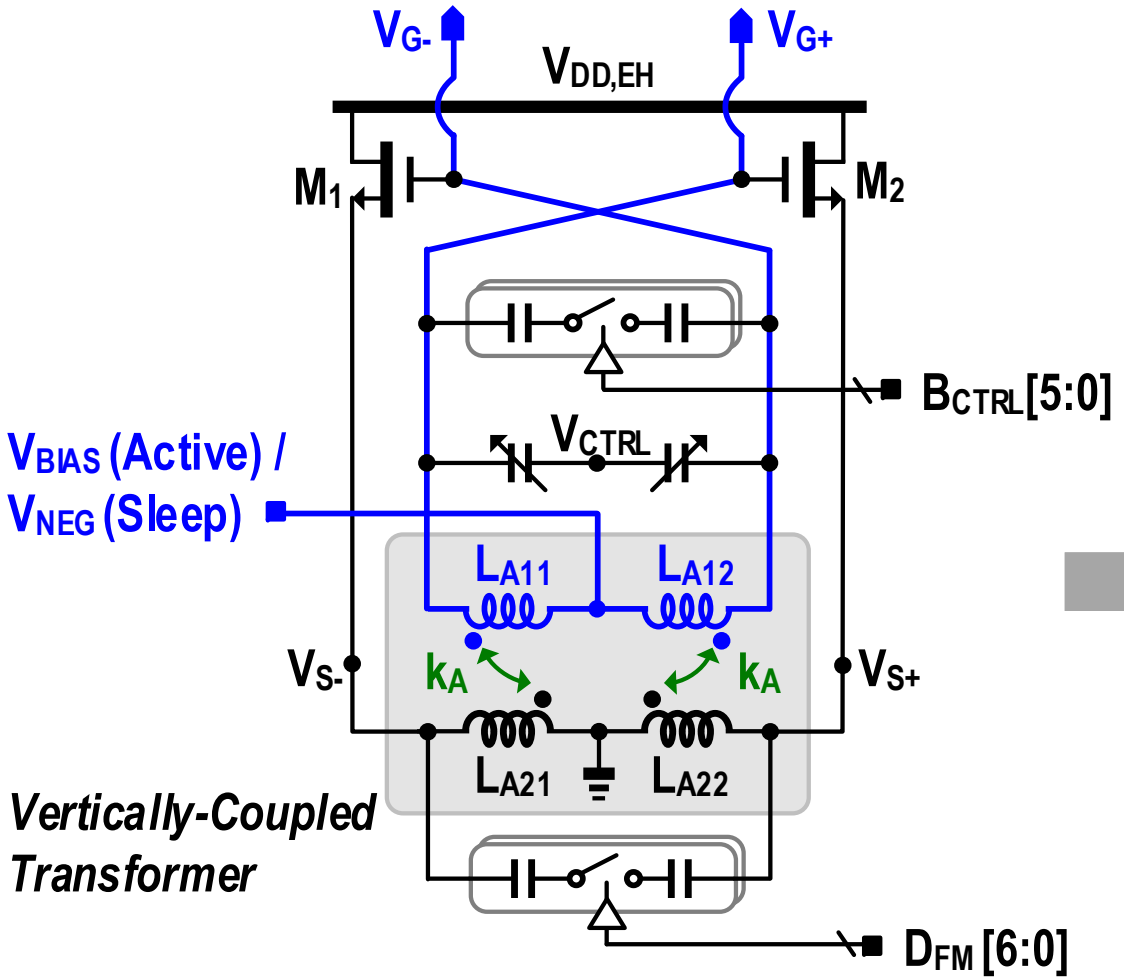


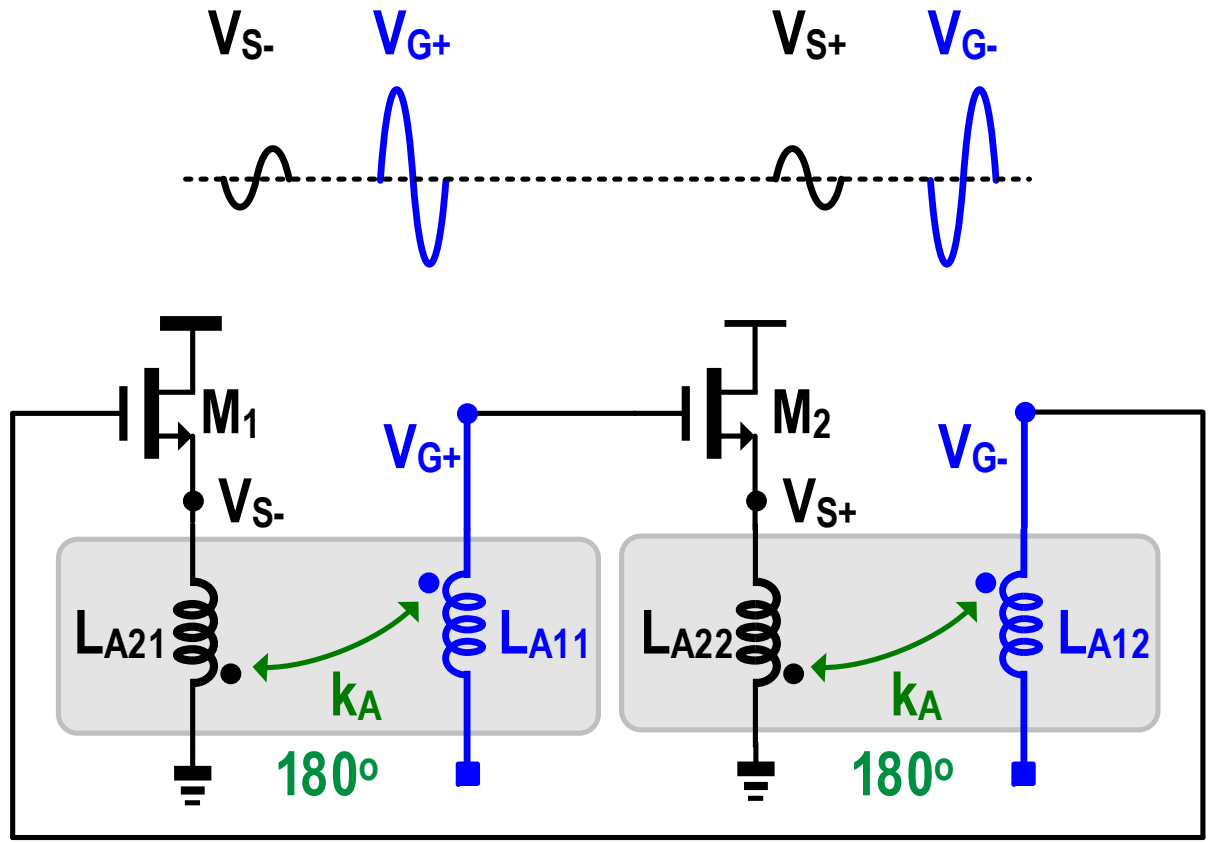


[A. W. L. Ng et. al., JSSC'06]

- Gate-to-Source Feedback DCO
  - ☺ Avoid $M_{1,2}$ into deep triode region at low V_{DD}
  - ☹ Static current at the bias voltage V_B

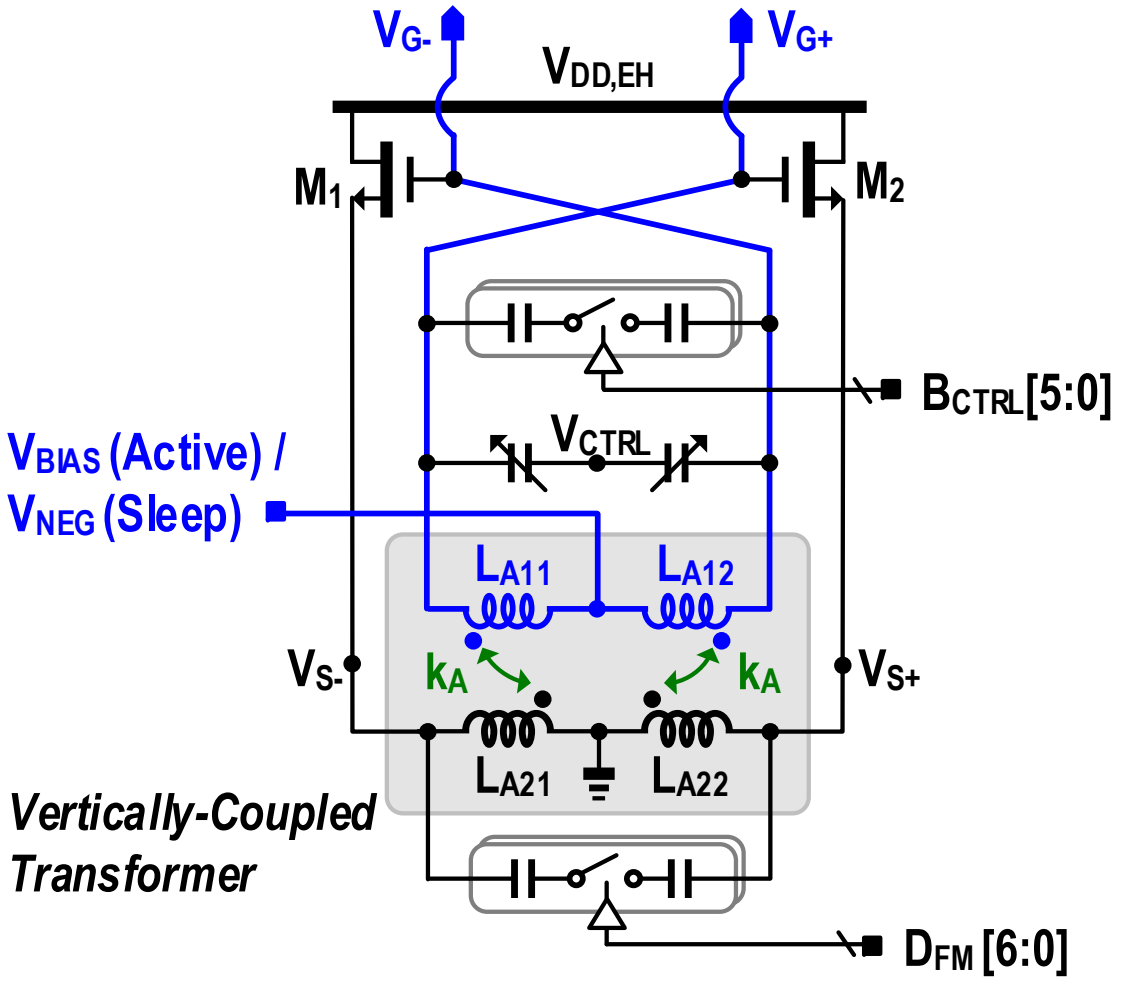
Proposed Diff. Gate-to-Source-Feedback VCO [1]

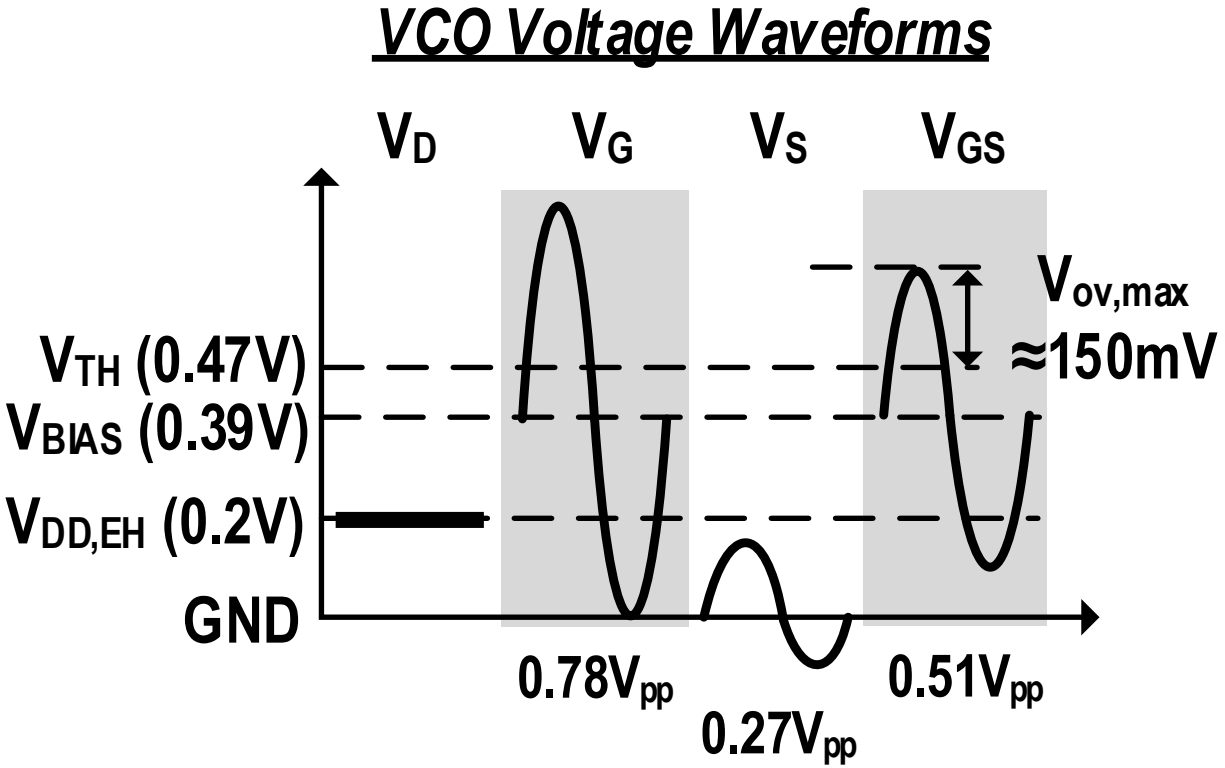




- Gate-to-source cross-coupling together with the transformer coupling to balance the differential outputs

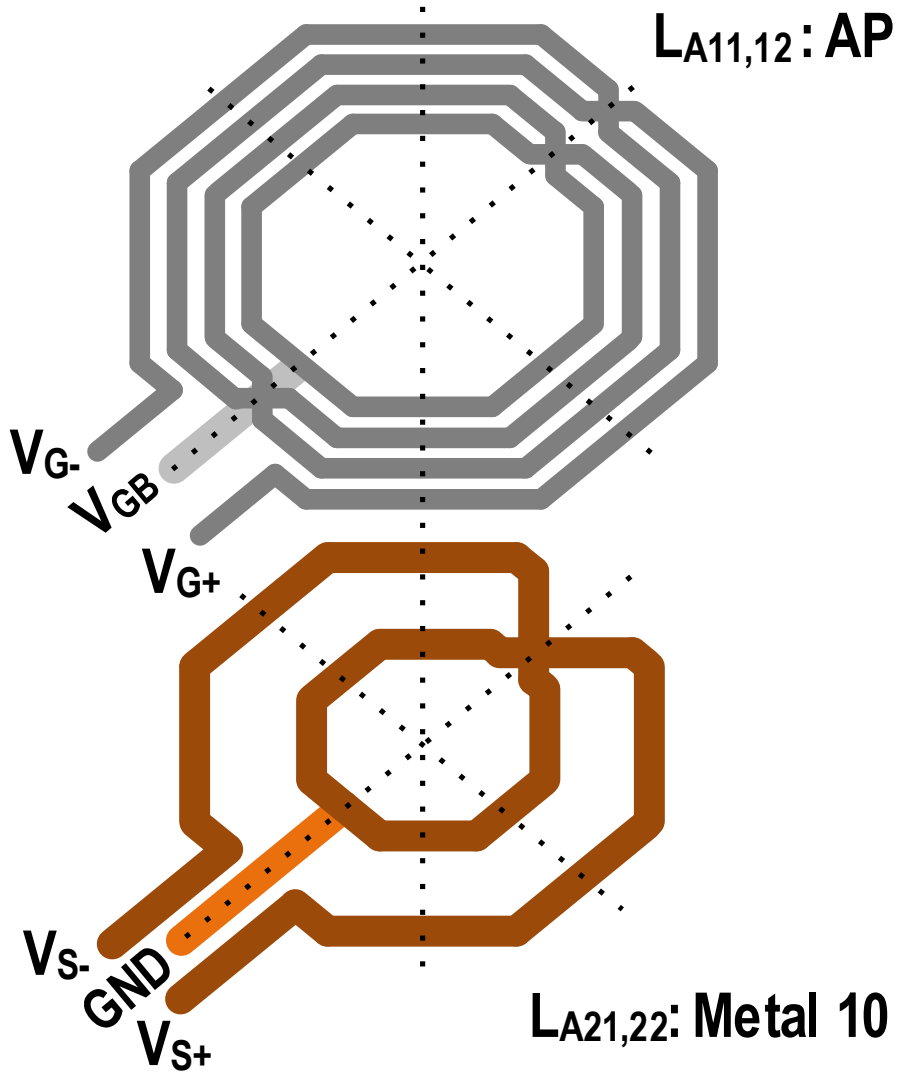
Proposed Diff. Gate-to-Source-Feedback VCO [2]





- $M_{1,2}$ is prevented from entering deep triode region

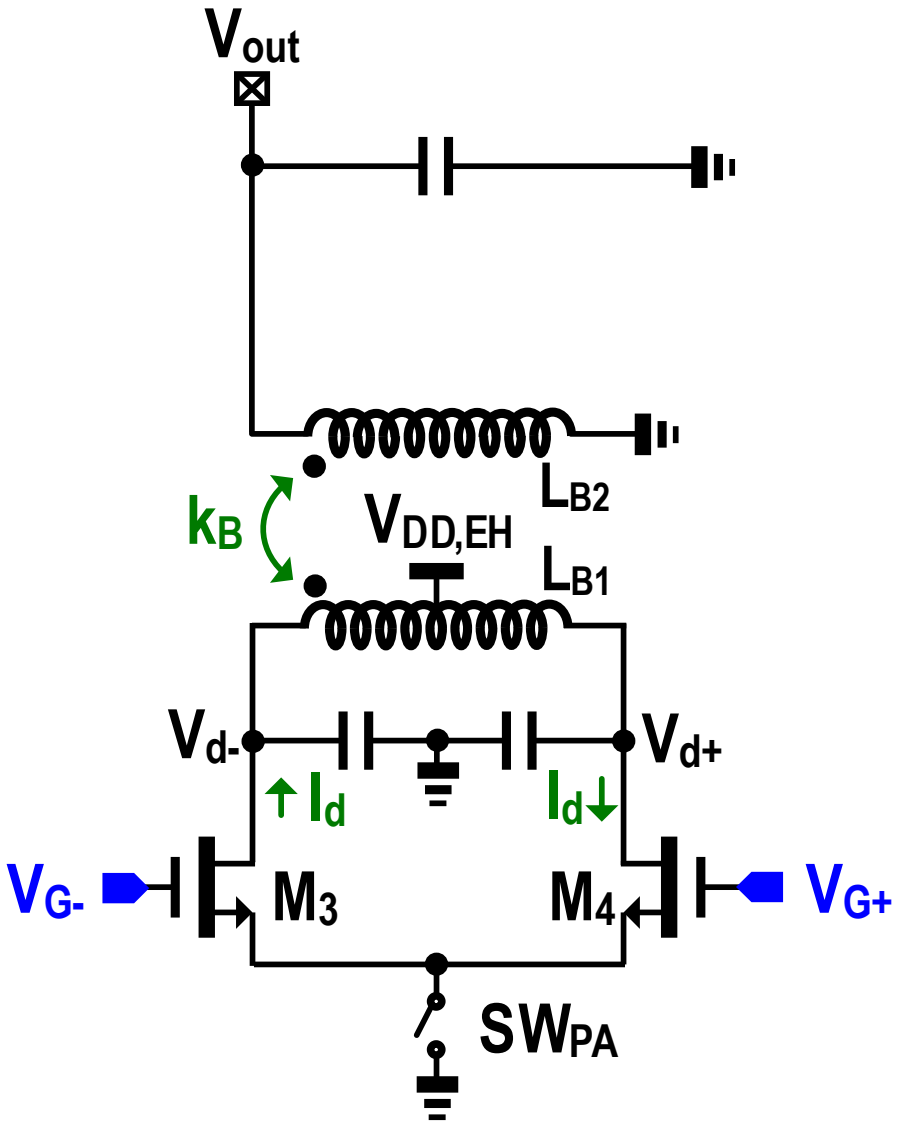
VCO Transformer Design



$$\text{Loop Gain: } A_{loop} \approx \frac{g_m k_A N_{GS}}{1 + g_m |Z_s|}$$

- Large $|Z_s|$ (L_{A21}) helps boosting $|V_G|$ but degrades A_{loop}
- Stacked transformer helps keeping a large A_{loop} by increasing k_A (≈0.76) even at a large turn-ratio N_{GS} ($=\sqrt{L_{A11}/L_{A21}}=5.6$)

ULV Class-E/F_2 PA



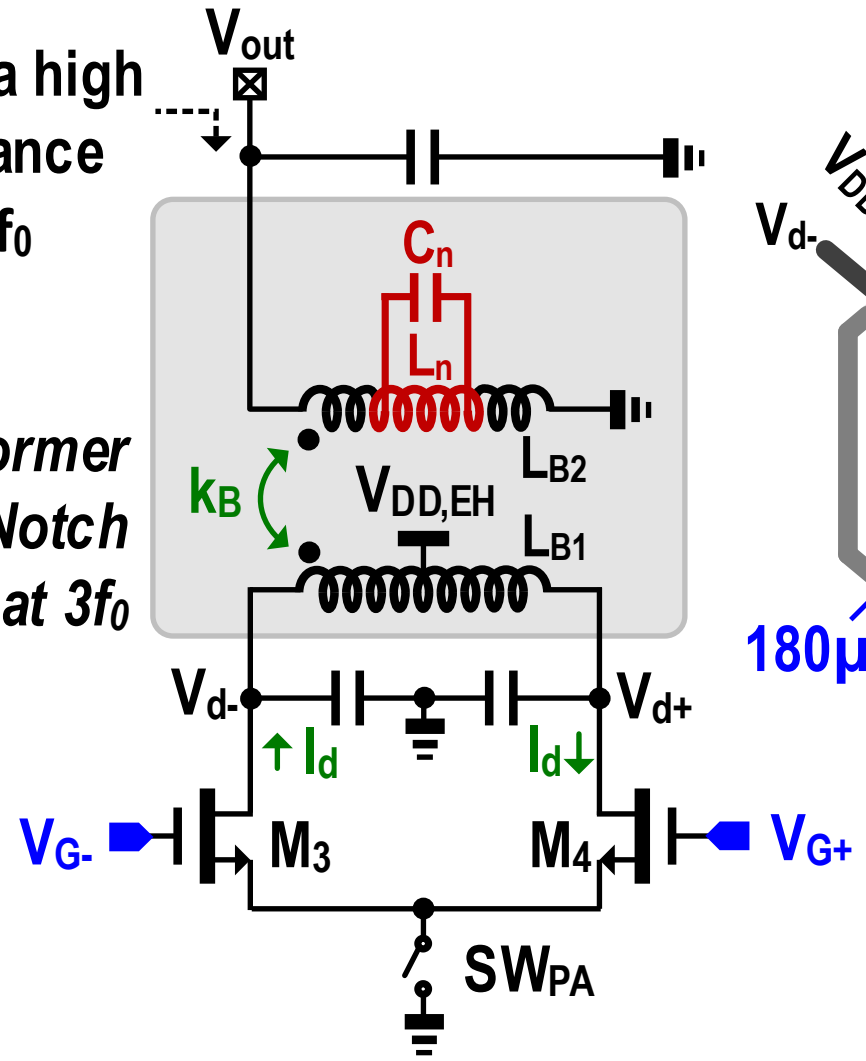
- Directly driven by the VCO
- Differential Class-E/F_2 PA for high output power and efficiency

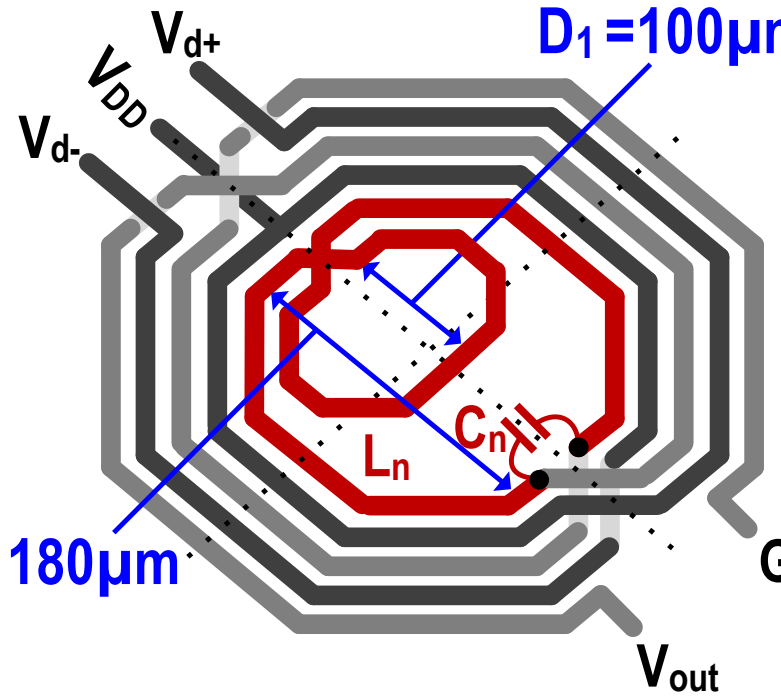
  [M. Babaie et. al., JSSC 2016]
- Low HD_2
- SW_{PA} for power down (e.g. switch to the receiver mode)
- **How about HD_3?**

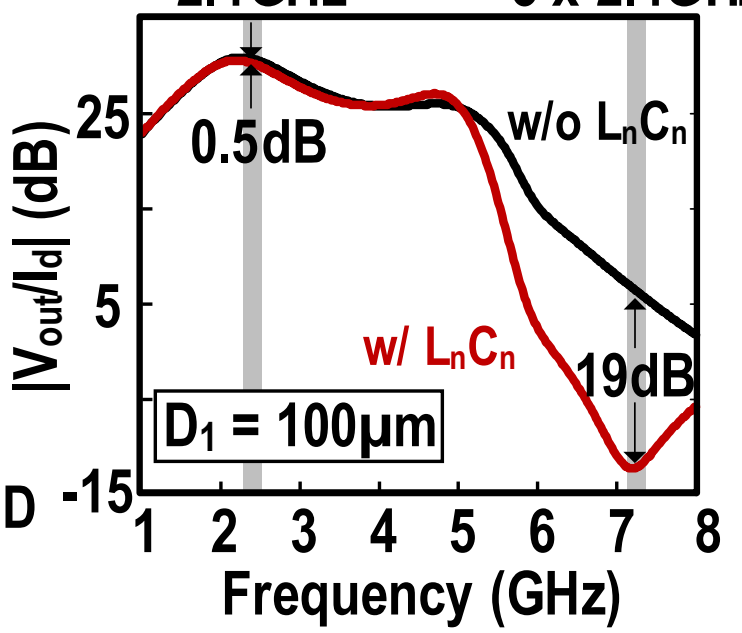
Proposed Inside-Transformer HD_3 Suppression Technique

Z_{22} with a high impedance at $3f_0$

Transformer w/ L_nC_n Notch at $3f_0$

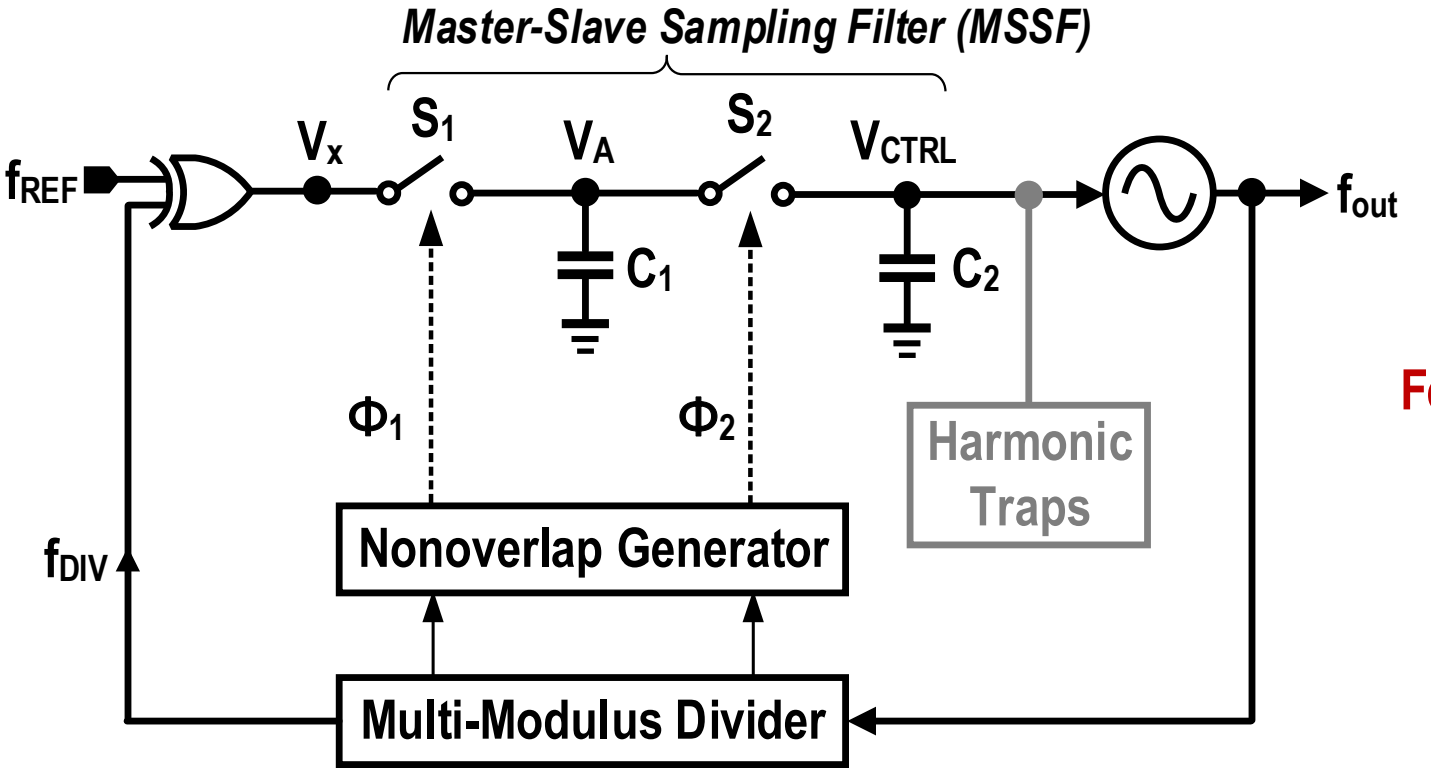


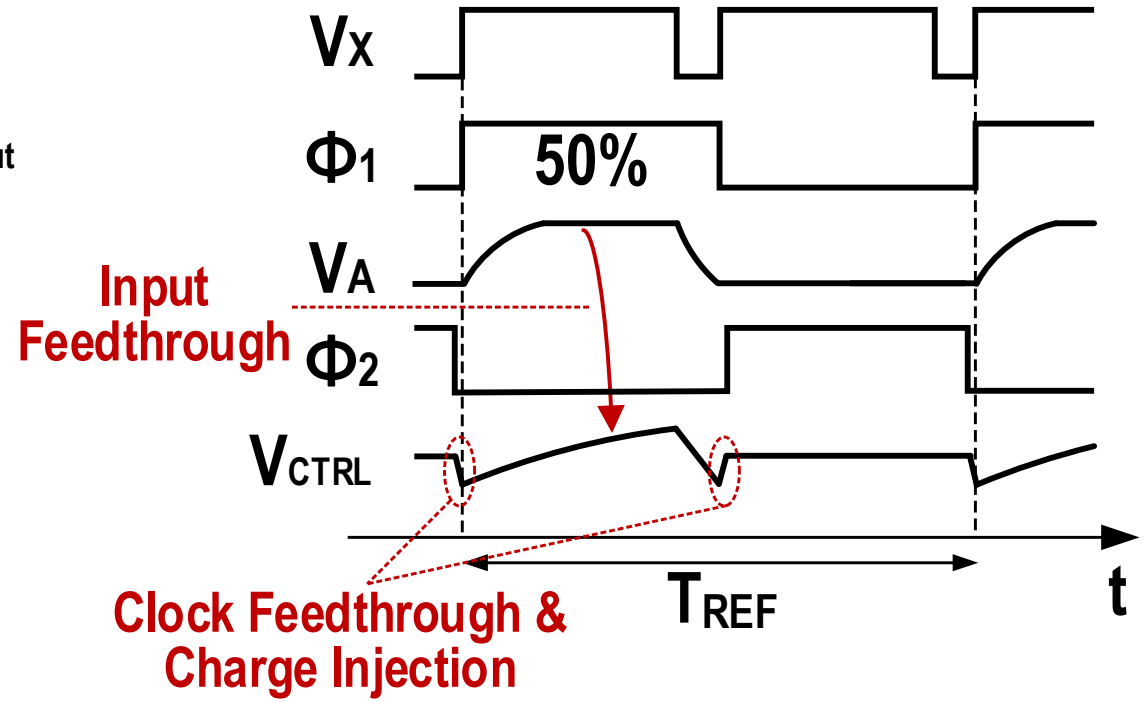




➢ Simulated HD_3 is improved by 19dB

Analog Type-I PLL [K. Long et. al., JSSC'16]

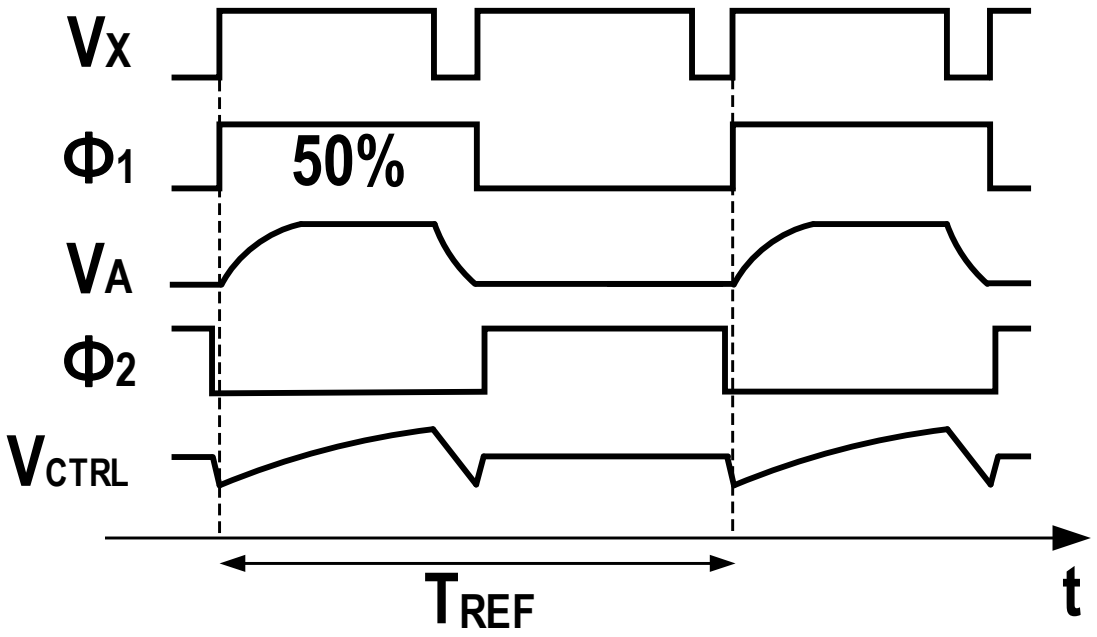




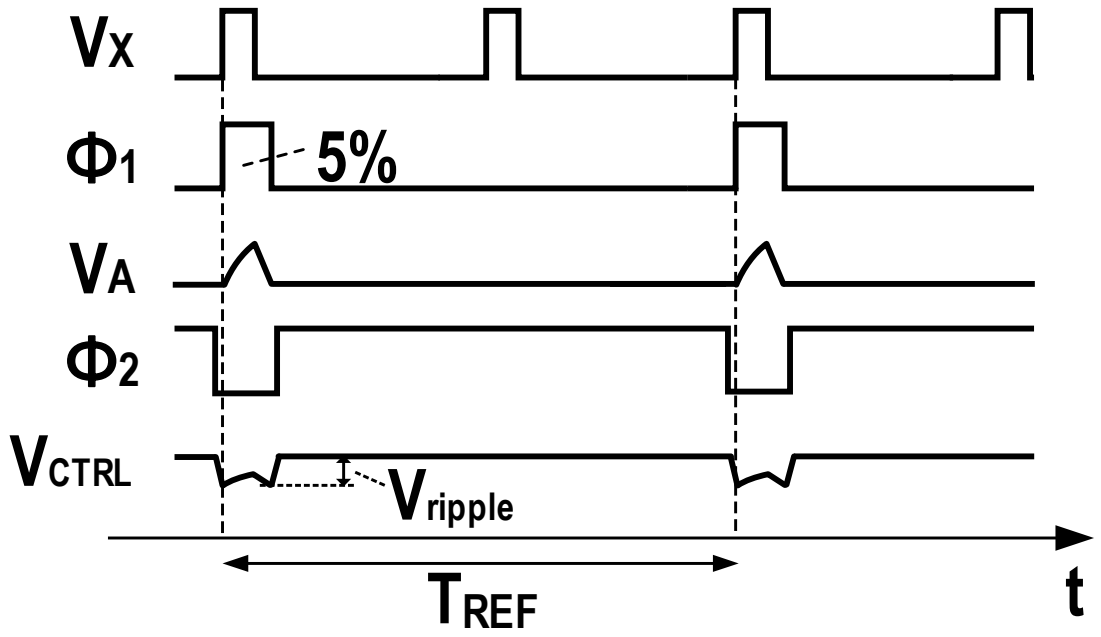
- Type-I PLL with Master-Slave Sampling Filter (MSSF)
  - Low power and small area (small C_1 and C_2)
  - Spur limited by non-ideal behavior of switch S_2

Proposed REF Spur Suppression Technique

50% Duty Cycle (α_{DC}) of Φ_1



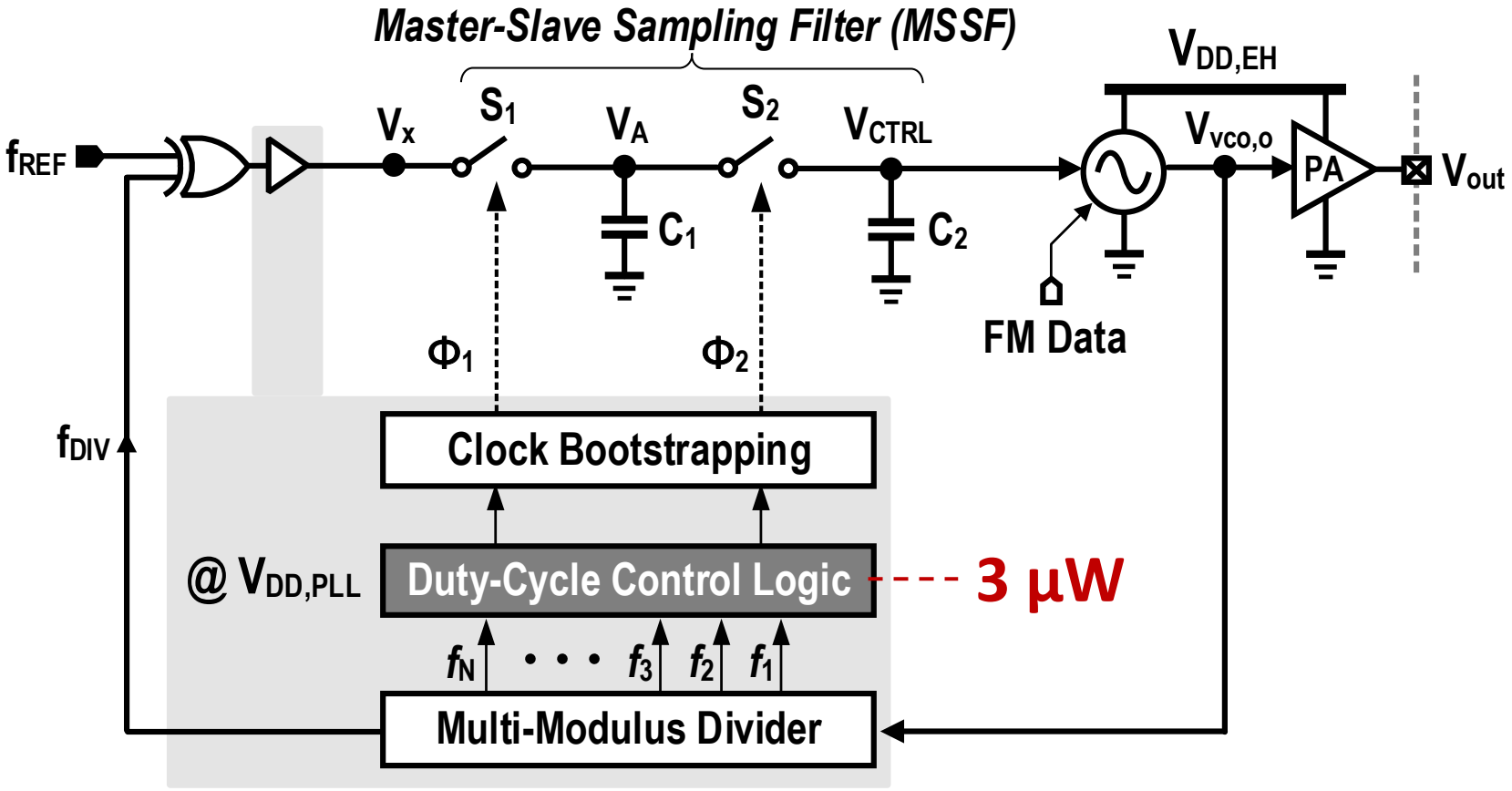
5% Duty Cycle (α_{DC}) of Φ_1

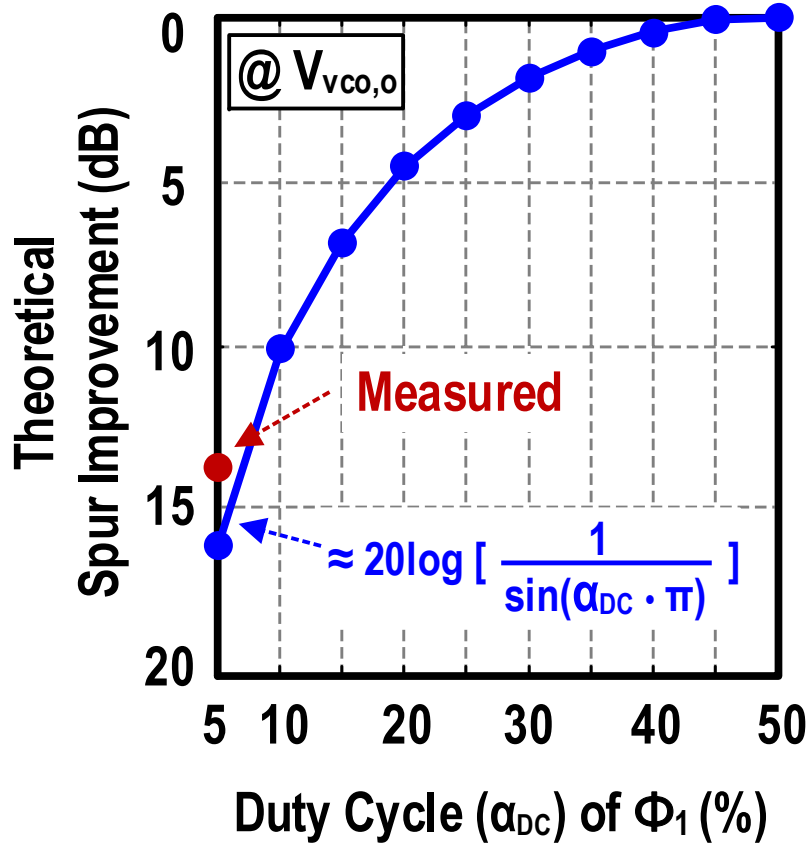


$$\text{1st harmonic Fourier Coefficient of } V_{CTRL} \approx V_{ripple} \cdot \frac{2}{\pi} \cdot \sin(\alpha_{DC} \cdot \pi)$$

- Small duty-cycle (α_{DC}) of Φ_1 helps suppressing the REF spur

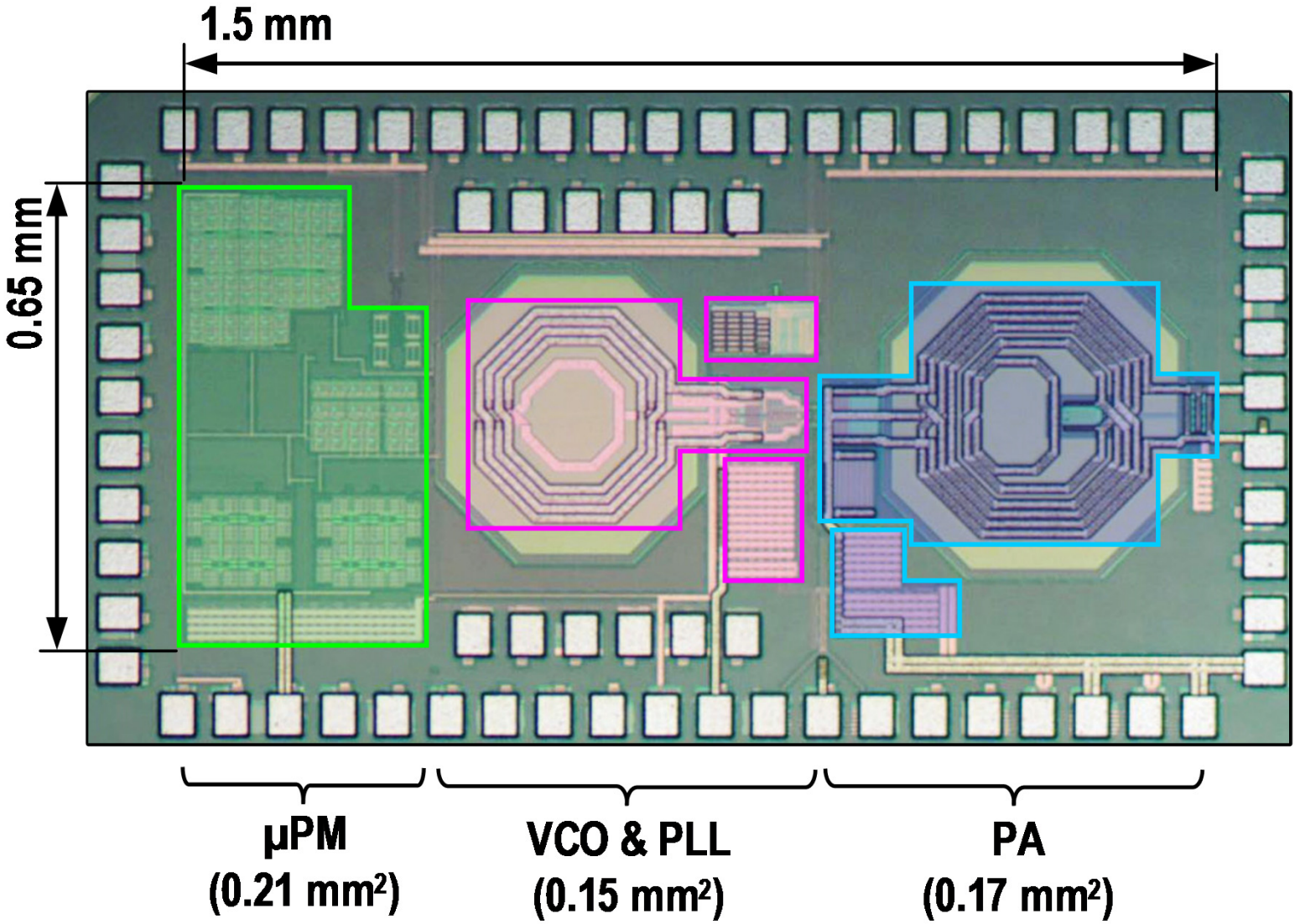
ULV Analog Type-I PLL with a Reduced Duty-Cycle Φ_1





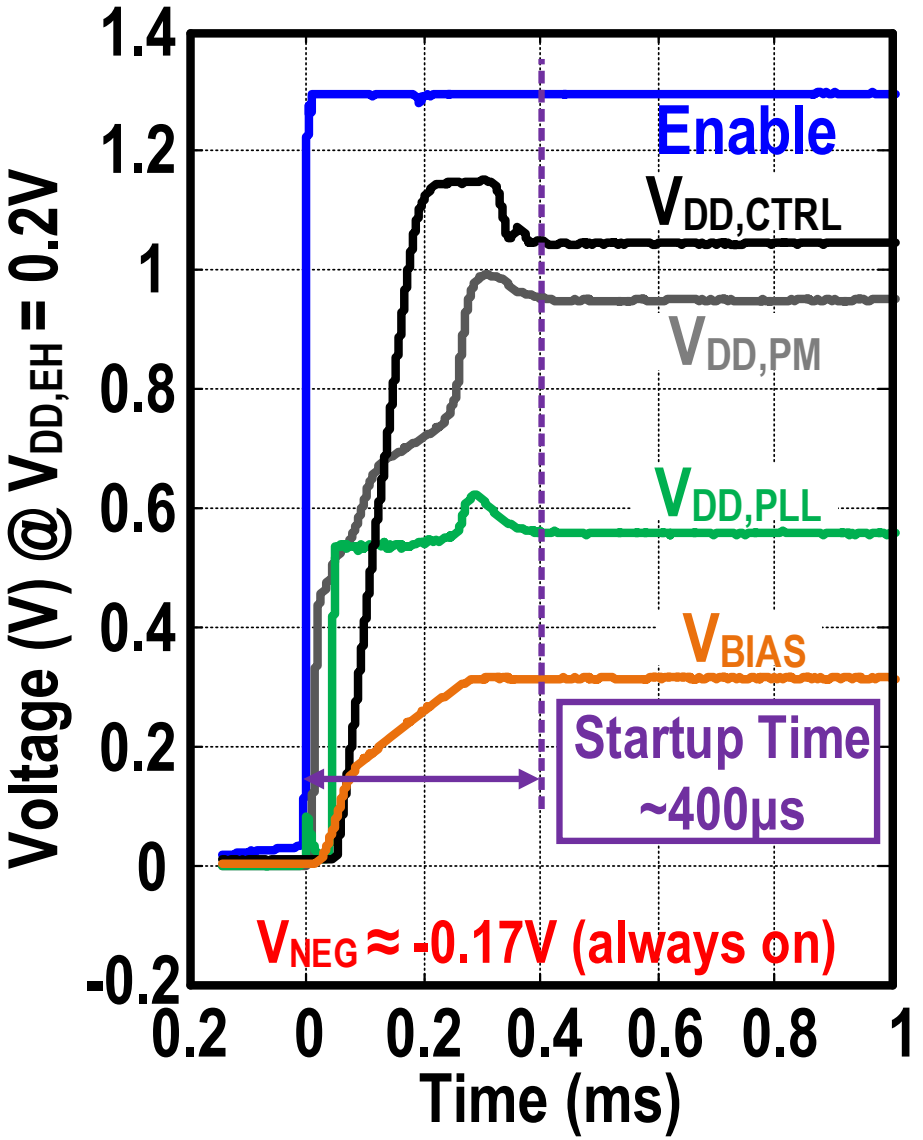
- Spur reduction tradeoffs the settling time
- 5% duty-cycled clocks are generated by utilizing high-frequency outputs of multi-modulus divider → negligible power overhead

Chip Microphotograph

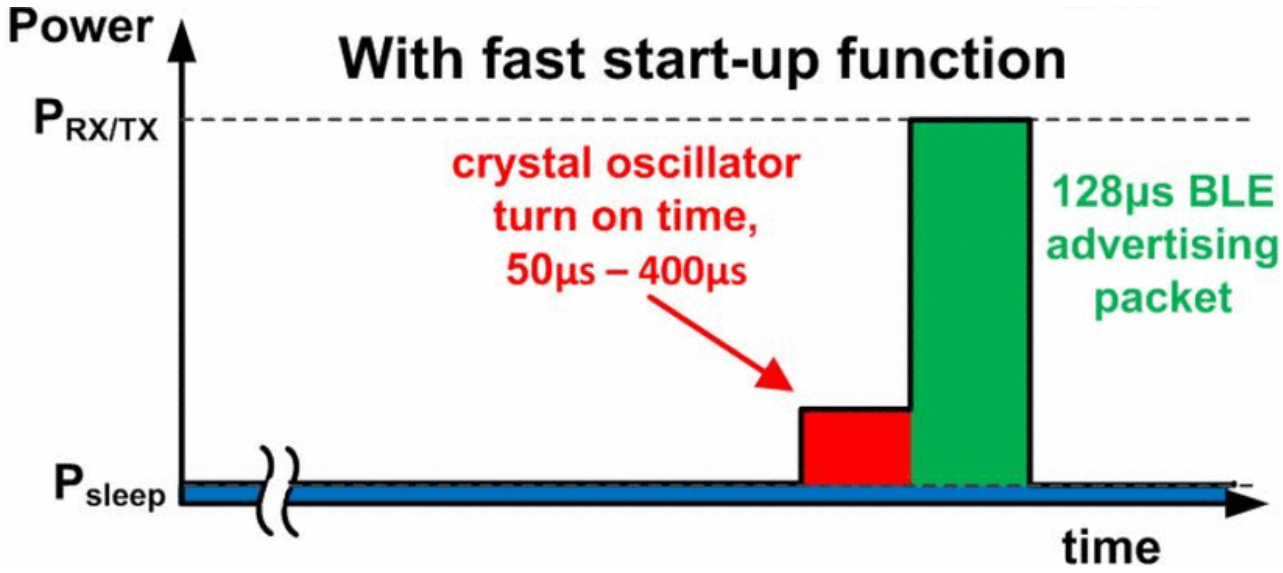


- 28nm Standard CMOS
- Met all density rules
- Active area: 0.53mm^2

Startup of the Micropower Manager

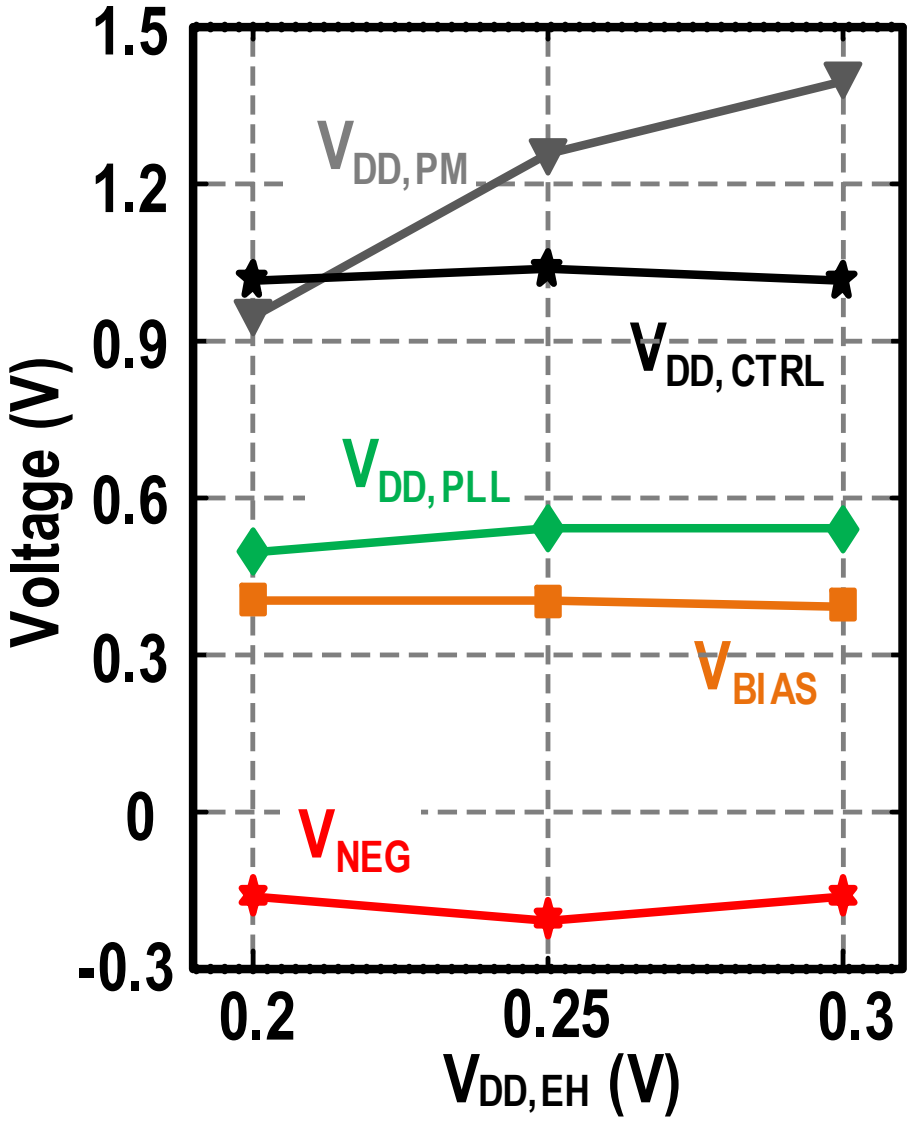


- The startup time can be overlapped with the state-of-the-art BLE crystal oscillator: <u>50 to 400µs</u>



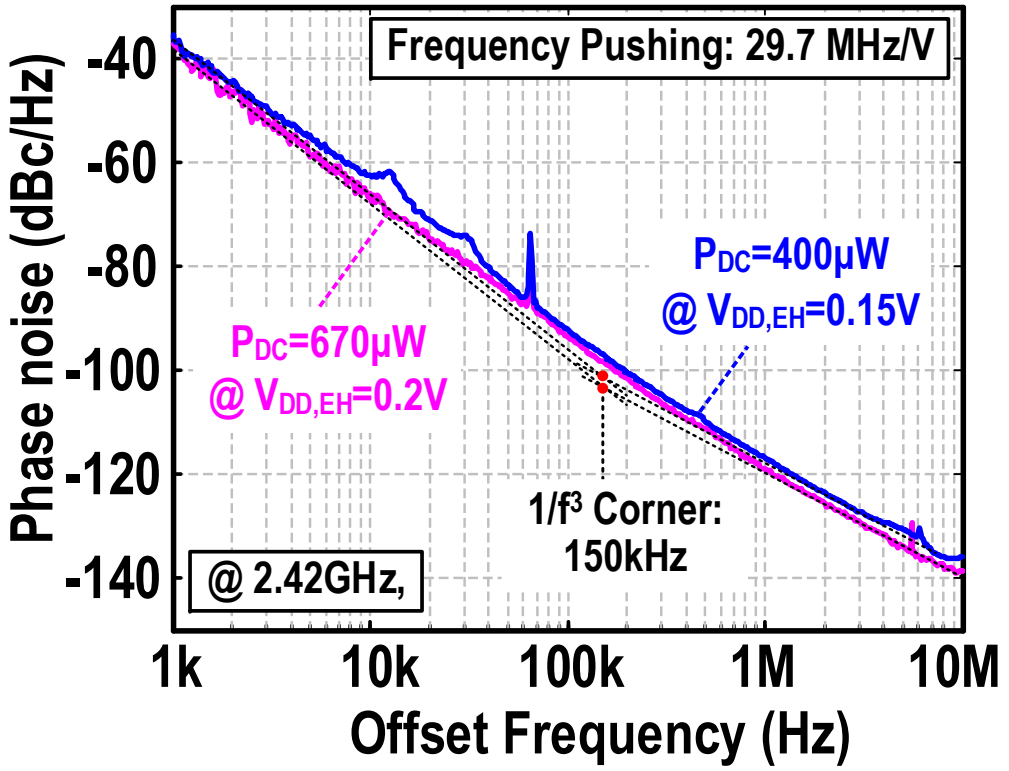
[D. Griffith, et al., ISSCC'16]

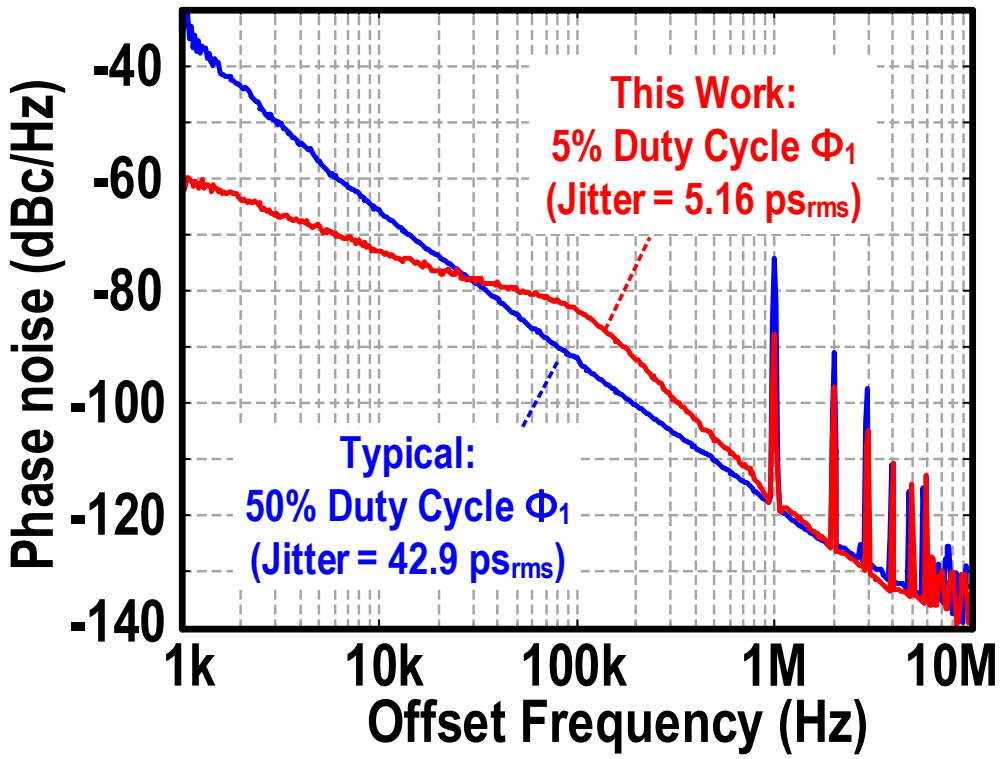
Output Voltages against $V_{DD,EH}$ (0.2 → 0.3V)



- Limited Ring VCO tuning range in CP_1 → vary with $V_{DD,EH}$
- Locked Ring VCO in $CP_{2,3}$ → low sensitivity with $V_{DD,EH}$
- BGR output → lowest sensitivity
- V_{NEG}: −0.17 to −0.22 V

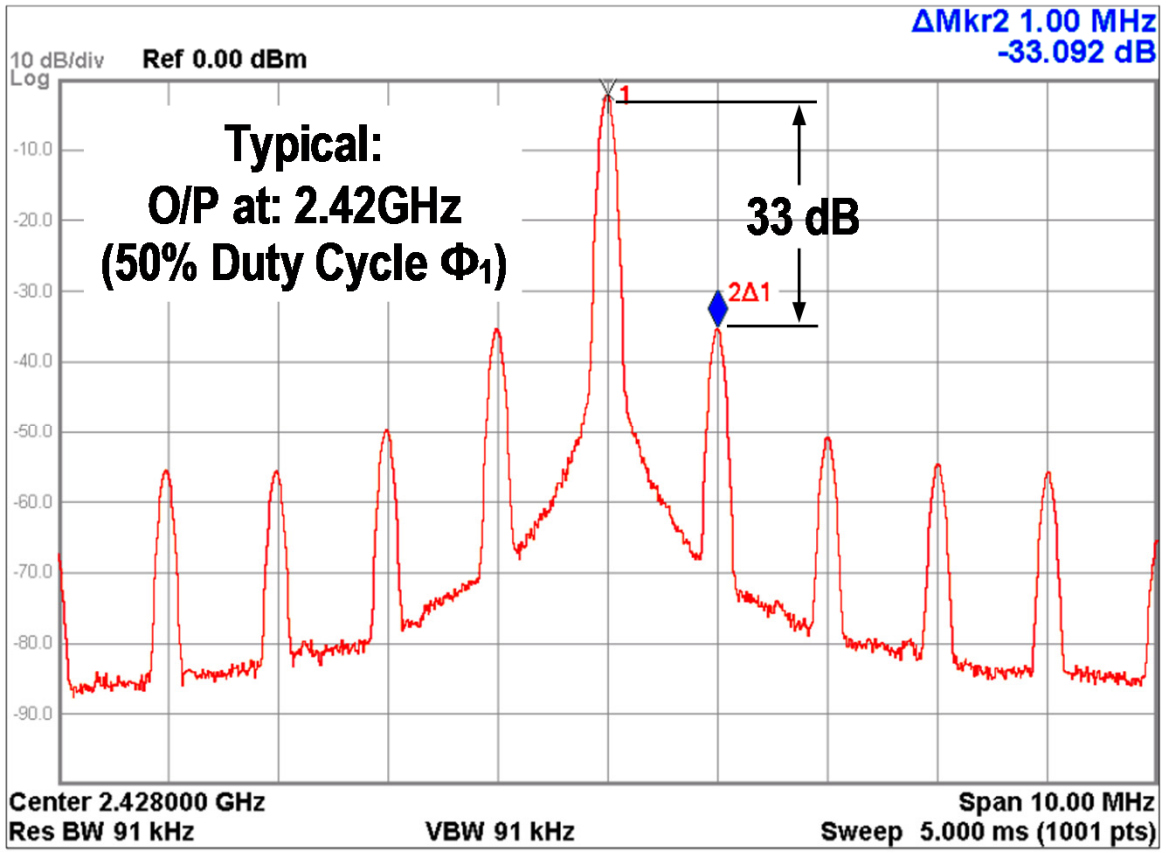
Phase Noise of Free-Running and PLL-locked VCO

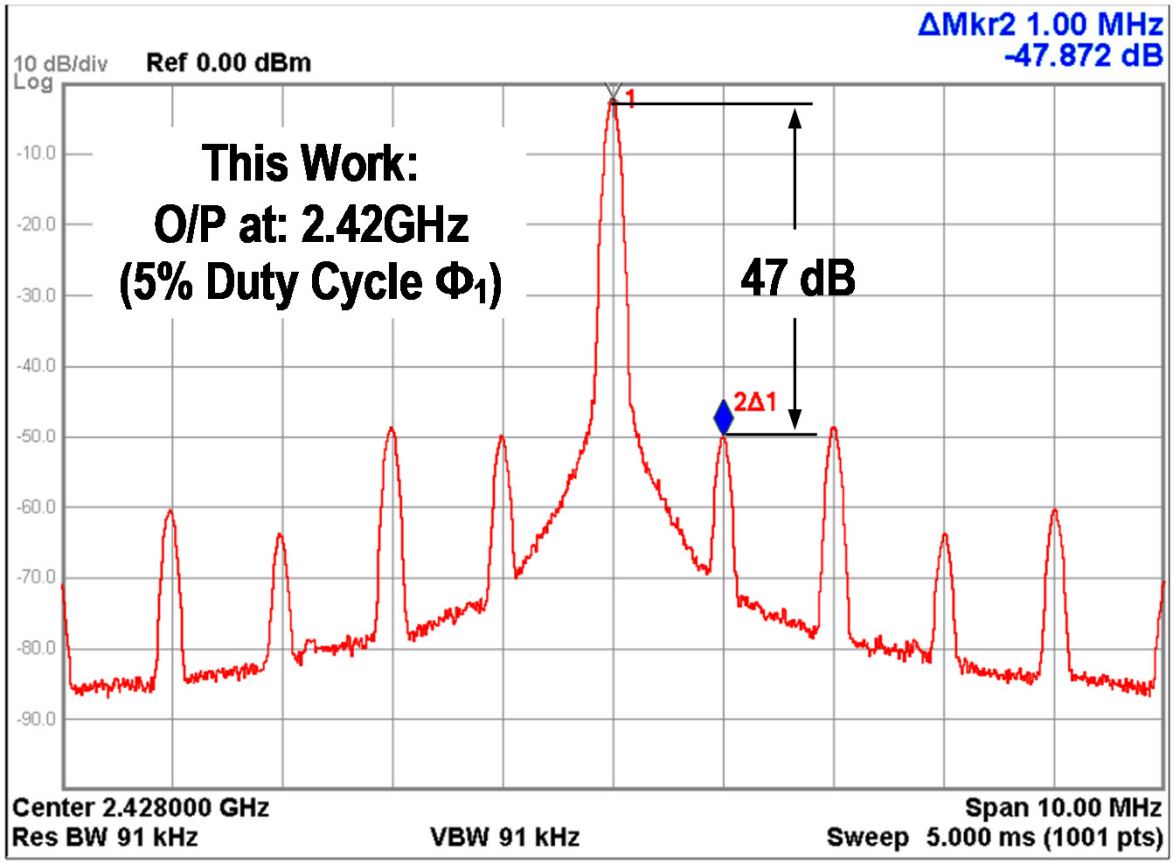




- VCO TR: 2.236~2.596GHz (14.9%)
- VCO phase noise@2.5MHz offset:
  - −127.7dBc/Hz @$V_{DD,EH}$ = **0.2V (670µW)**
  - −125.6dBc/Hz @$V_{DD,EH}$ = **0.15V (400µW)**
- Power of PLL loop: ~30µW
- PLL RMS Jitter:
  - 42.9ps @ **50%** duty cycle of Φ_1
  - 5.16ps @ **5%** duty cycle of Φ_1

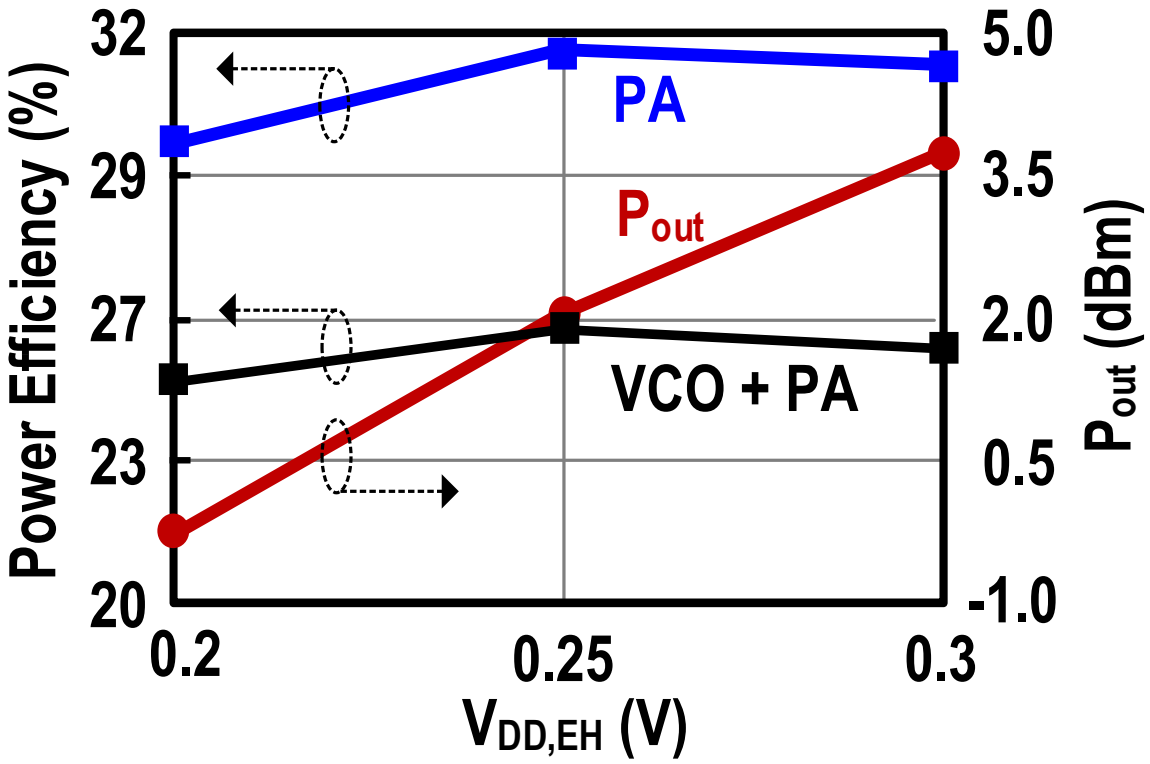
PLL Reference Spur and Settling Time

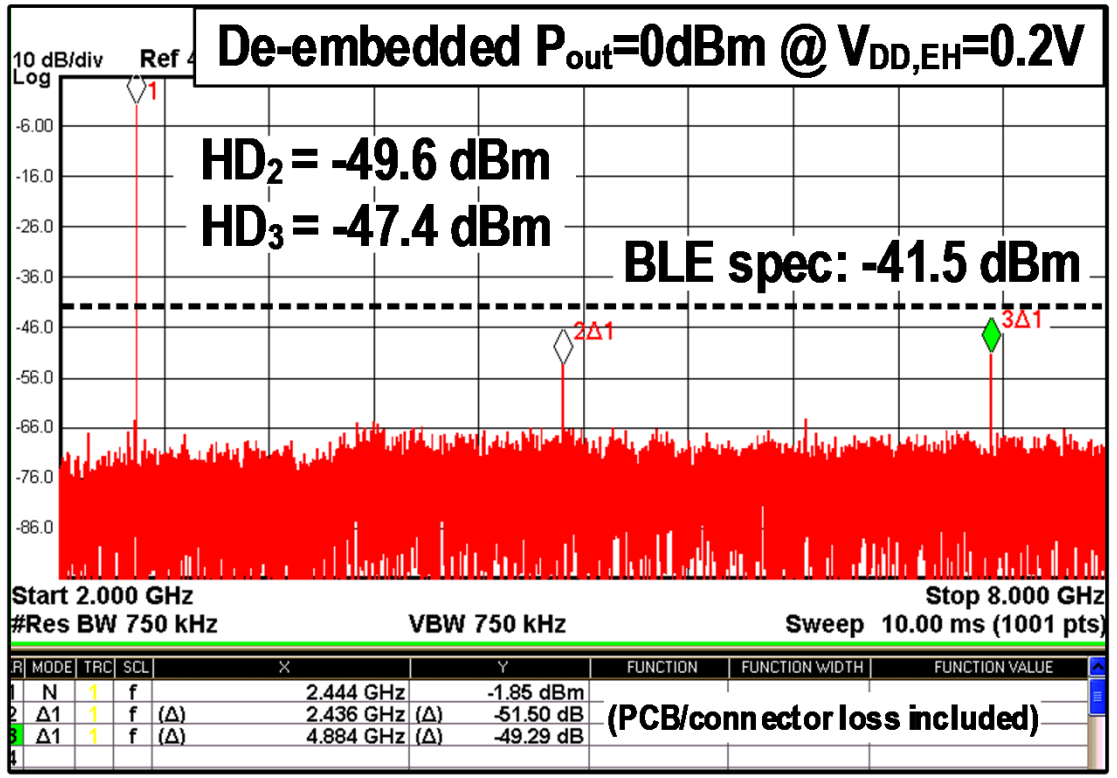




- PLL REF spur is reduced by 14dB
- PLL Settling time is ~30µs at an initial freq. offset of 30MHz

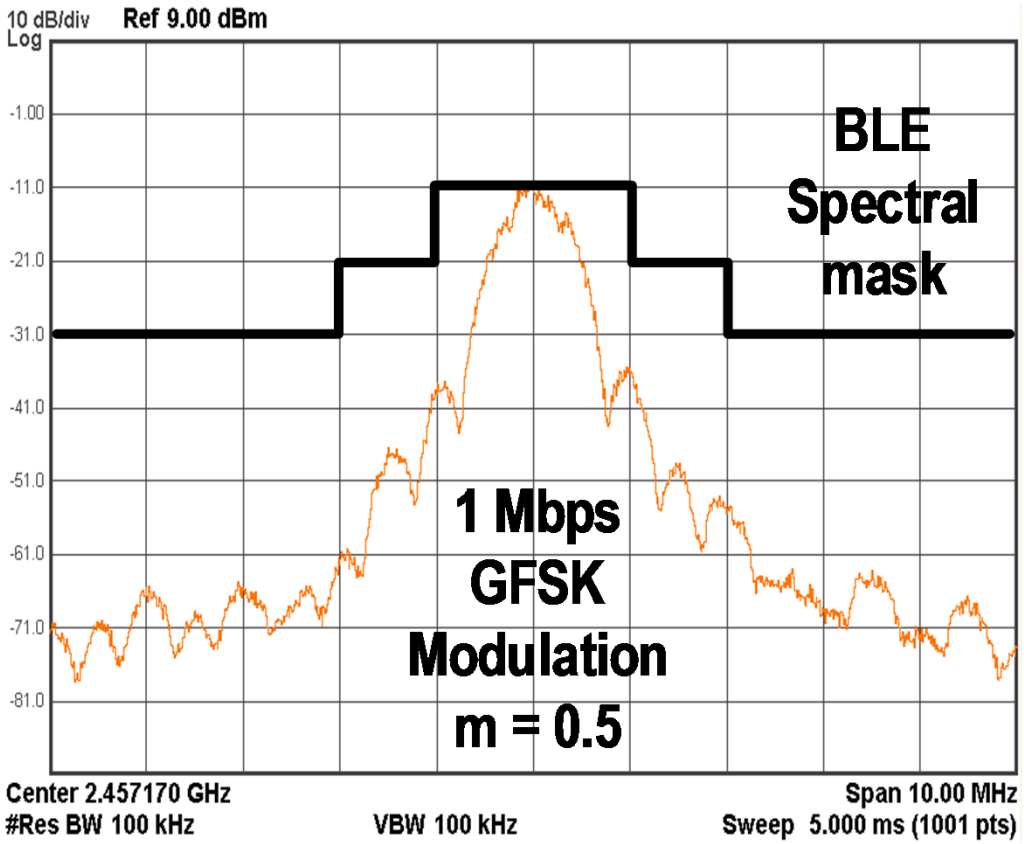
Power Efficiency and Harmonic Distortion

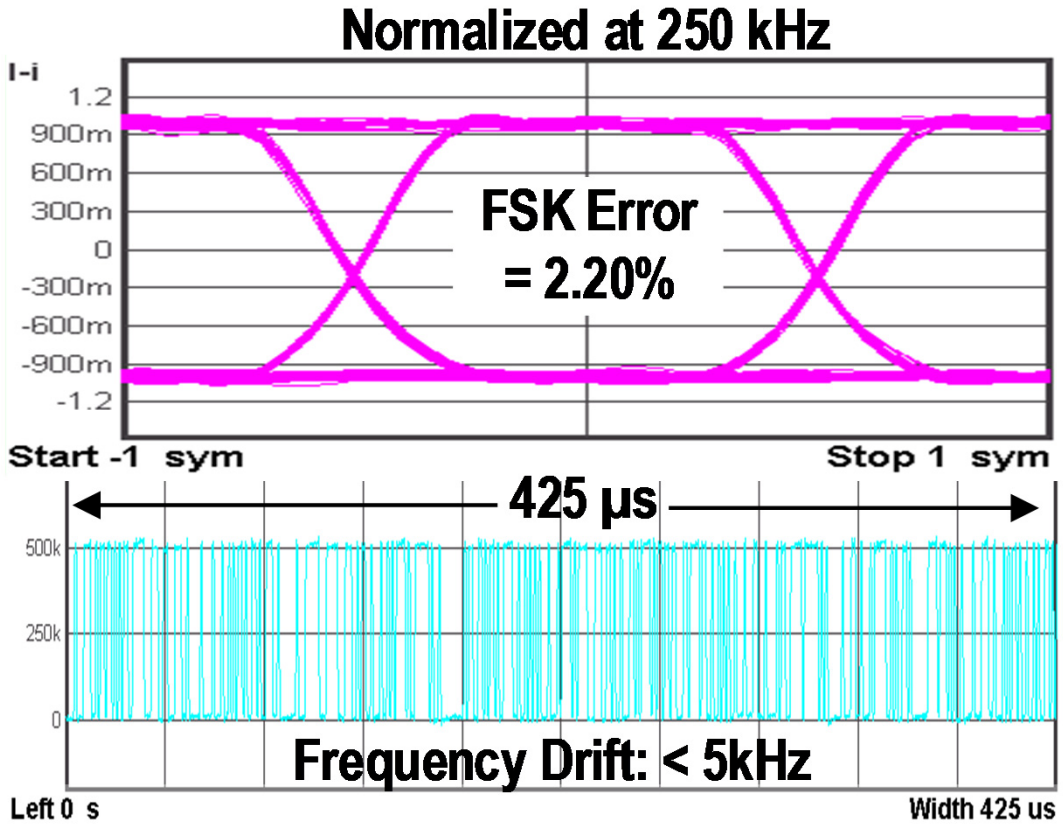




- P_{out}= 0dBm, η_{PA}= 30%, η_{PA+VCO}= 25% @ $V_{DD,EH}$= 0.2V
- HD_2=−49.6dBm, HD_3=−47.4dBm @ P_{out}= 0dBm, $V_{DD,EH}$= 0.2V

Transmitter Performance (Open-loop modulation)



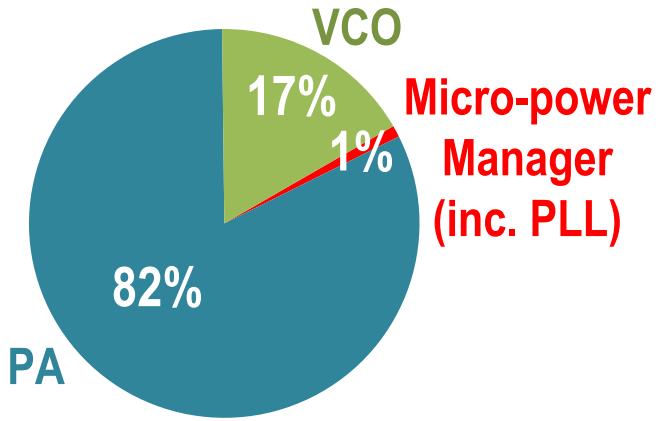


- FSK error = 2.20%
- Frequency drift <5kHz (within 425µs BLE packet)

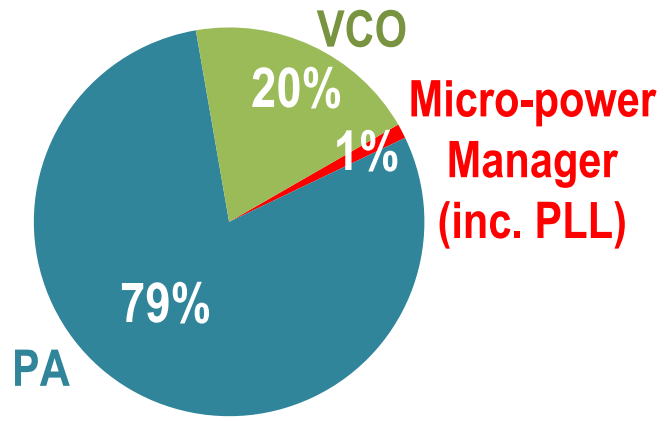
Active and Sleep Power Against $V_{DD,EH}$

Active Power

3.97mW @ $V_{DD,EH}$=0.2V

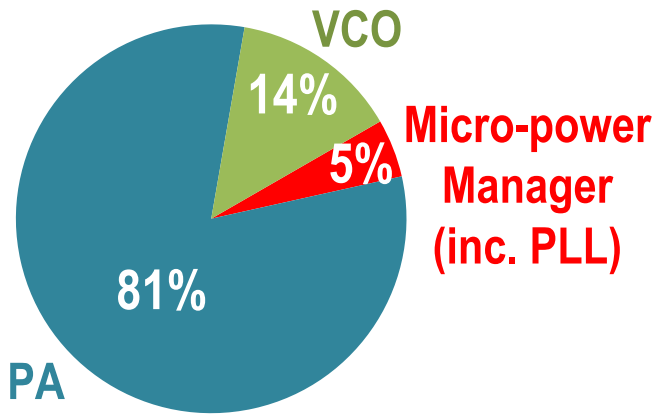


9.9mW @ $V_{DD,EH}$=0.3V

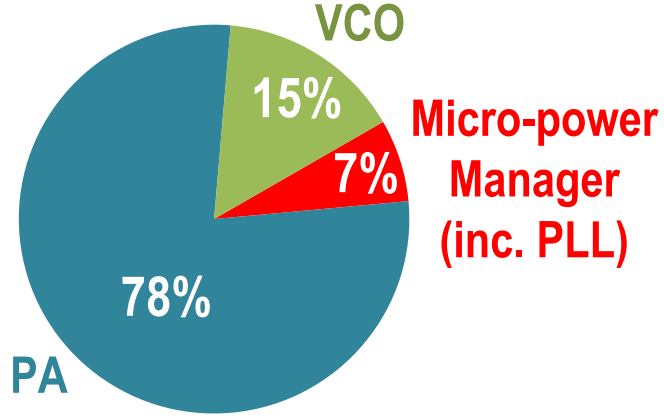


Sleep Power

5.17nW @ $V_{DD,EH}$=0.2V



45nW @ $V_{DD,EH}$=0.3V



Comparison with State-of-the-Art

Parameters	**This Work**	JSSC'16	JSSC'17	ISSCC'15
Key Techniques	**µPM + ULV VCO & PA + Type-I Analog PLL**	Dual-V_{DD} + Class-E/F_2 PA + LC-DCO + ADPLL	Dual-V_{DD} + Function-Reuse DCO-PA + ADPLL	Class-D PA + LC-DCO + ADPLL
CMOS Technology	**28 nm**	28 nm	65 nm	40 nm
Active Area (mm^2)	**0.53 ***	0.65	0.39	0.6
O/P Matching Network	**Fully On-Chip**	Fully On-Chip	Partially On-Chip	Partially On-Chip
HD_2/HD_3 @ P_{out} (dBm)	**−49.6 / −47.4 @ 0 dBm**	−50 / −47 @ 0 dBm	−43.2 / −47.6 @ 0 dBm	−49 / −53 @ −2 dBm
Modulation Error	**2.2% (GFSK)**	2.7% (GFSK)	2.29% (HS-OQPSK)	4.8% (GFSK)
Supply Voltage (V)	**0.2**	0.5 (DCO) / 1 (ADPLL & PA)	0.4 (DCO-PA) / 0.7 (ADPLL)	1
TX Power Consump. (mW) @ P_{out}	**4 @ 0 dBm ***	3.6 @ 0 dBm	4.4 @ 0 dBm	3.45 @ −2 dBm
TX Power Efficiency (%) @ P_{out}	**25 @ 0 dBm ***	28 @ 0 dBm	22.6 @ 0 dBm	18.3 @ −2 dBm
Sleep Power (nW)	**5.2**	N/A	N/A	N/A
VCO PN @ 1MHz offset (dBc/Hz)	**−119**	−116 to −117	−116	−110
VCO FoM @ 1MHz offset (dB)	**188.4**	188 to 189	N/A	183
PLL Power Efficiency (mW/GHz)	**0.29**	0.57	N/A	0.39
PLL FoM #(dB) normalized @ 1MHz f_{ref}	**−227.2**	−231.6	N/A	−220.9
PLL Largest Spurs (dBc)	**−47**	−60	−42	−38

* Included a fully-integrated µPM. [5-7] have not included the loss, power and area of the power-management units.

$$\#\,\text{PLL FoM} = 10\log\left[\left(\frac{\sigma_{\text{rms}}}{1\ \text{sec}}\right)^2 \cdot \frac{\text{Power}}{1\ \text{mW}} \cdot \frac{f_{\text{REF}}}{1\ \text{MHz}}\right]$$

Conclusions

- A BLE TX fully-integrated a micropower manager to enable ULV operation down to **0.2V** in 28nm CMOS

  - **ULV gate-to-source feedback VCO →**

    670µW @ $V_{DD,EH}$ = 0.2V and −127.7dBc/Hz PN @ 2.5MHz offset

  - **ULV class-E/F_2 PA with embedded 3rd-harmonic notching →**

    −47.4dBm HD_3 with no extra area

  - **ULV Type-I PLL with a 5% duty-cycled clock for MSSF →**

    14dB lower REF spurs with negligible extra power

Acknowledgments

- Multi-Year Research Grant of University of Macau

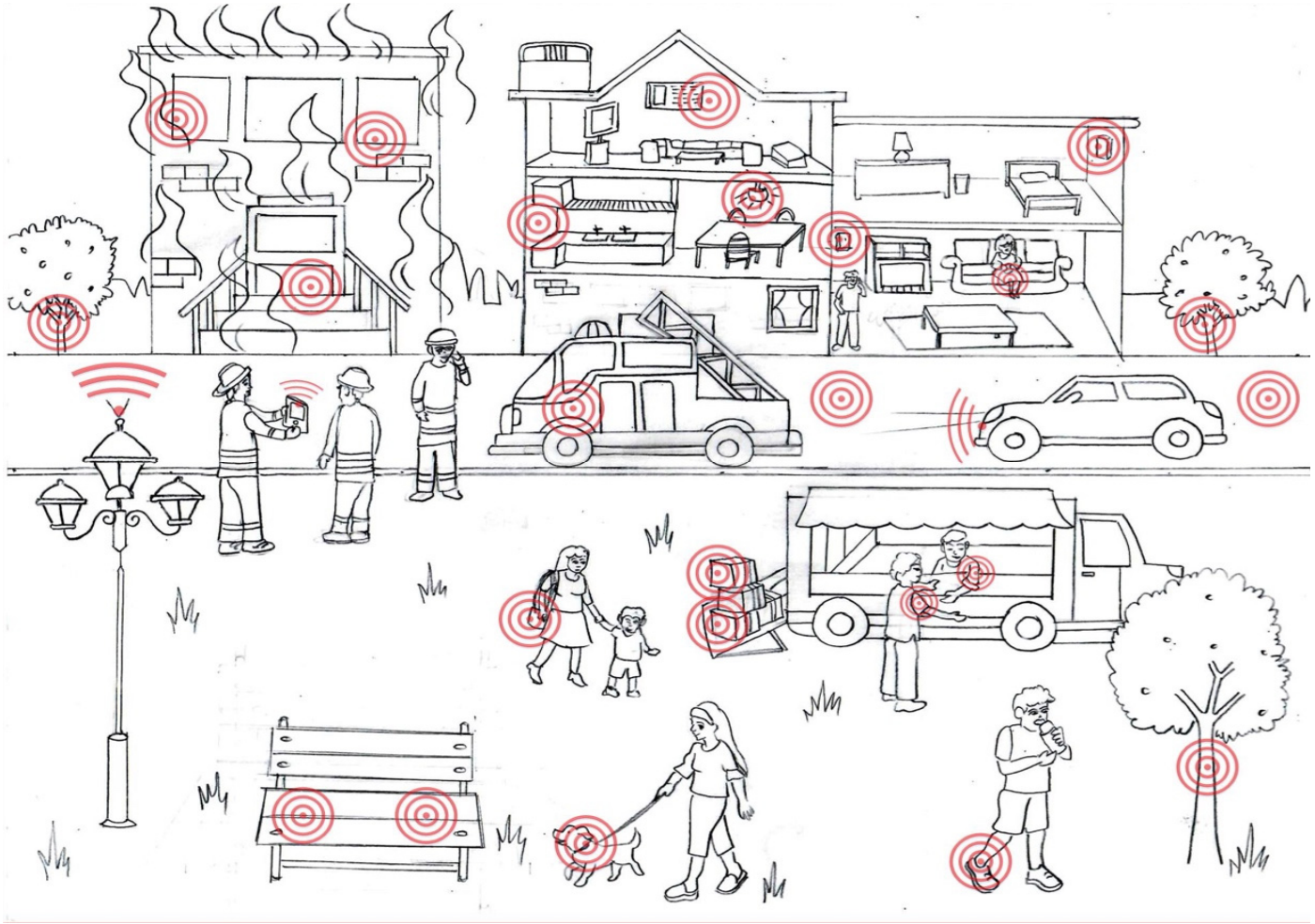
- Macao Science and Technology Development Fund (FDCT)

A -76dBm 7.4nW Wakeup Radio with Automatic Offset Compensation

Jesse Moody, Pouyan Bassirian, Abhishek Roy, Ningxi Liu, Stephen Pancrazio, N. Scott Barker, Benton H. Calhoun, Steven M. Bowers

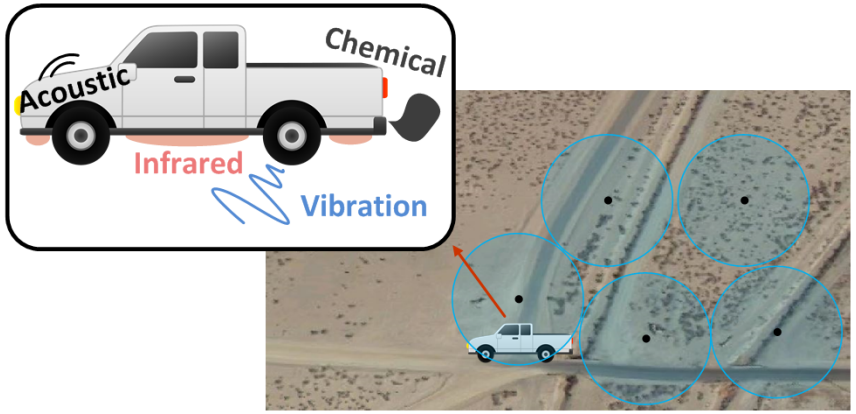
University of Virginia

Applications enabled by smart sensor nodes



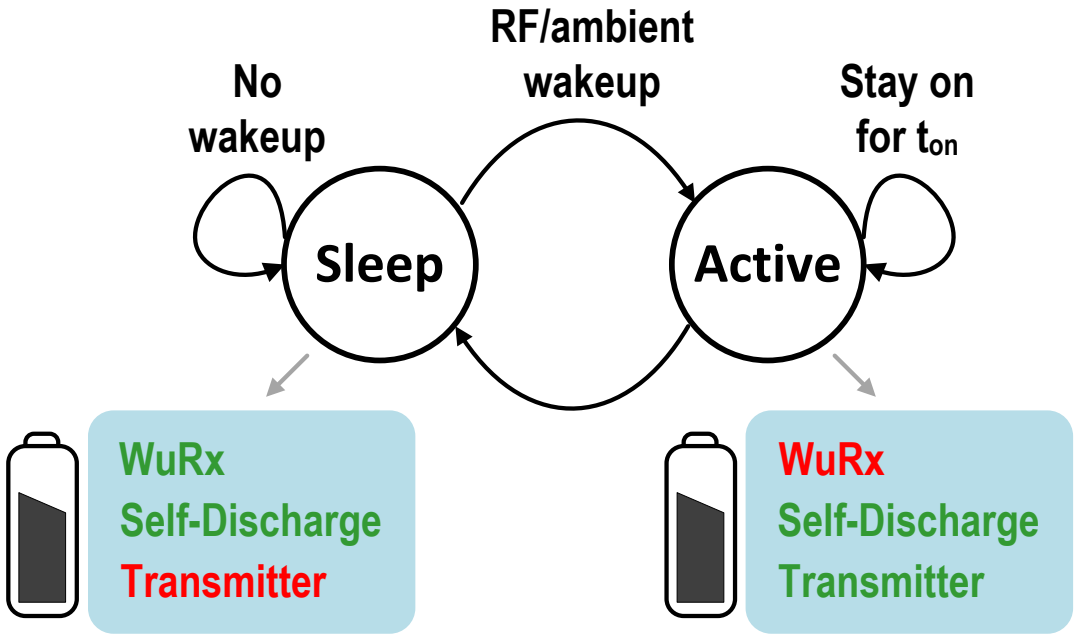
Smart Cities

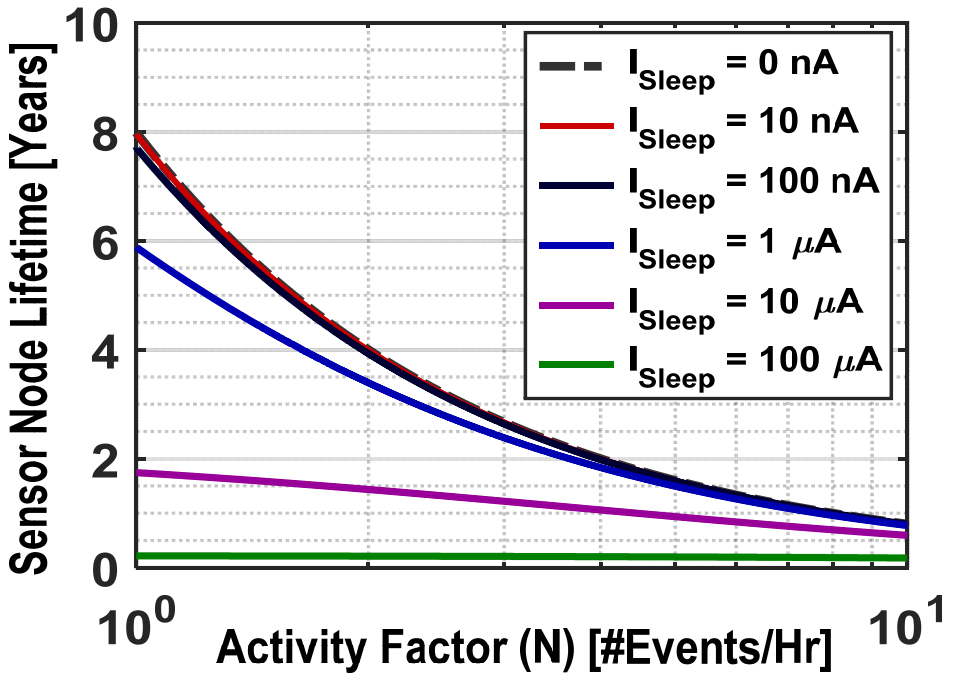
Agriculture Monitoring



Unattended ground sensors

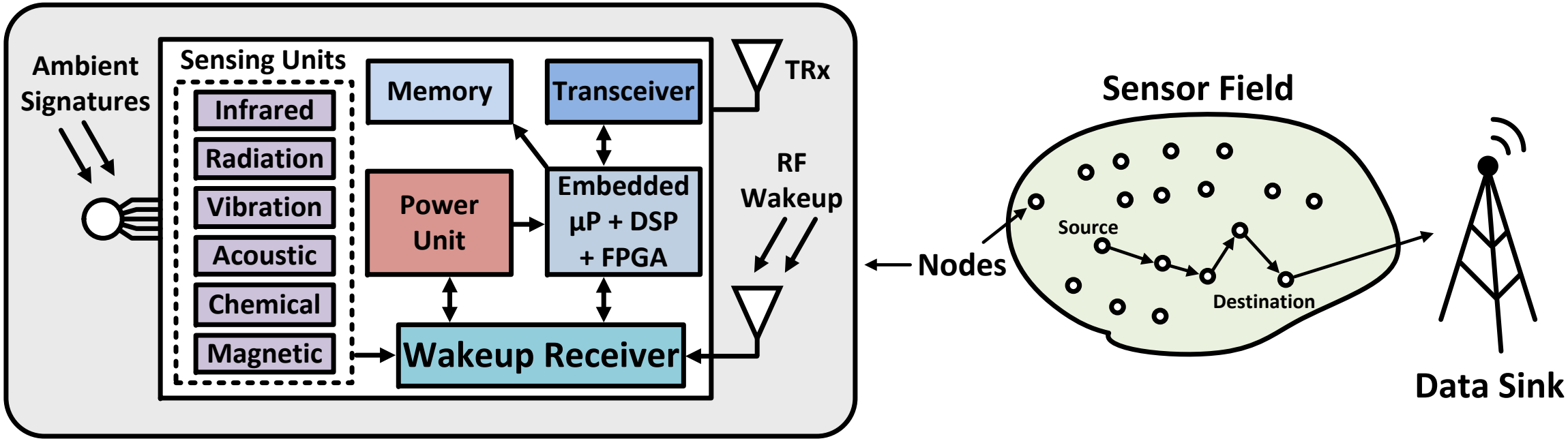
Smart sensor node lifetime





- When considering a sensor node utilizing ~10mW on power life time can be extended by years utilizing nanowatt level WuRx's

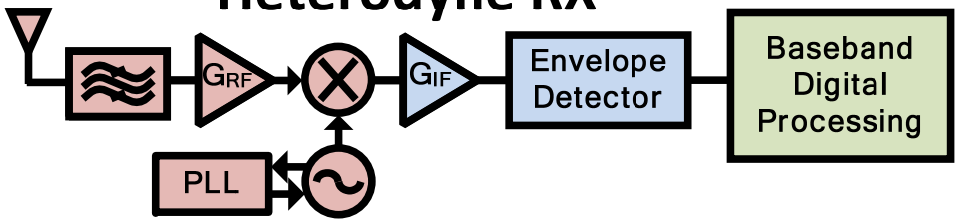
Event-driven smart sensor nodes



- Ubiquitous, persistent real time environmental monitoring
- Operation over extreme time scales and environmental conditions

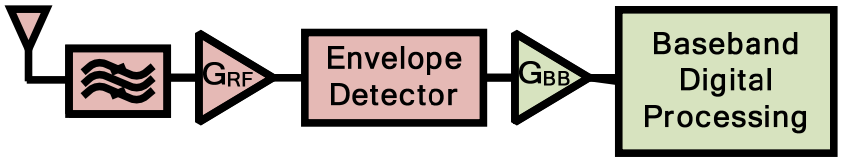
WuRx front-end architectures

Heterodyne RX



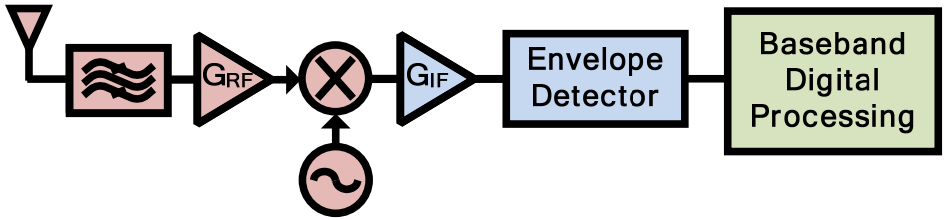
- Traditional radio reciever architecture
- Highest sensitivity
- Highest power

Tuned Front End RX



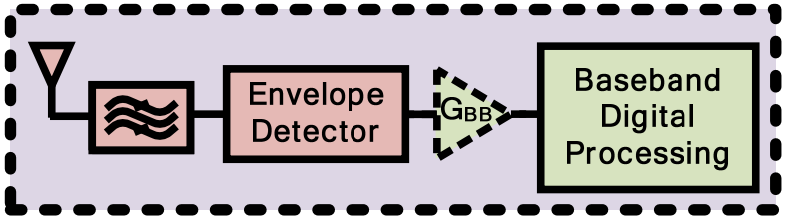
- Input LNA for increased sensitivity
- High sensitivity
- RF LNA required

"Uncertain IF" RX



- Unlocked oscillator into wideband IF
- High sensitivity
- RF Oscillator required, IF gain stages required

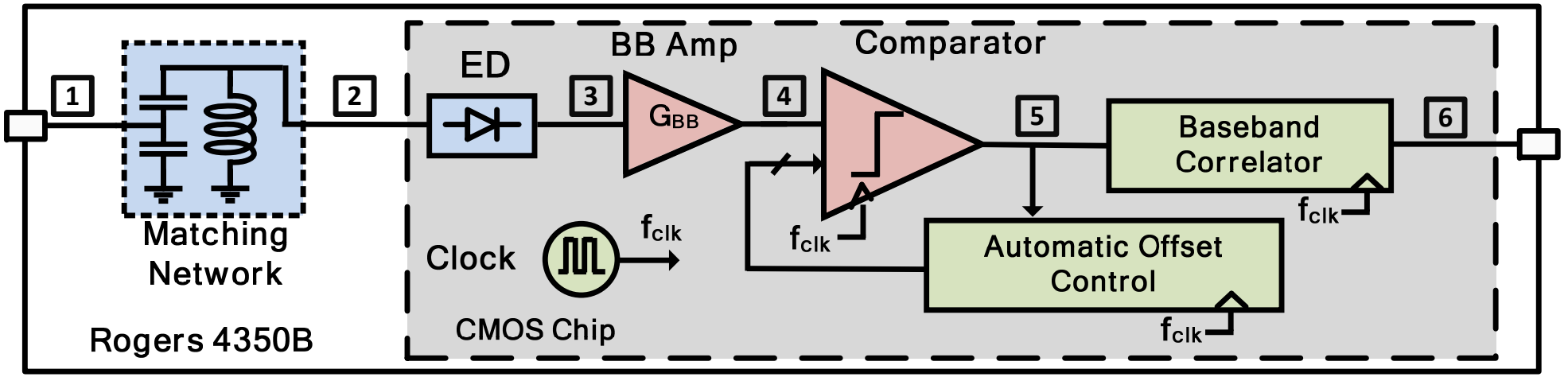
Detector First RX

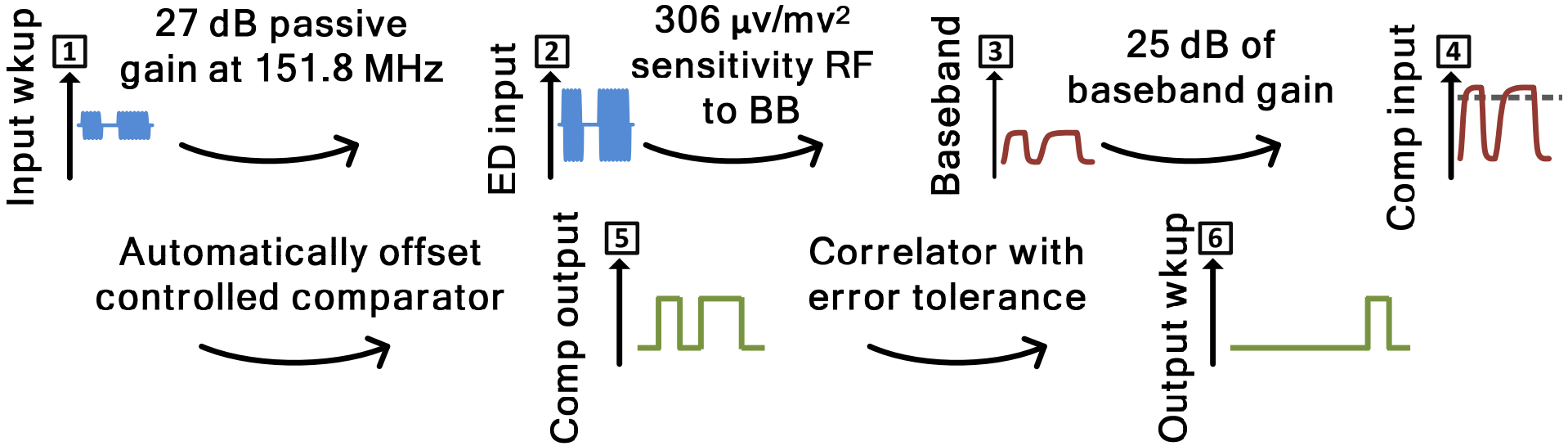


- Lowest DC Power consumption
- Moderate sensitivity
- No gain required at RF frequencies

System Architecture

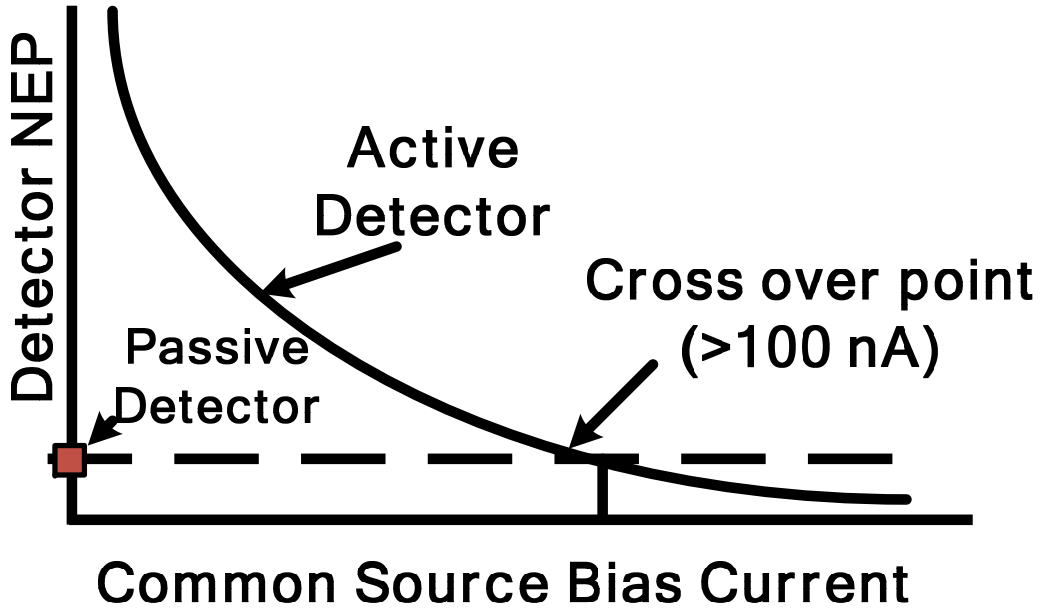
This work: Detector First RX



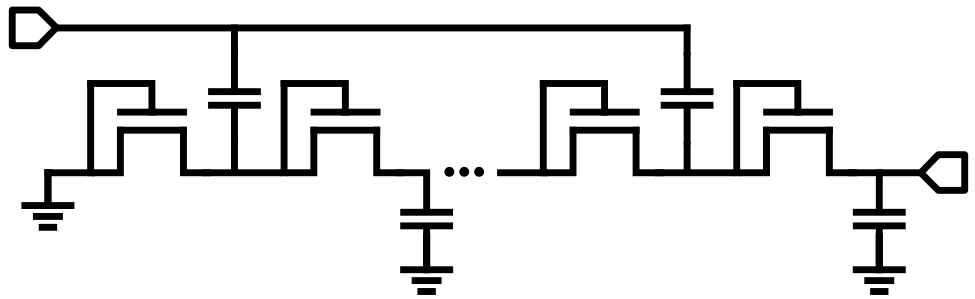


Envelope Detector comparison

- Optimal RX sensitivity requires:
  1. High OCVS (V_{DC}/P_{RF})
  2. Low output noise levels
  3. Low bandwidth reception



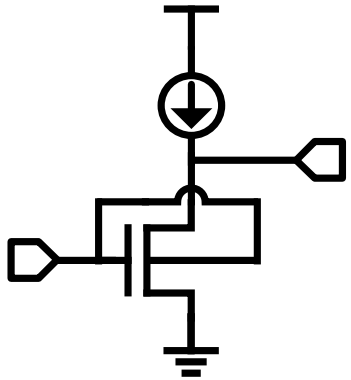
Dickson Passive Detector



- High Voltage Sensitivity
- Zero Power
- High output impedance
- Zi vs. Conversion Gain

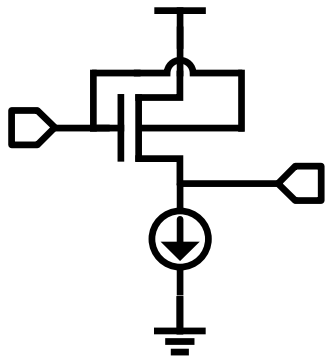
Optimal for P_{DC} <100nW

Common Source Active Detector



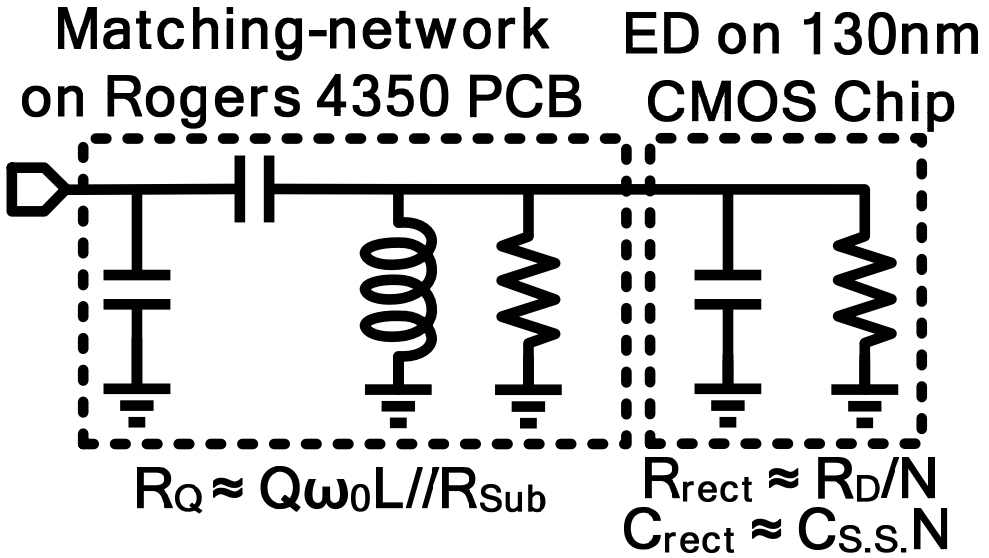
- Medium Voltage Sensitivity
- Zi vs. Flicker Noise
- High Power

Common Drain Active Detector



- Low Voltage Sensitivity
- Zi vs. Flicker Noise
- High Power

Matching-network ED codesign



$$SNR_{Out} = \frac{N\mu_D P_{in} R_D R_p}{(R_D + NR_p)\sqrt{4kTNR_D B}}$$

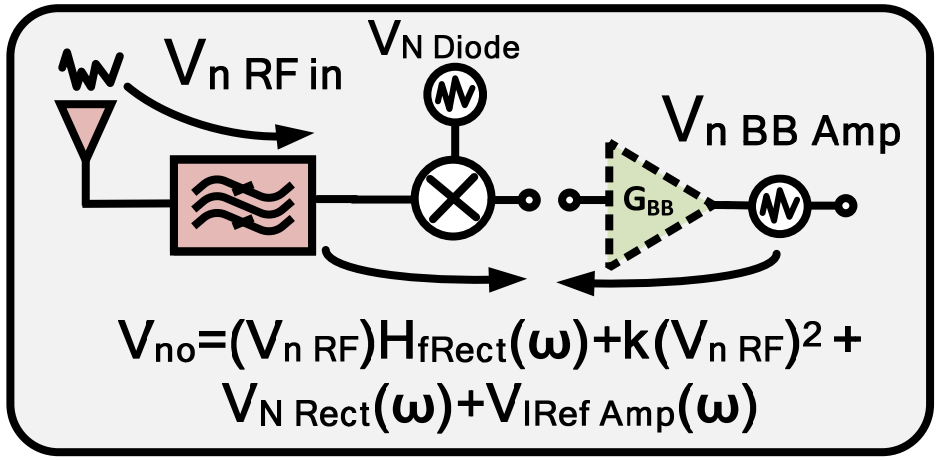
$$SNR_{Opt} \propto k\sqrt{R_p} \qquad N_{opt} = \frac{R_D}{R_p}$$

- For optimal output SNR:
  - $R_{Rect} \approx R_Q$
  - Two independent design variables available
    - R_D ~ DC channel impedance of diode
    - N ~ Number of diodes
- Output SNR is a monotonically increasing function of R_Q
  - Increase Q factor
  - Decrease capacitance

Baseband/Dickson envelope detector codesign

- In order to overcome input referred baseband noise:
  - $V_{nDet} > V_{NAmp}$
- For detector output impedance we find that:
  - $R_{ORect} \approx NR_D$
  - Or that: $R_{ORect} \approx N^2 R_Q$
  - Where R_Q is the shunt resistance of RF resonator

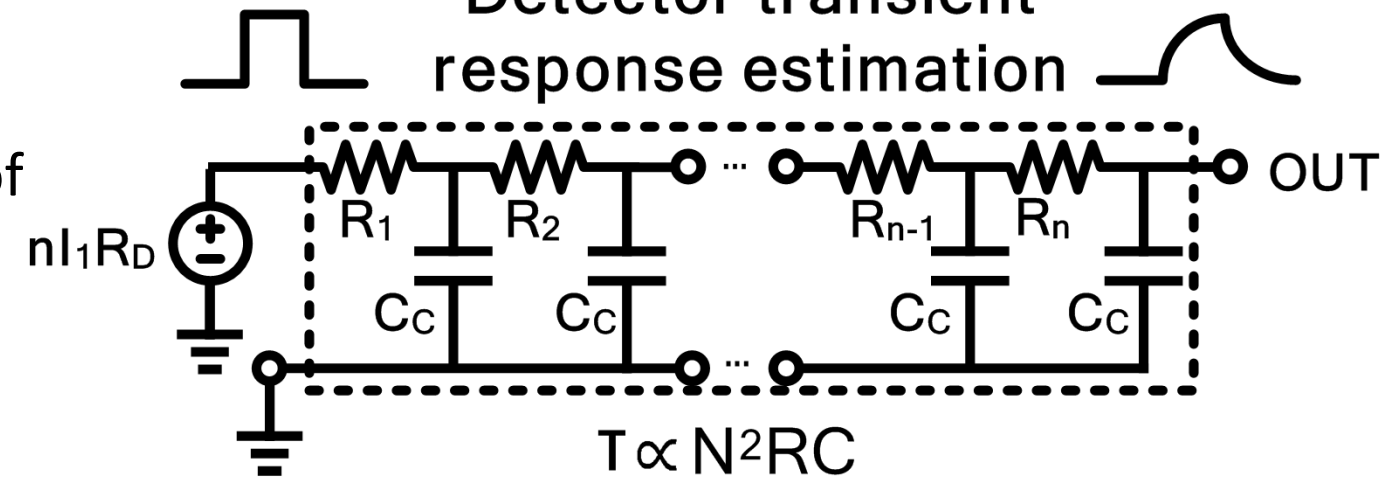
Front end noise sources



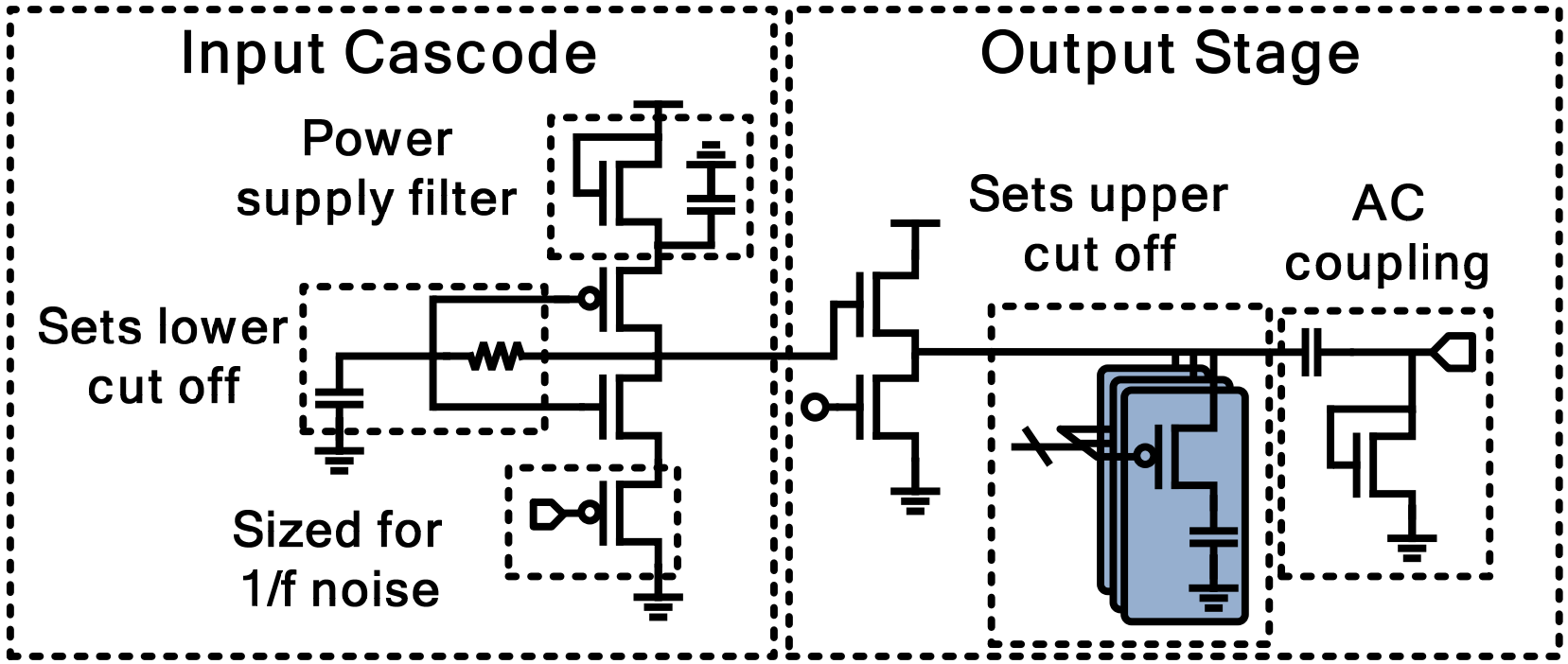
$$V_{nDET} \propto \sqrt{NR_D}$$

$$V_{nAmp} \propto \sqrt{1/I_D}$$

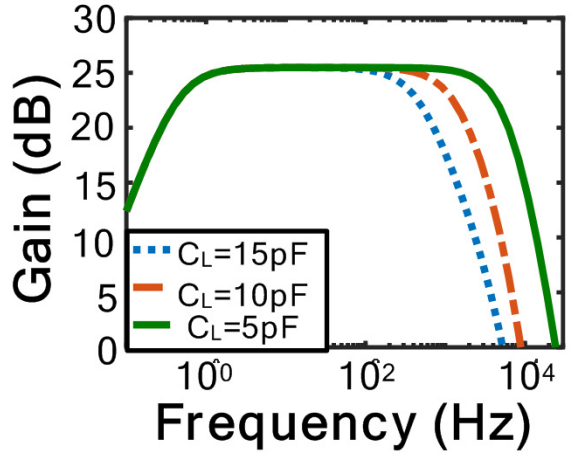
Detector transient response estimation



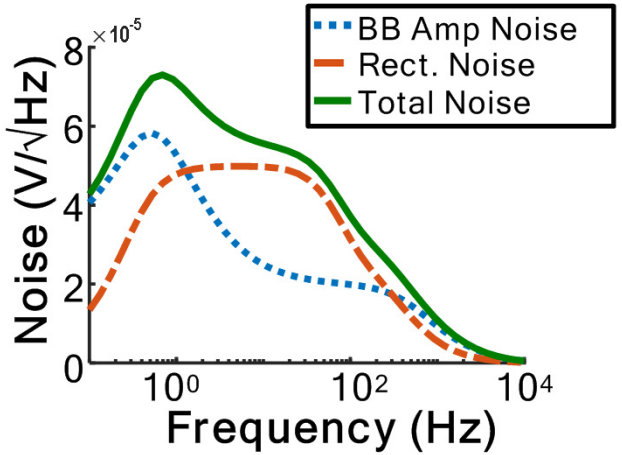
Baseband Amplifier Design



Simulated Baseband Amplifier Gain

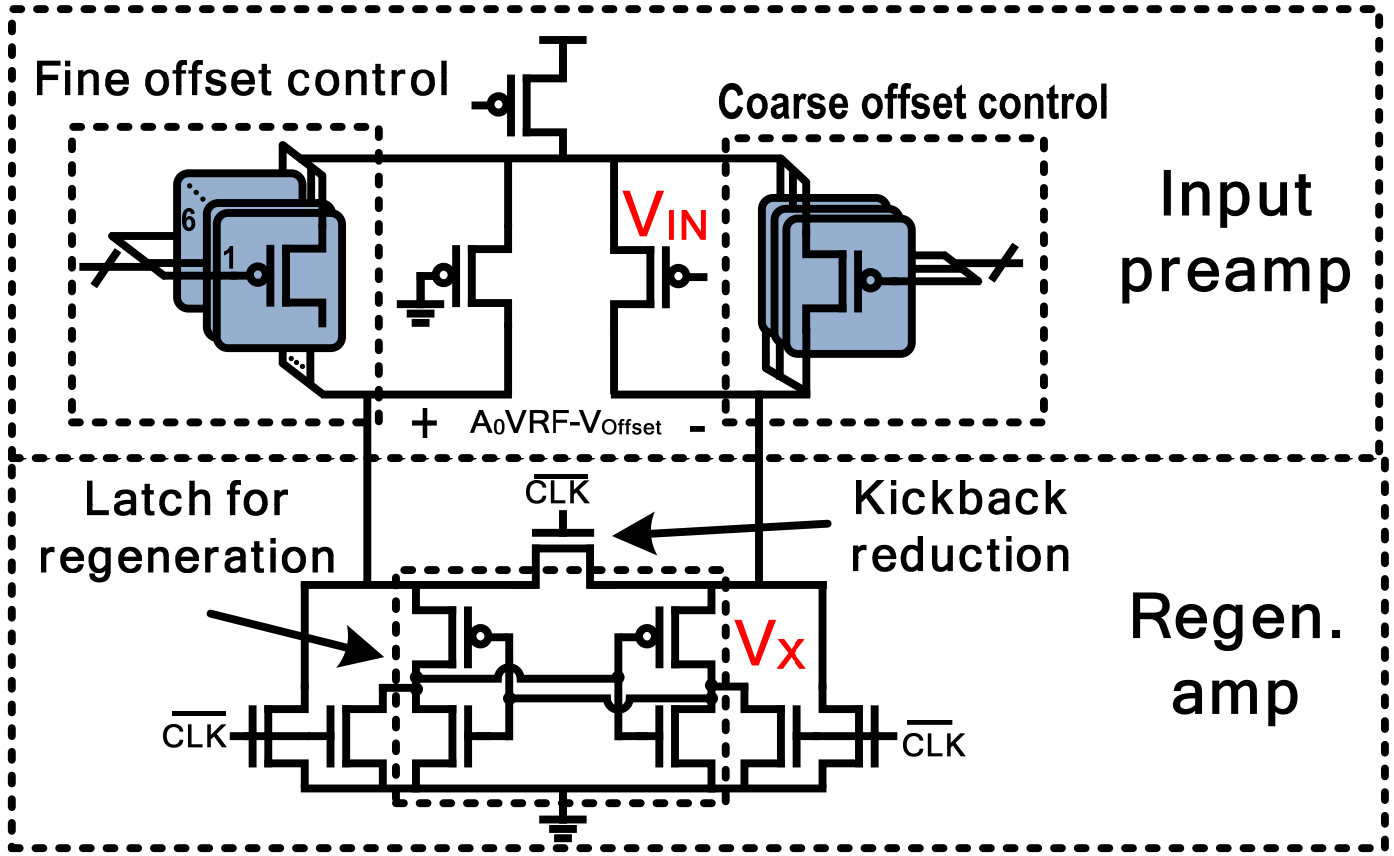


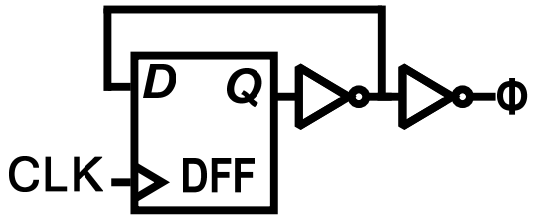
Simulated Noise Contributions Referred to Comparator Input

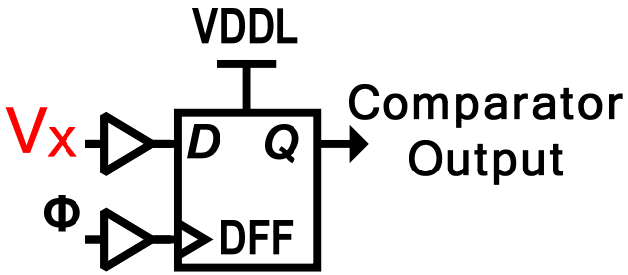


- Introduction of low frequency transmission zero rejects interferers
- DC power level set by output noise of rectifier

Comparator design



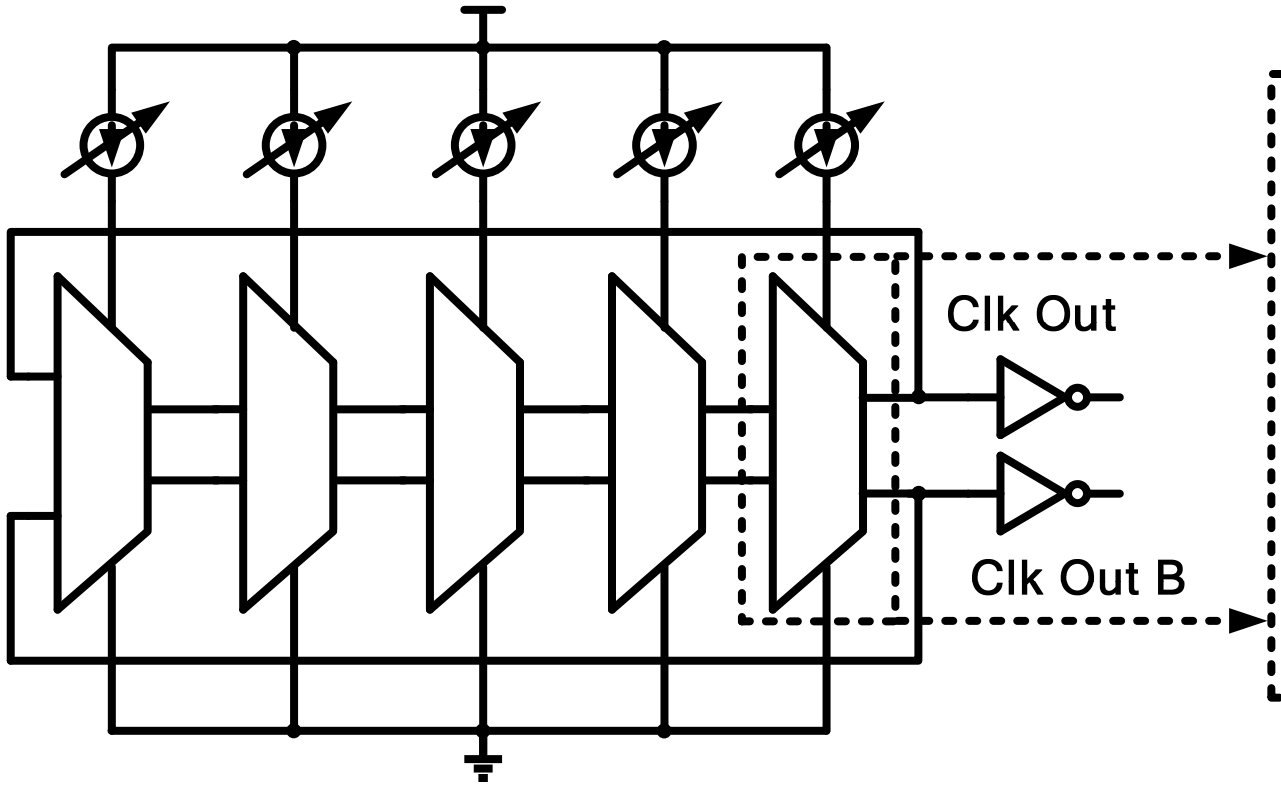




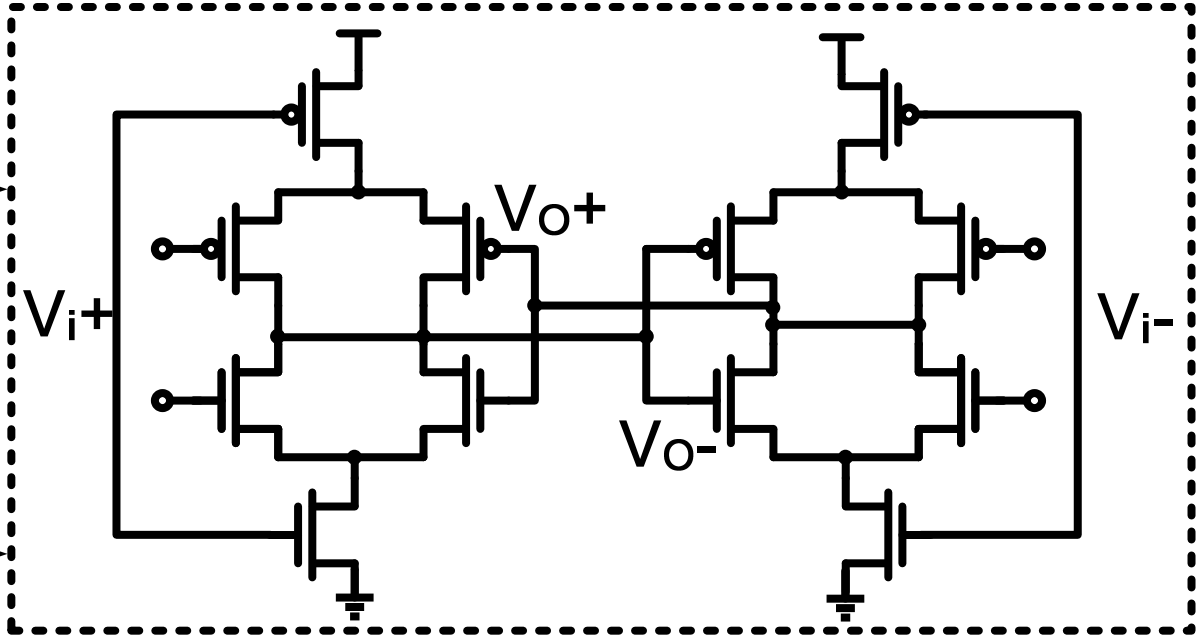
- Current reused between latching stage and preamplifier
- 9 bits of offset control allowing for ultra wide trip voltage range

Clock source

5 Stage current starved ring oscillator



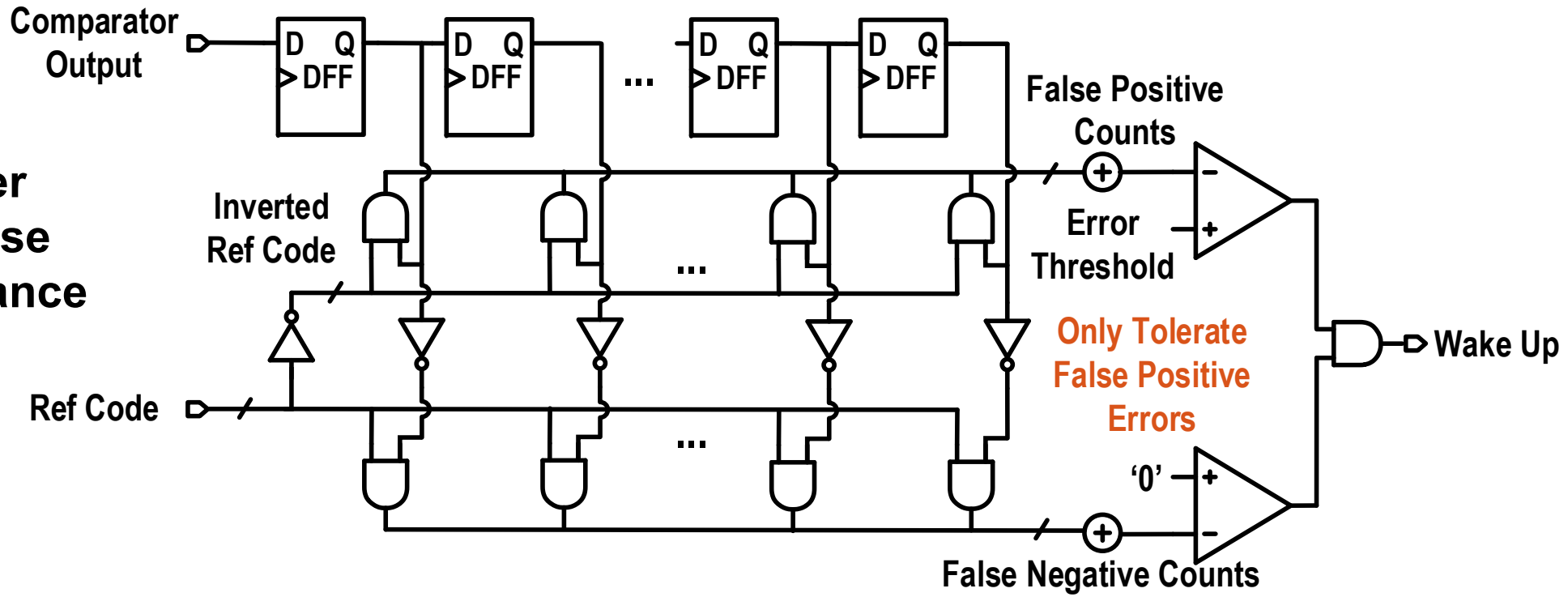
Unit gain unit cell



- External bias sets device bias and operation frequency
- Operates from 50 Hz to 10 kHz

Digital backend

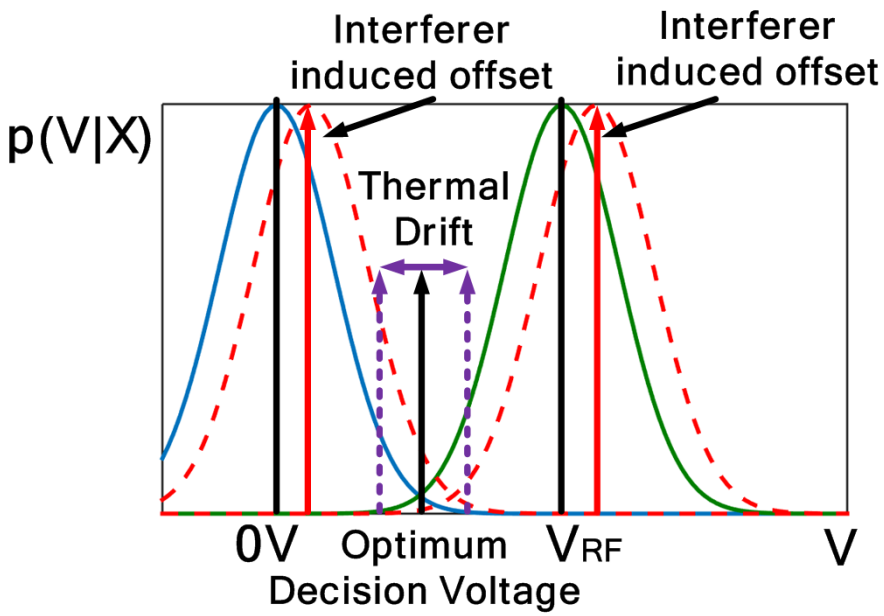
8-bit Shift Register Correlator with False Positive Error Tolerance

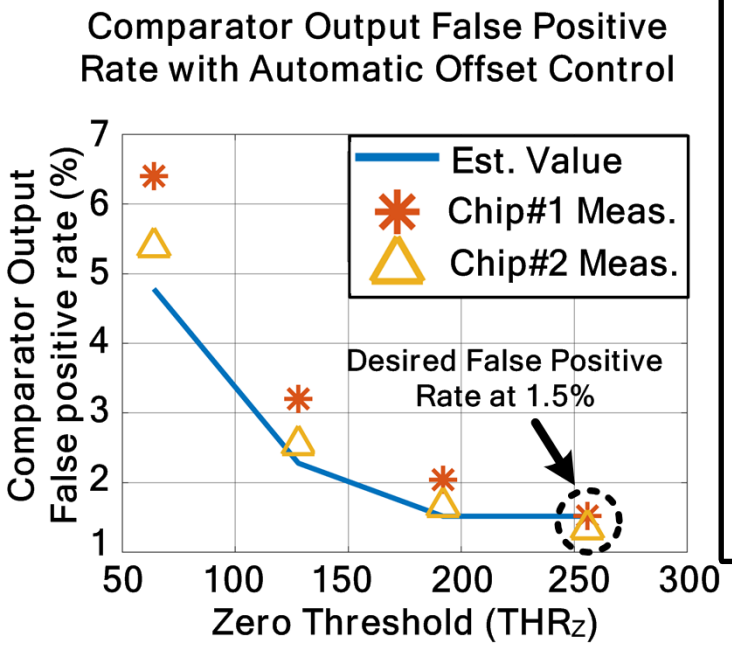


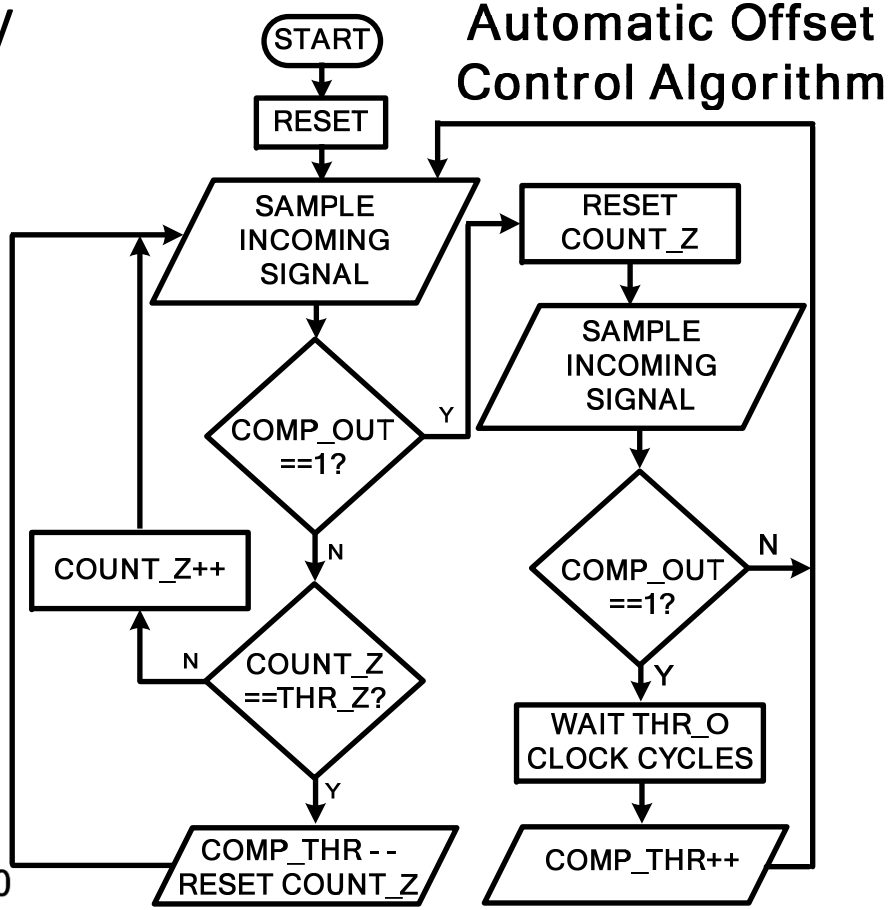
- Asymmetric error tolerance increases robustness without degrading false alarm rate
- <1 nW DC power consumption

Automatic offset control algorithm

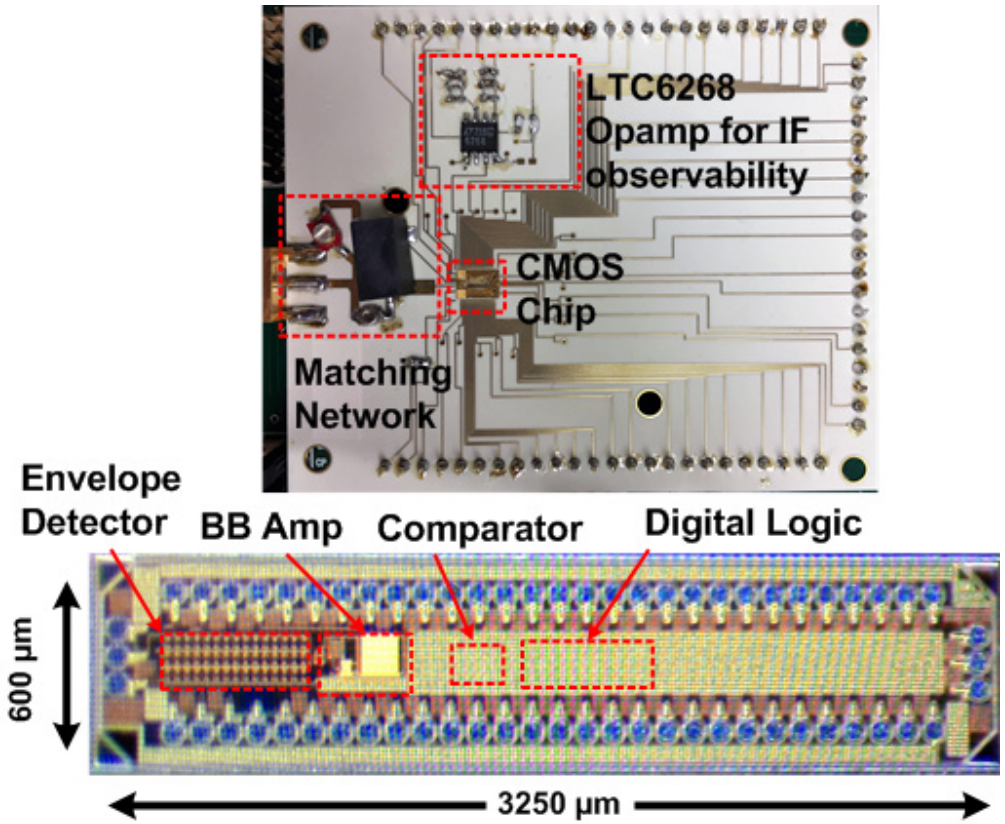
- Rejects fluctuations due to PVT variation dynamically
- No input RF signal required for calibration

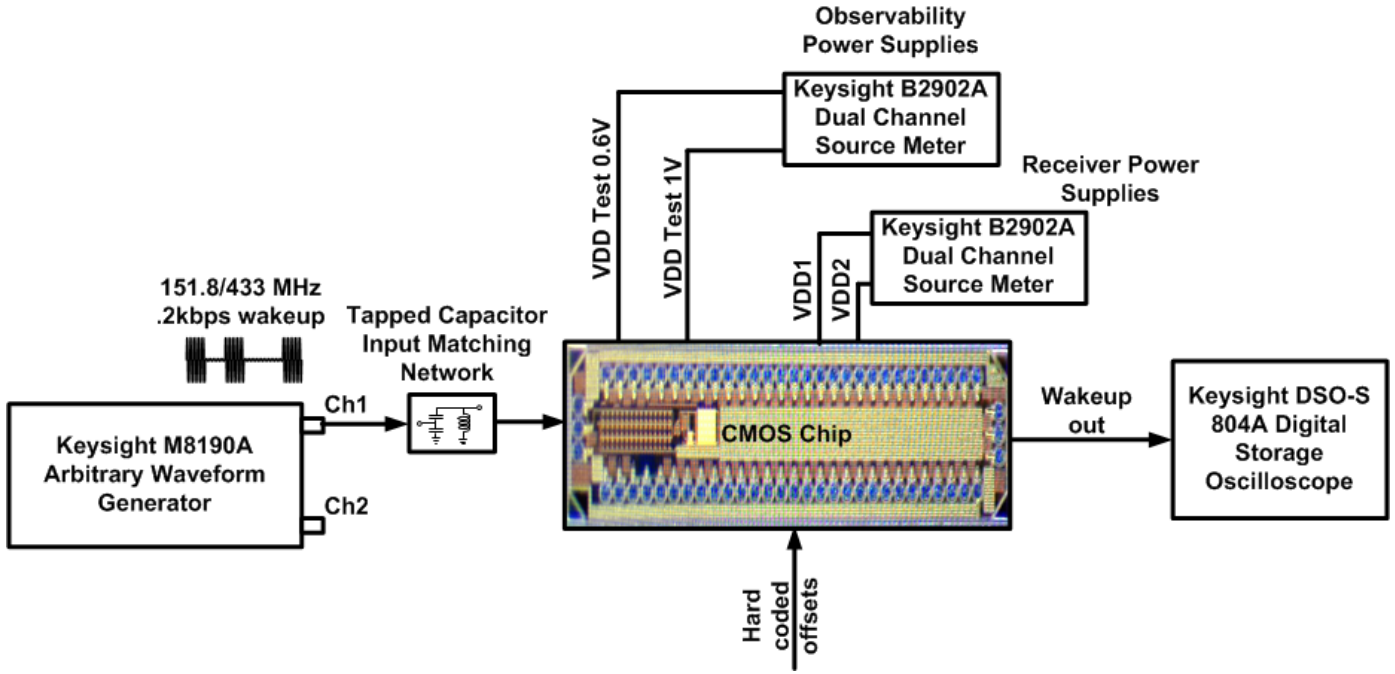






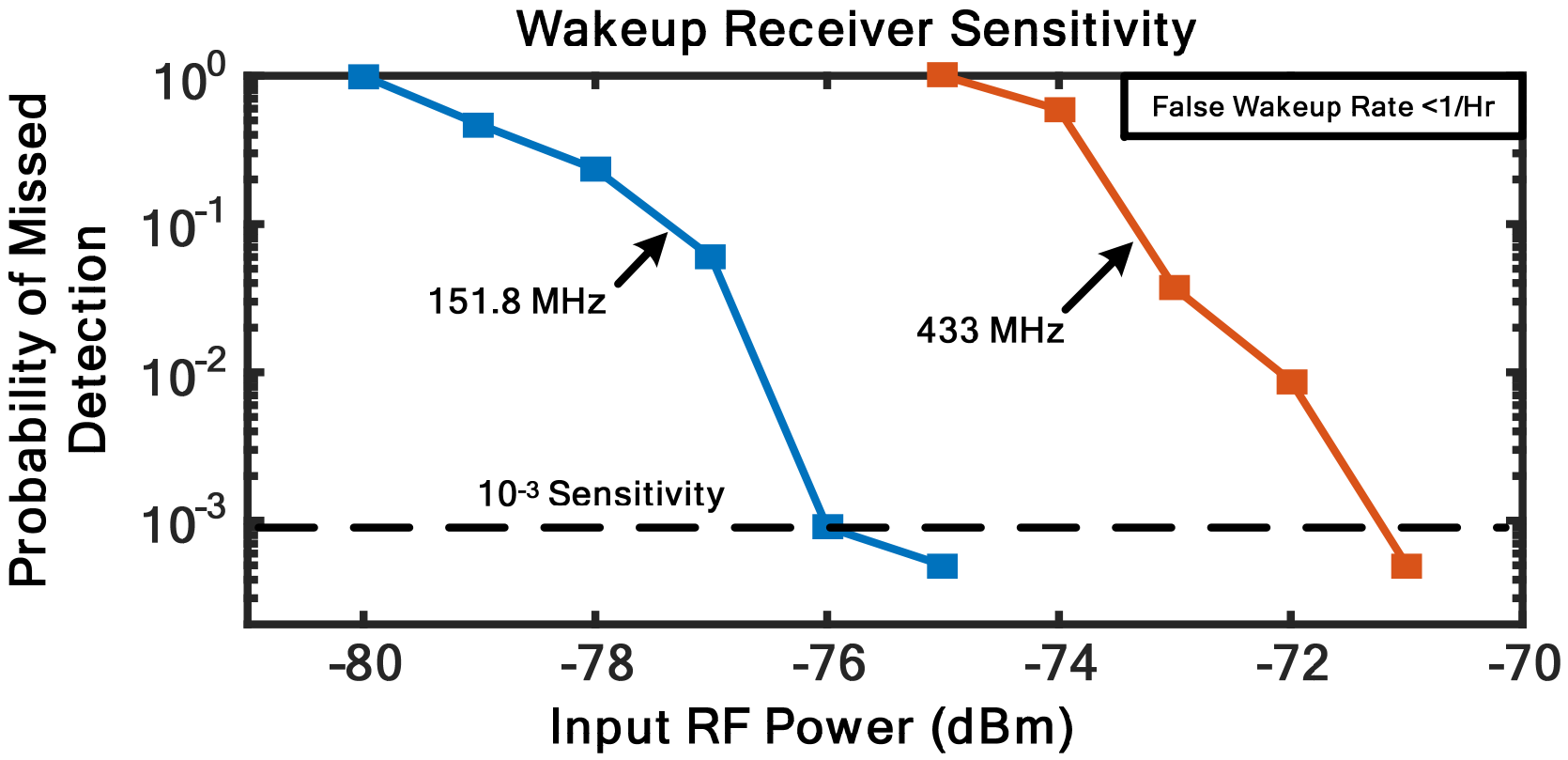
Measurement setup for power and sensitivity

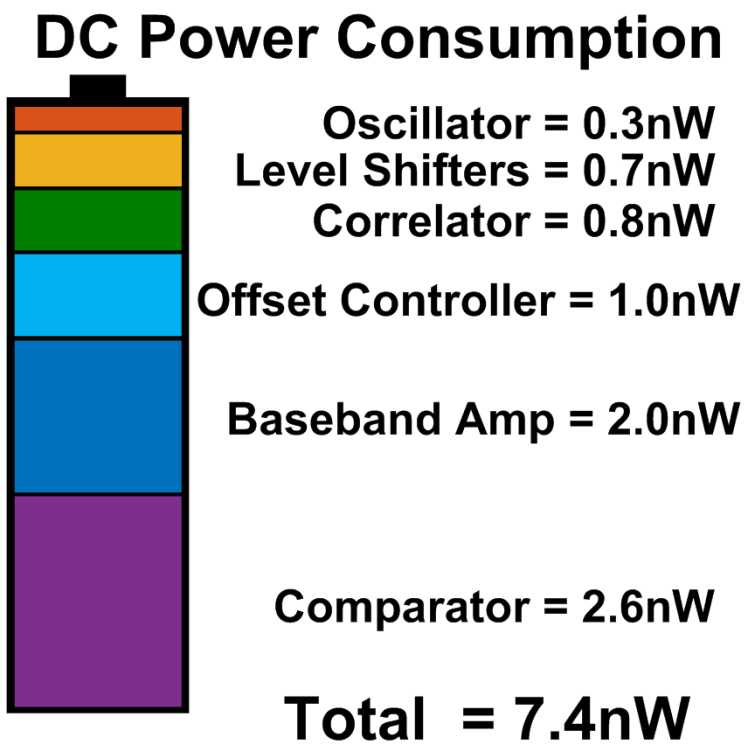




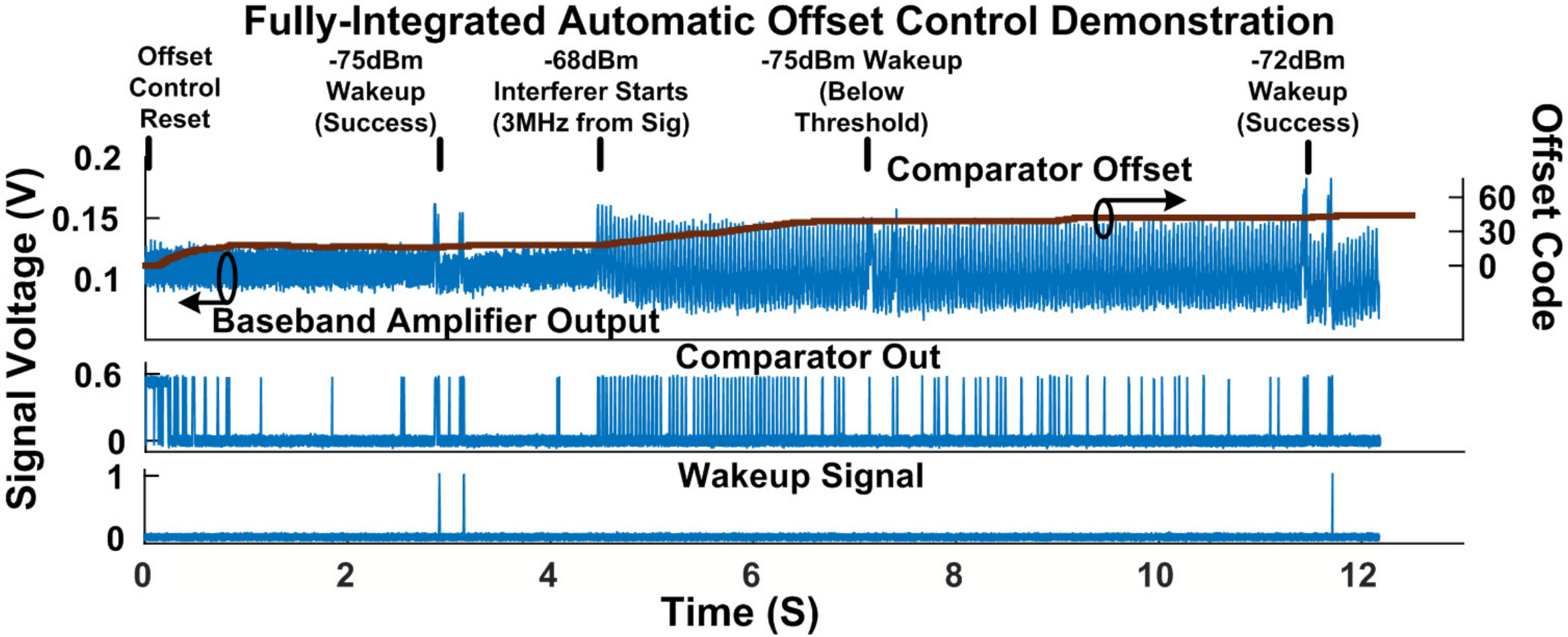
- Chip fabricated in 130nm RF CMOS process

Sensitivity measurement results





Automatic offset compensation and interferer rejection measurement results



Comparison to the state of the art

	This Work		Jiang ISSCC'17 [1]	Roberts ISSCC'16 [2]	Sadagopan RFIC'17 [3]	Salazar ISSCC'15	Abe VLSI'14	Pletcher ISSCC'08
Technology	130 nm		180 nm	65 nm	65 nm	65 nm	65 nm	90 nm
Carrier Frequency	151.8MHz	433MHz	113.5MHz	2.4GHz	2.4GHz	2.4GHz	925.4MHz	2 GHz
Power Consumption	7.4 nw	7.4 nw	4.5 nW	236 nW	365 nW	99 µW	45.5 µW	52 µW
Data Rate	200 bps	200 bps	300 bps	8.192 kbps	2.5 kbps	10 kbps	50 kbps	100 kbps
Dissipated Energy per bit	37 pJ	37 pJ	15 pJ	28.8 pJ	146 pJ	9900 pJ	910 pJ	520 pJ
Non-constant Envelope Interferer Rejection	Integrated Auto Offset Control Loop		N/A	N/A	N/A	N/A	2-Step Wakeup	N/A
Out-of-band Interferer Rejection Method	High-Q FE Transofrmer		High-Q FE Transformer	Matching Network	High-Q FE Co-Design	N-path filter	2-Step Wakeup	MEMS Filter
Sensitivity	-76 dBm [1]	-71 dBm [1]	-69 dBm [1]	-56.5 dBm [2]	-61.5 dBm [2]	-97 dBm [2]	-87 dBm [2]	-72 dBm [2]
Sensitivity with CW interference	-76 dBm [3]	N/A	N/A	N/A	-58.5 dBm [4]	-94 dBm [5]	-84 dBm [6]	N/A
Die Area	1.95 mm^2		6 mm^2	2.25 mm^2 *	1.1 mm^2 *	0.0576 mm^2 *	1.27 mm^2 *	0.1 mm^2 *

[1] 10^{-3} Prob. of Missed Detection (PMD) [2] 10^{-3} Bit Error Rate (BER) [3] Carrier-to-interference ratio (CIR)= -30dB @ -3MHz offset, 10^{-3} PMD [4] CIR=-20dB @ -3MHz offset, 10^{-3} BER. [5] CIR=-31dB/-27dB @ +/-5MHz offset, 10^{-3} BER [6] CIR= -40dB@ -3 MHz offset, 1% packet error ratio (PER)

* Active area

Conclusions

- Demonstration of -76 dBm sensitivity with 7.4 nW DC power consumption
- Utilizing novel offset compensation algorithms calibration can occur without power hungry RF test circuit
  - Suppresses non-envelope interference
- Front end detector choice is a critical design parameter for development of ULP WuRx
  - Achieved 15.8mV/nW OCVS at 151.8MHz and 6.3mV/nW at 433MHz
  - Total analog DC power <5 nW.
  - > 30dB envelope interference rejection

Acknowledgements

- The authors would like to acknowledge the following people and groups for helpful technical discussions
  - Prof. Stephen Wilson of the University of Virginia
  - Members of the University of Virginia IECS and RLP-VLSI Groups

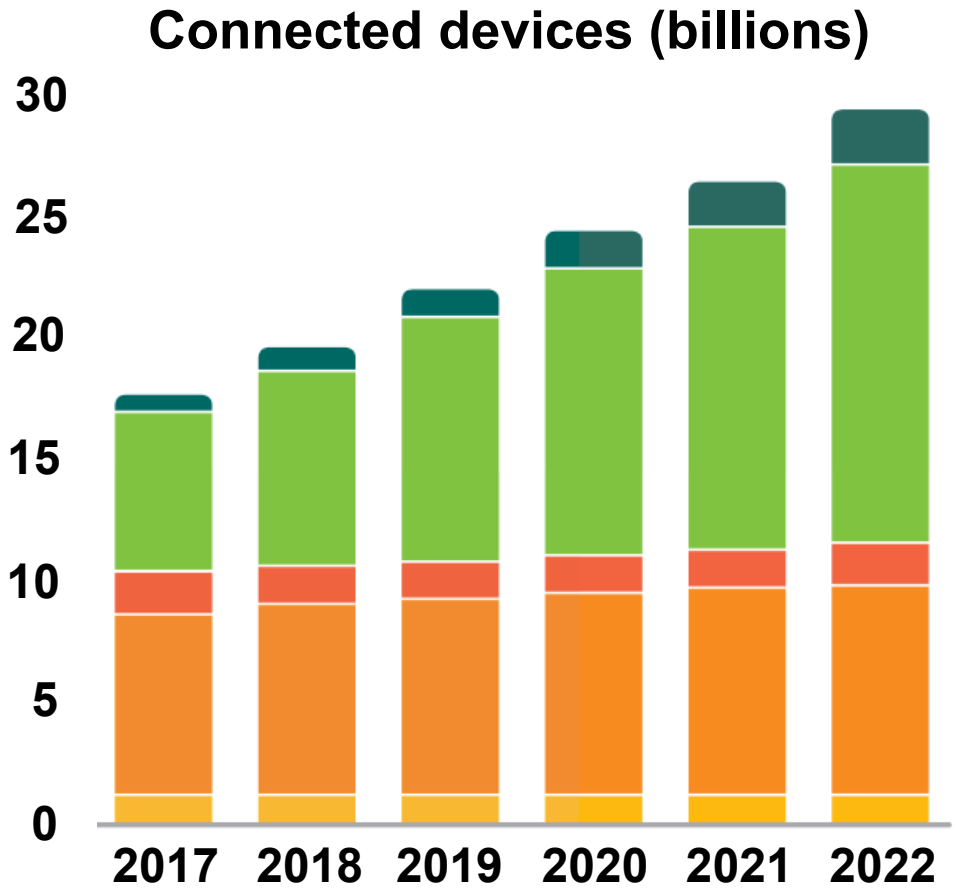
- We would also like to thank Troy Olsson and the DARPA NZERO program for support.

A 14.5mm^2 8nW -59.7dBm-Sensitivity Ultrasonic Wake-Up Receiver for Power-, Area-, and Interference-Constrained Applications

Angad Singh Rekhi and Amin Arbabian

Stanford University

An Increasingly Interconnected World



	2016	2022	CAGR
Wide-area IoT	0.4	2.1	30%
Short-range IoT	5.2	15.5	20%
PC/laptop/tablet	1.6	1.7	0%
Mobile phones	7.3	8.6	3%
Fixed phones	1.4	1.3	0%

5-year projection of global growth of wirelessly-connected devices
[Ericsson Mobility Report, 2017]

An Increasingly Interconnected World

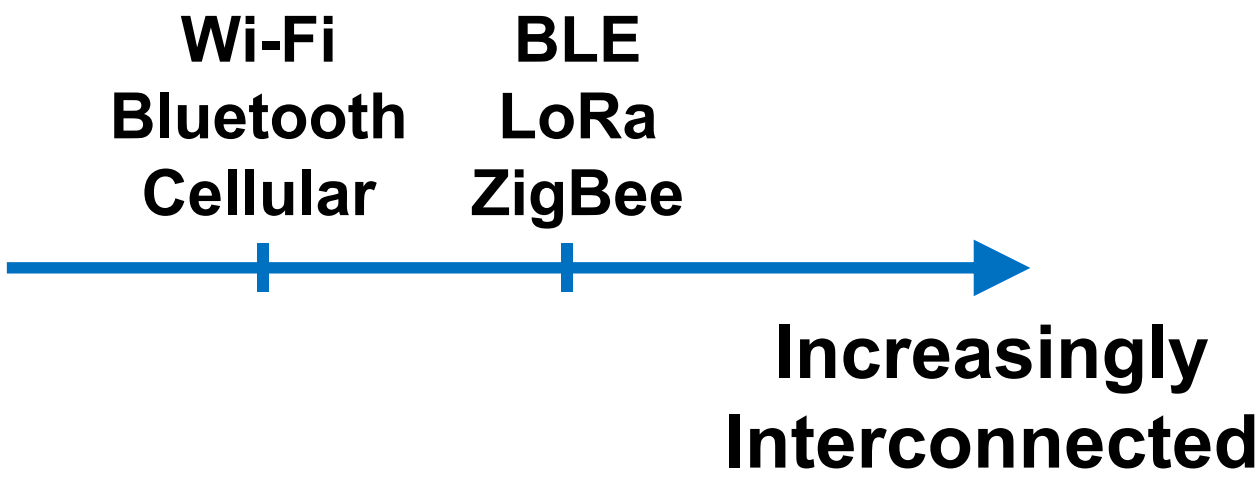
Tablets, phones, watches, home appliances, …

An Increasingly Interconnected World

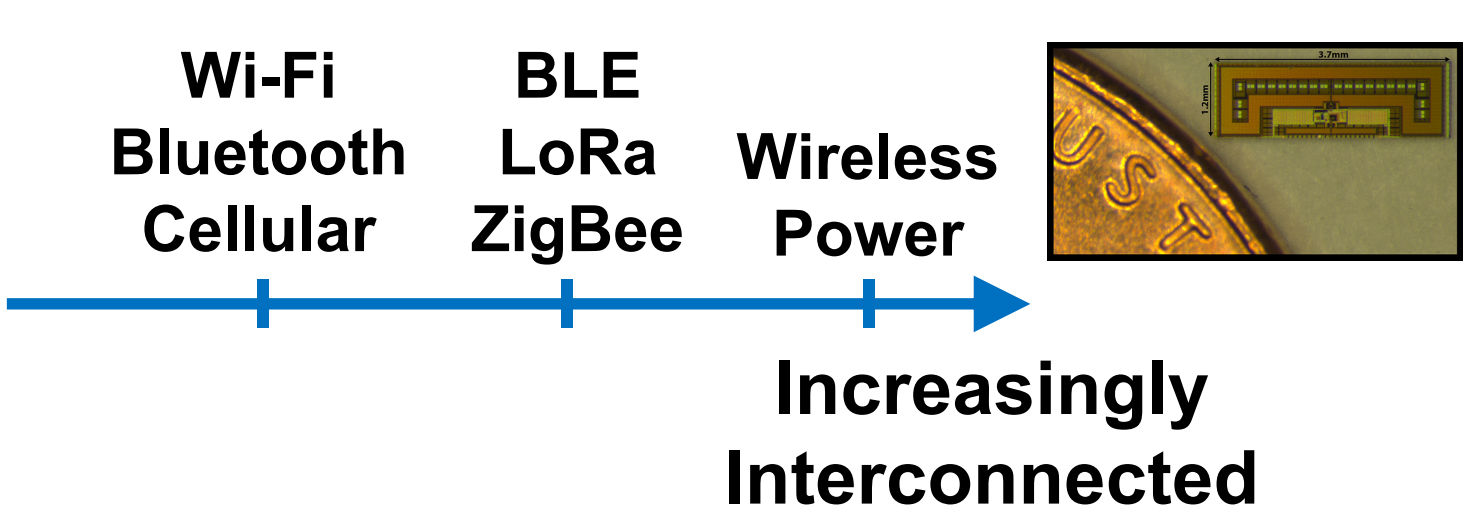
Tablets, phones, watches, home appliances, …

Connected, unobtrusive, ubiquitous networks of nodes

The Evolving Internet of Things

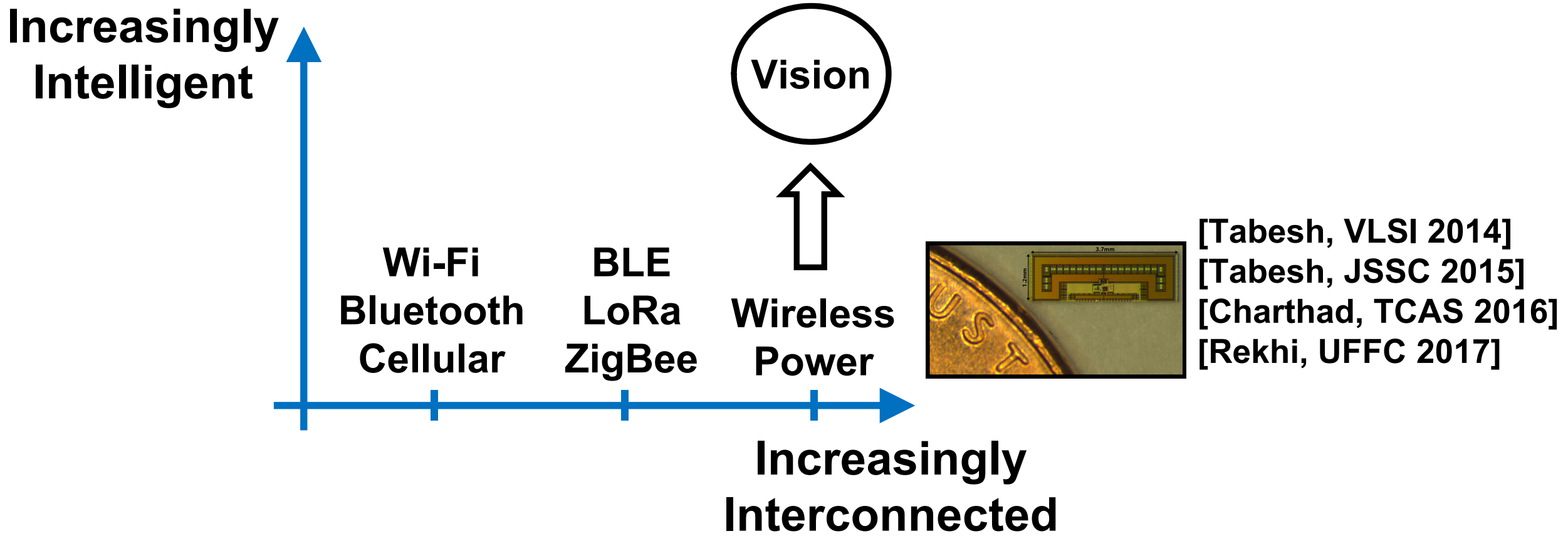


The Evolving Internet of Things

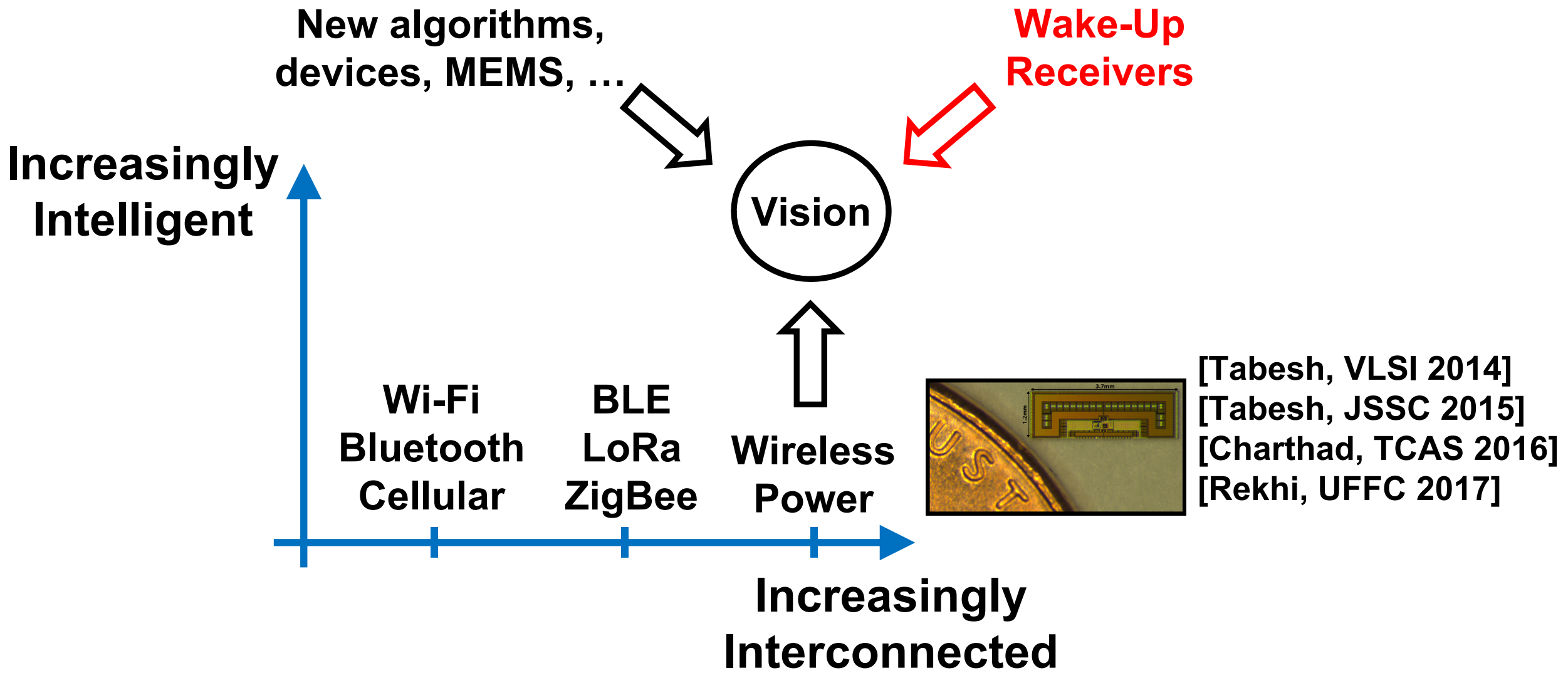


[Tabesh, VLSI 2014]
[Tabesh, JSSC 2015]
[Charthad, TCAS 2016]
[Rekhi, UFFC 2017]

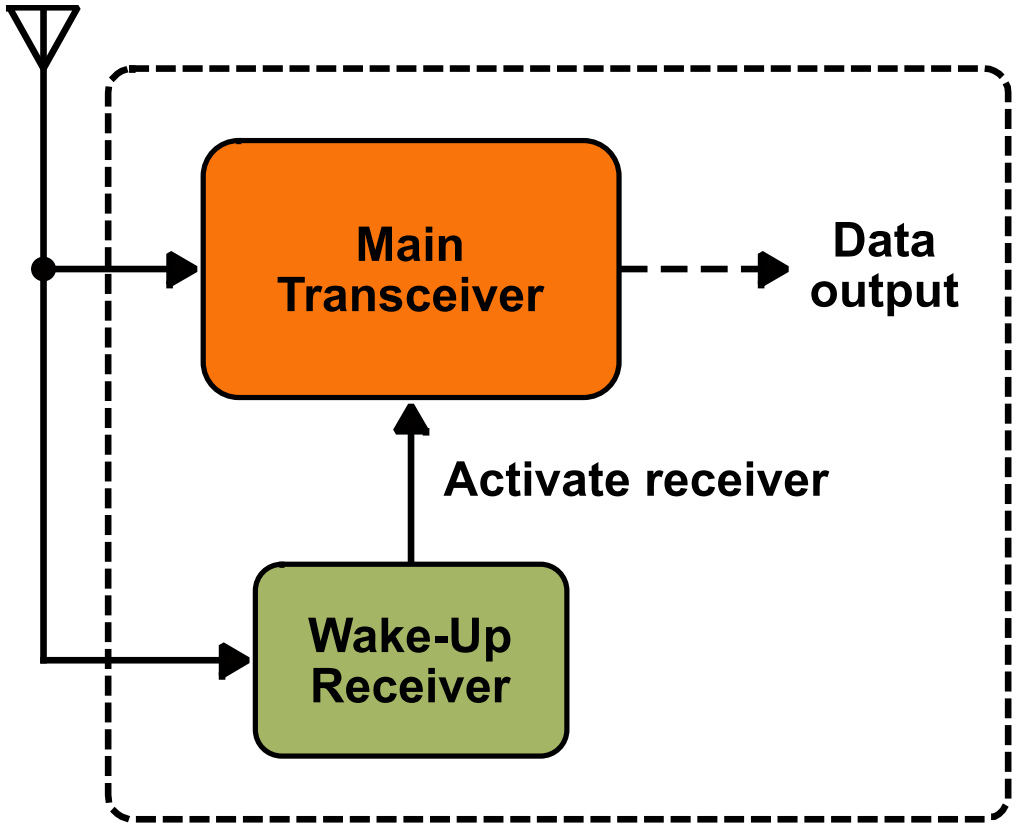
The Evolving Internet of Things



The Evolving Internet of Things



Wake-Up Receivers

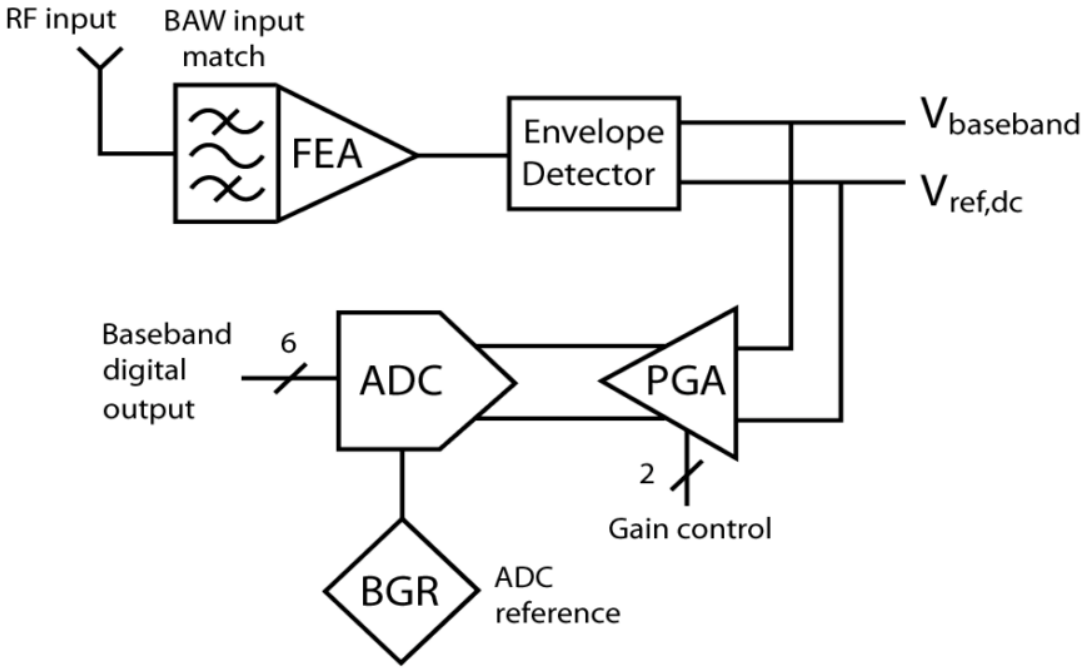


[Cheng, TCAS-I 2017]

- Keeps main node off until needed
- Continuously listens for signature
- Allows intermittent operation

Wake-Up Receivers

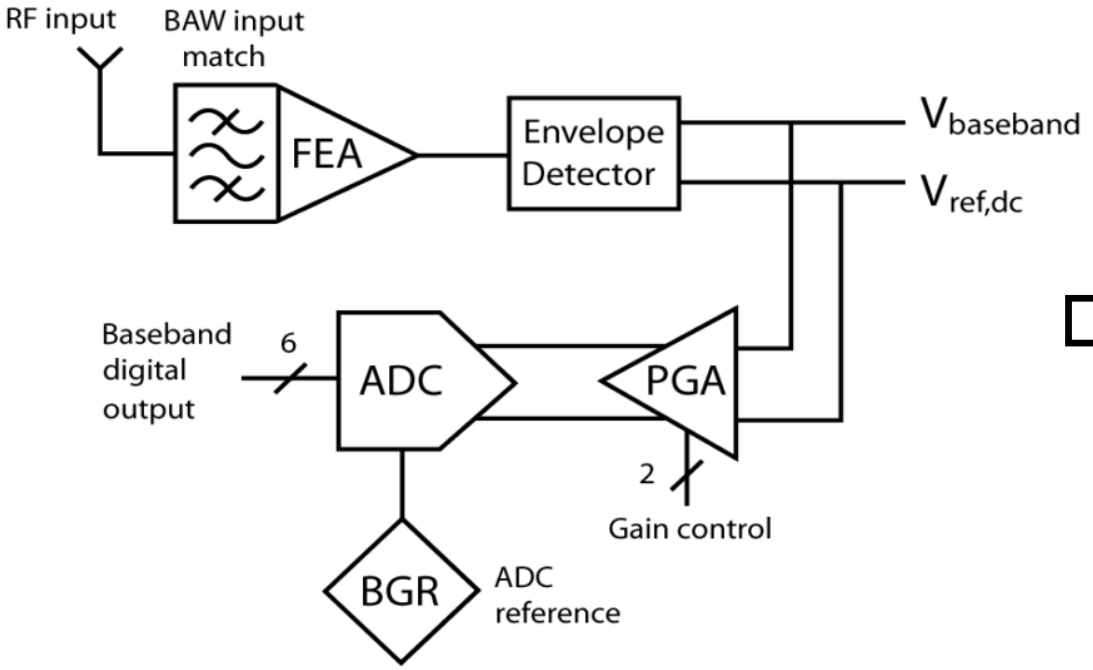
[Pletcher, CICC 2007]



Sens = –56 dBm
Power = 65 µW

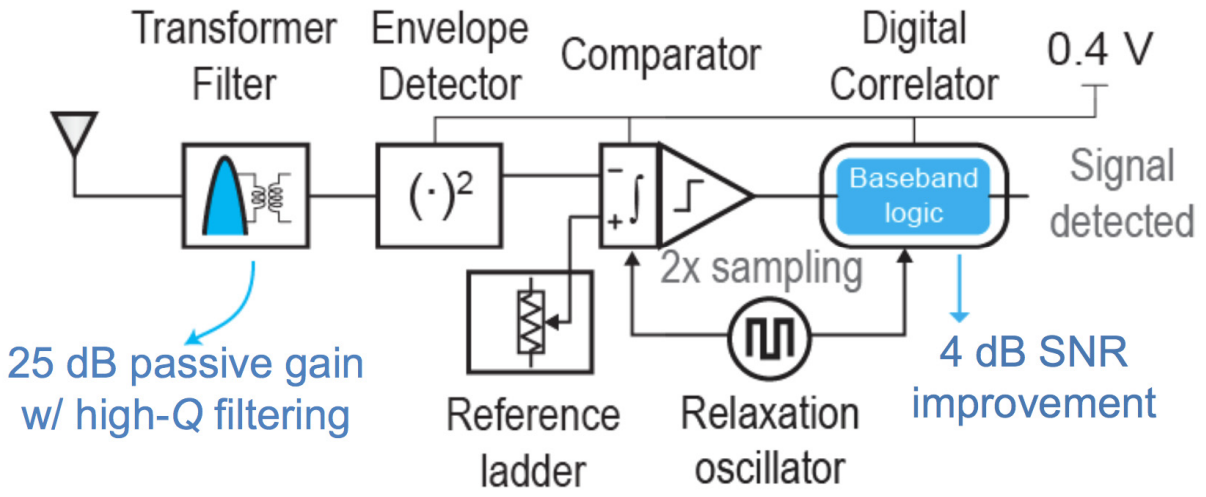
Wake-Up Receivers

[Pletcher, CICC 2007]



Sens = –56 dBm
Power = 65 µW

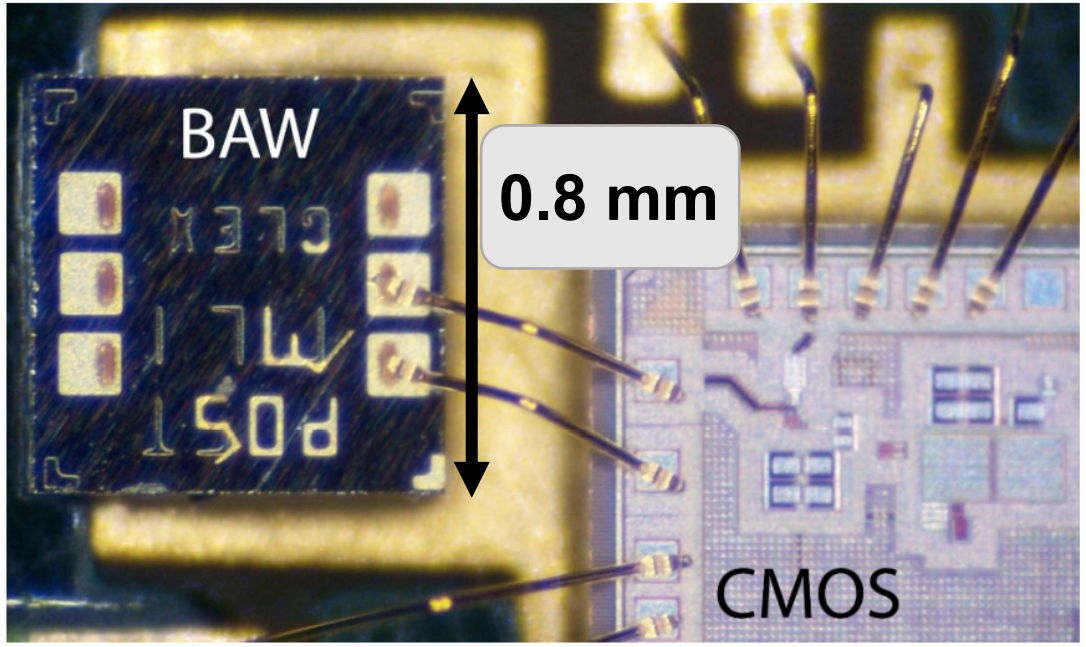
[Jiang, ISSCC 2017]



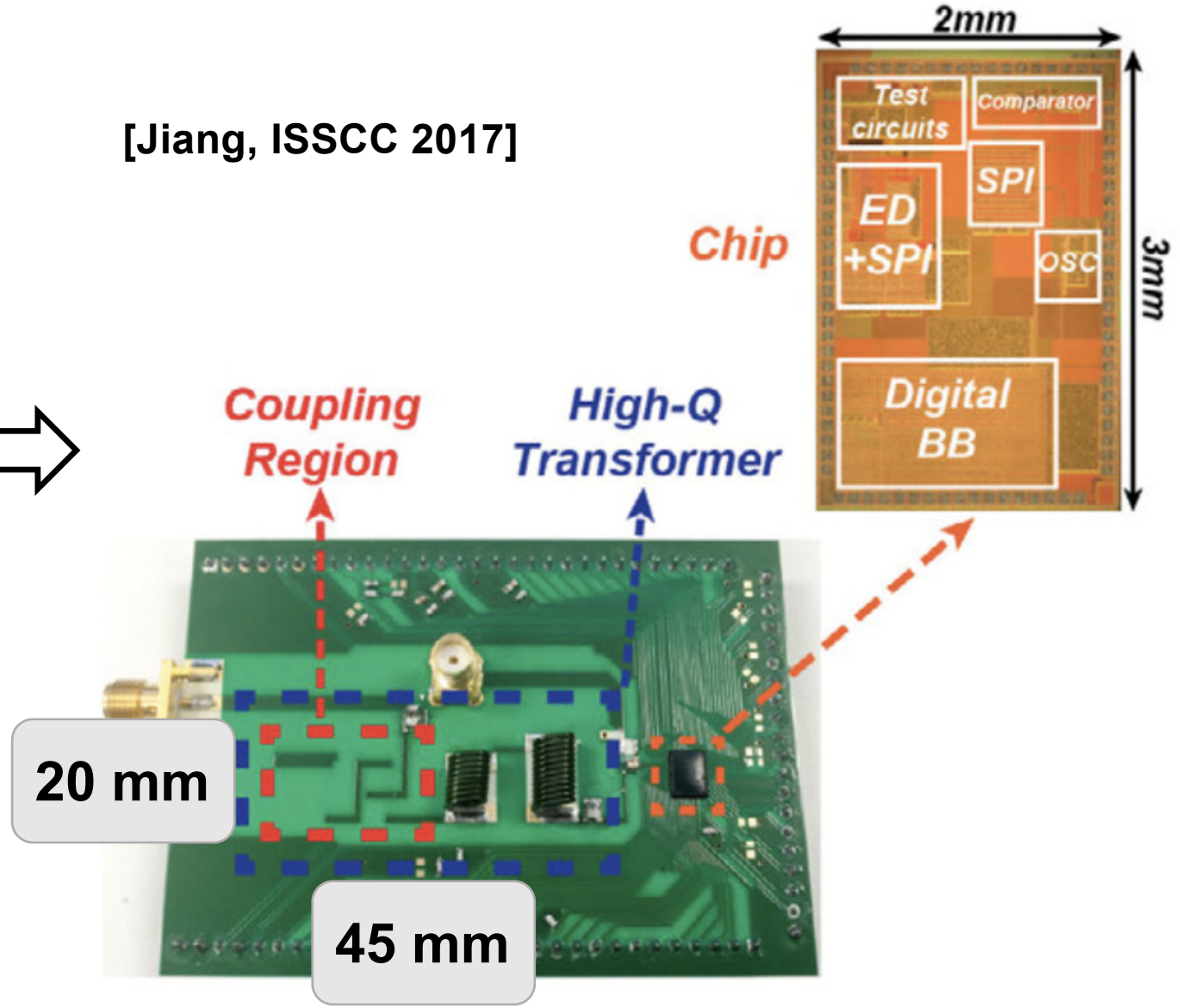
Sens = –69 dBm
Power = 4.5 nW

Area as a Resource

[Pletcher, CICC 2007]



[Jiang, ISSCC 2017]



Our Approach

- **Antenna size ~ wavelength for efficient signal extraction [Wheeler, *Proc. IRE*, ’47]**

Our Approach

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- **Change mode of communication to ultrasound**

Our Approach

- **Antenna size ~ wavelength for efficient signal extraction [Wheeler, *Proc. IRE*, ’47]**
- **Change mode of communication to ultrasound**
- **Low carrier frequency → high-impedance interface**

Our Ultrasonic Wake-Up Receiver

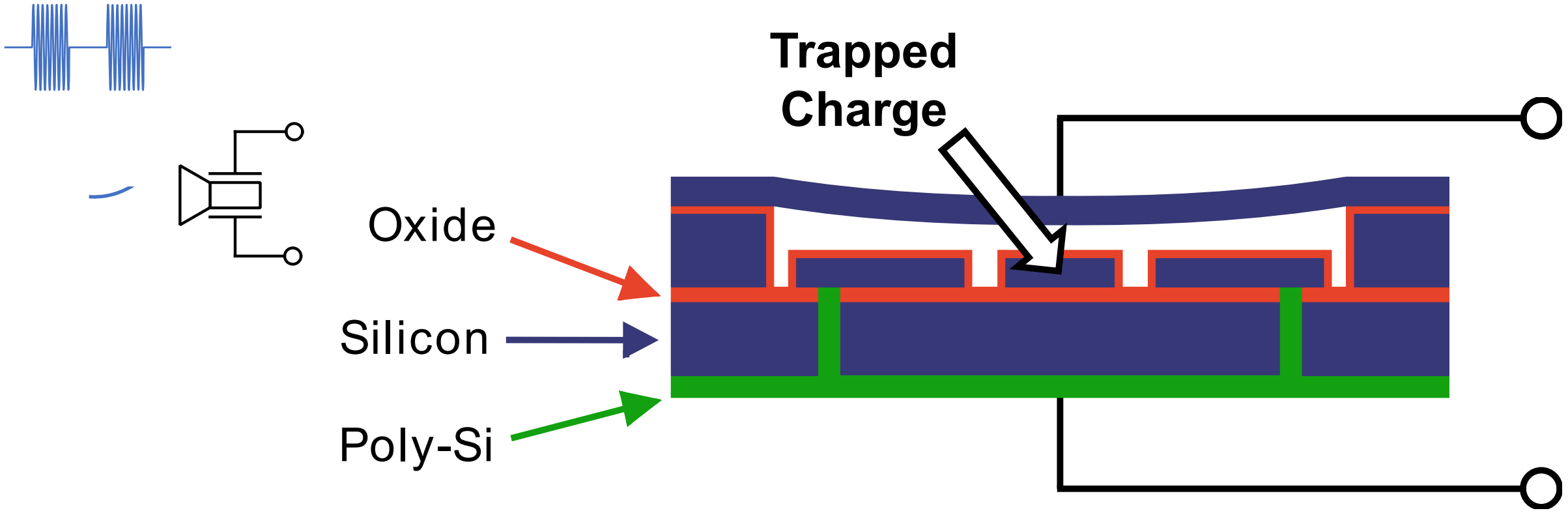
Competitive sensitivity (-59.7 dBm)

Low-power operation (8 nW)

Small size (14.5 mm^2)

Robust to RF and US interference

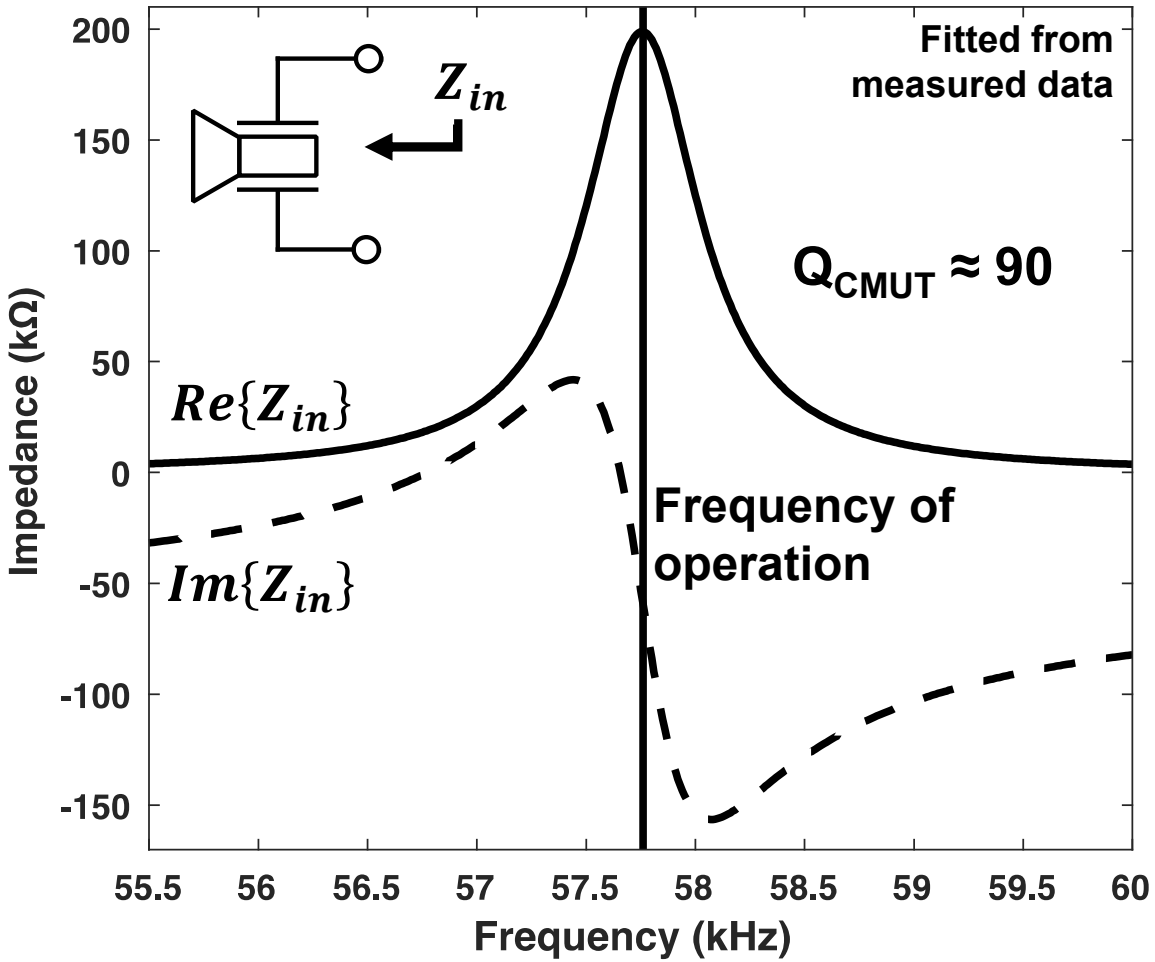
Precharged CMUT as Antenna



[Min-Chieh Ho and Pierre Khuri-Yakub, IUS 2012]

Cross-section of capacitive micromachined ultrasonic transducer (CMUT)

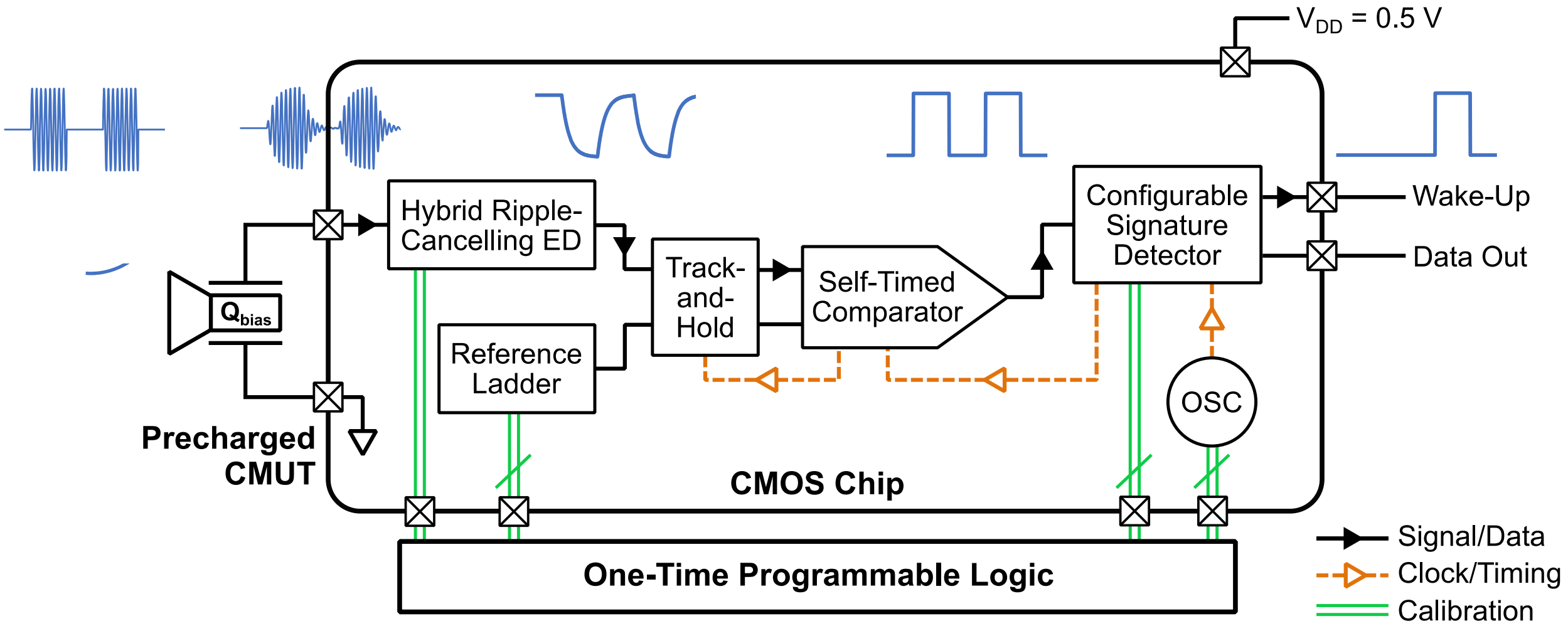
High-Impedance Interface



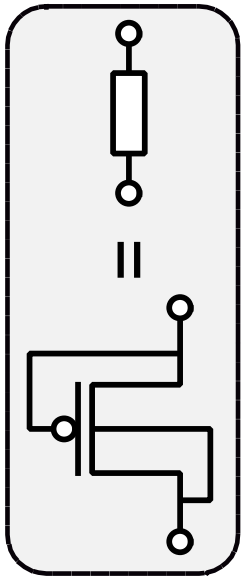
Precharged CMUT impedance

- **Trapped charge leads to resonant behavior**
- **Frequency can be chosen to achieve high impedance**
- **High impedance replaces need for power-hungry gain**
- **No extra area needed**

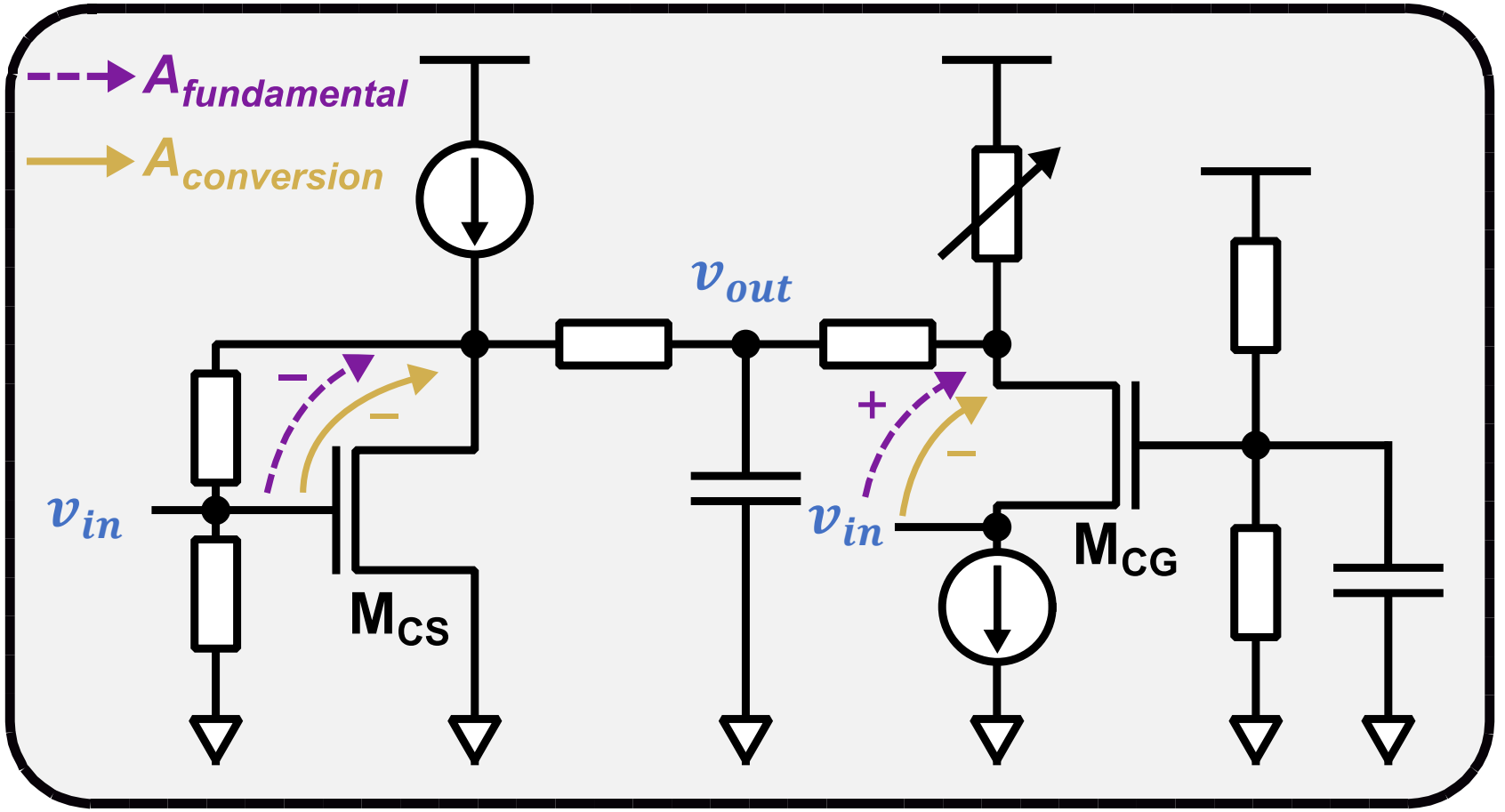
Block Diagram of our WuRX



Hybrid CS-CG Ripple-Cancelling ED



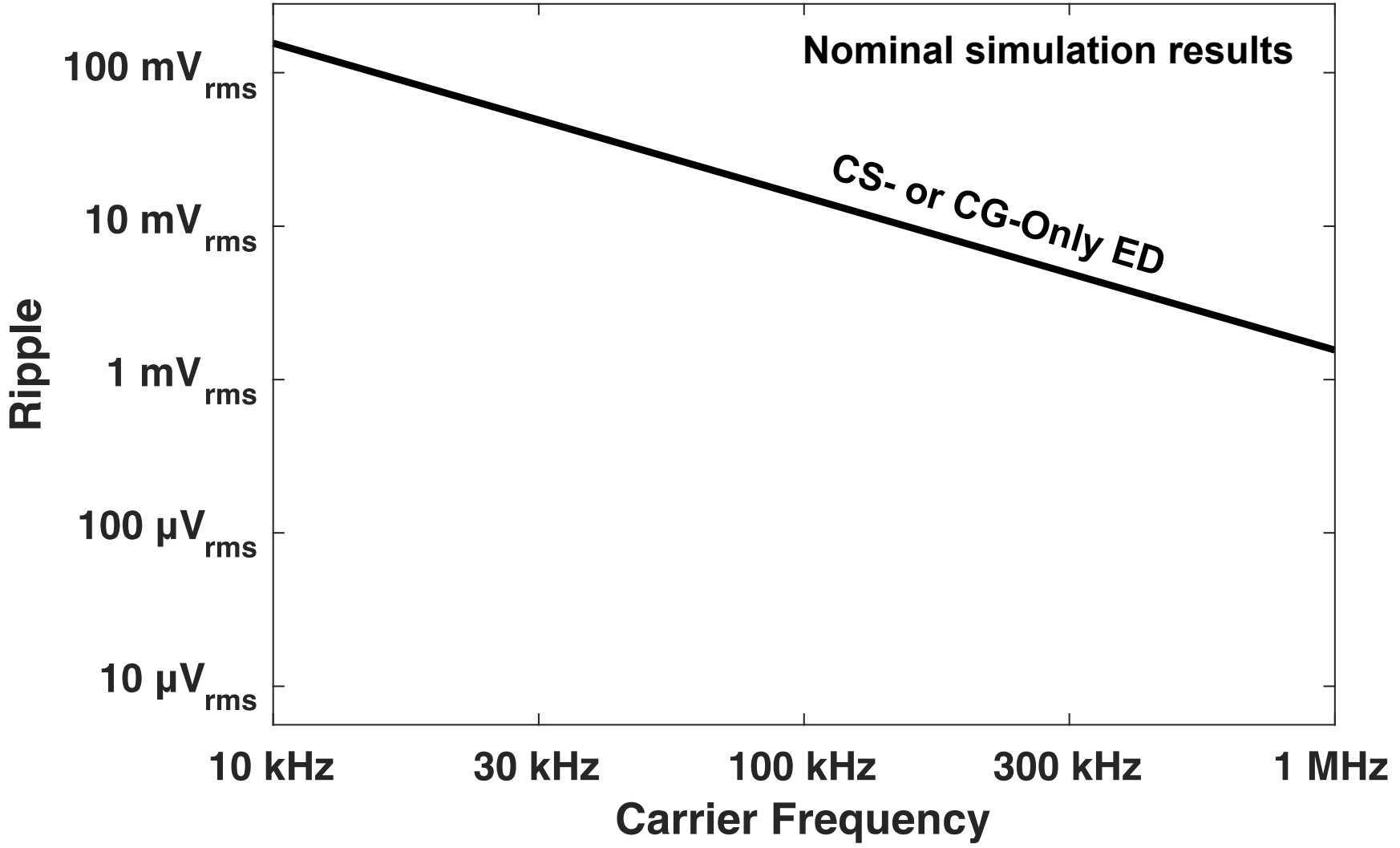
PMOS pseudo-R



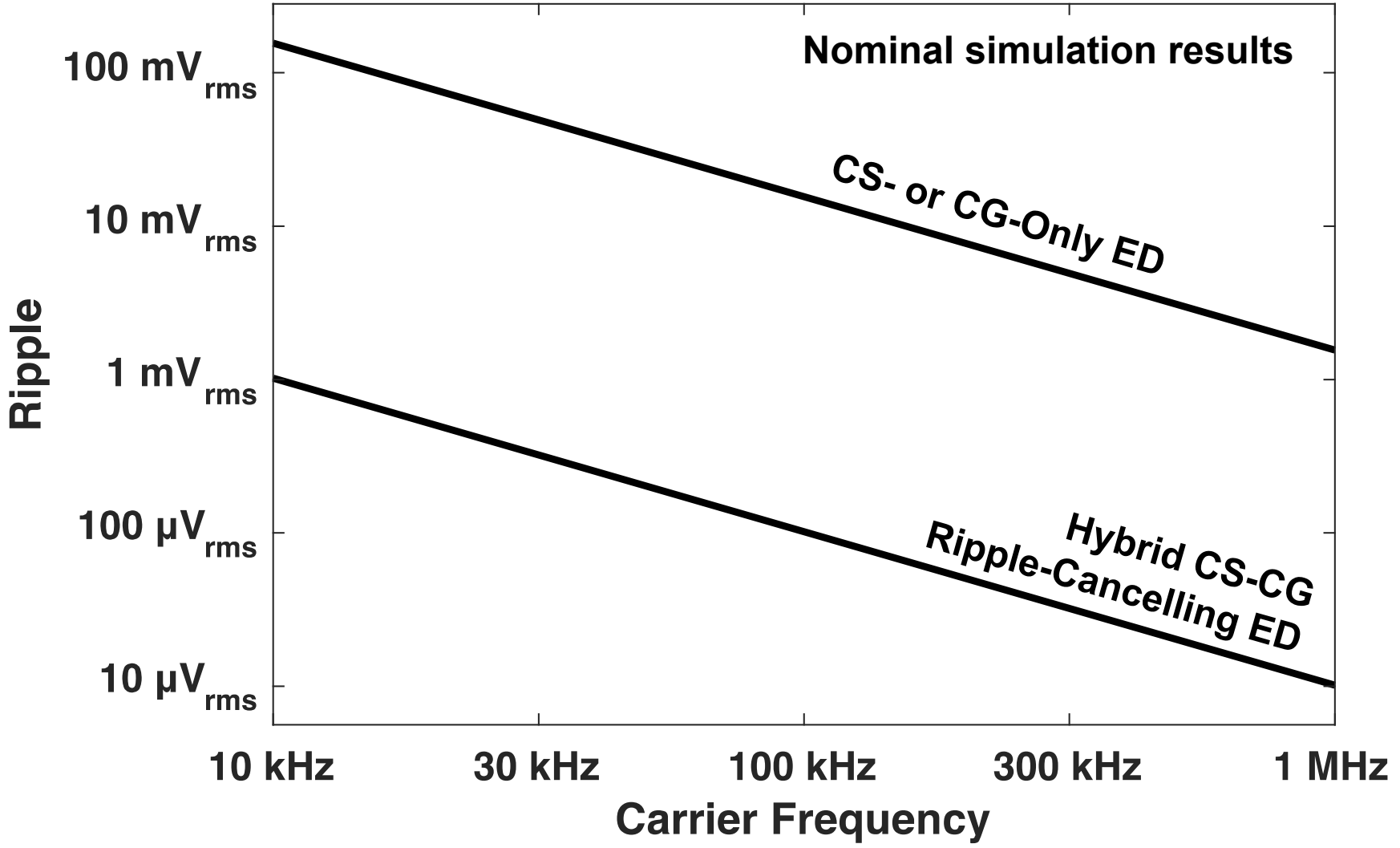
Ratiometric biasing to combat pseudoresistor variation

M_{CS}, M_{CG}: deep N-well devices with body tied to gate (not shown) to avoid drop in $A_{conversion}$

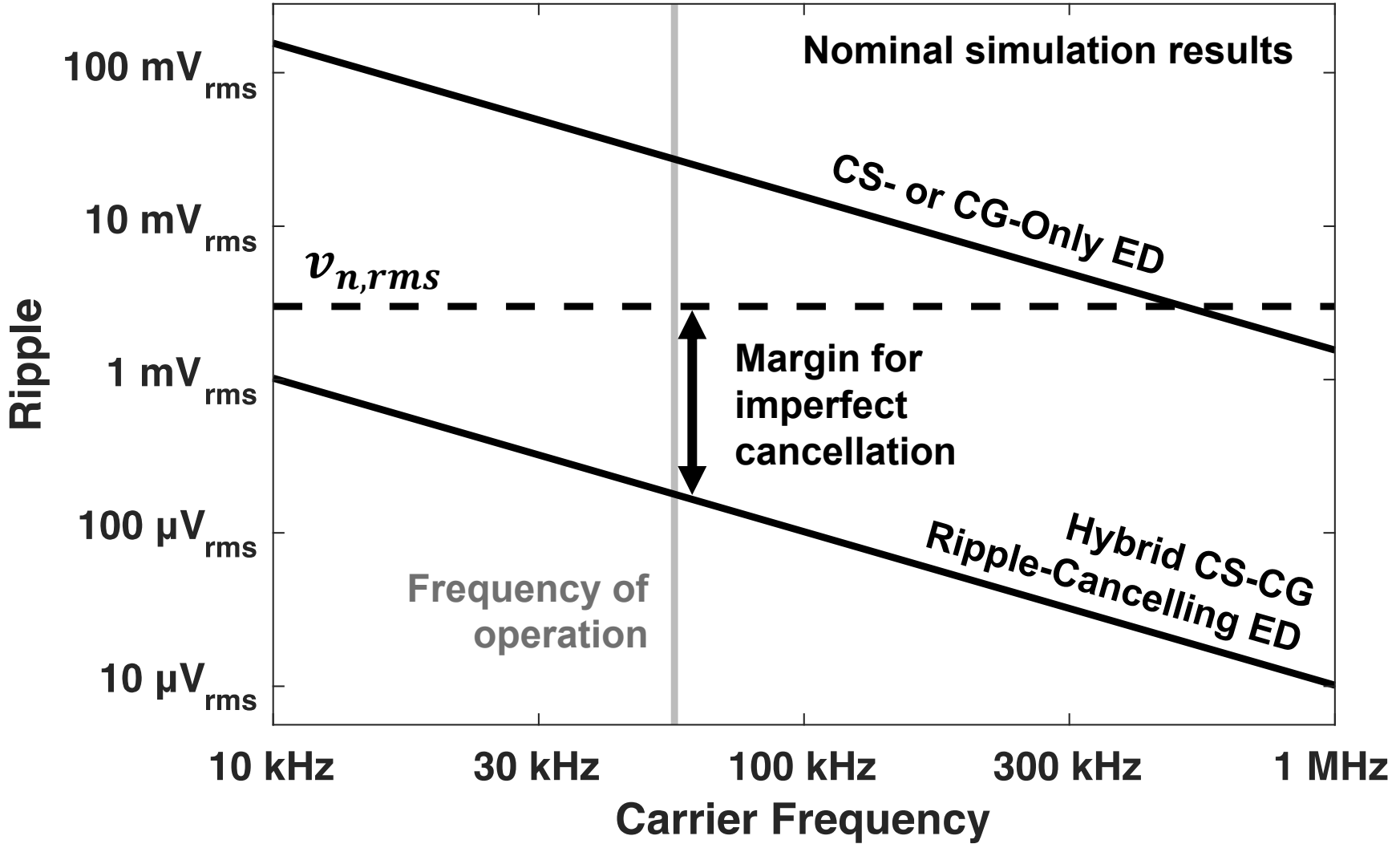
Hybrid CS-CG Ripple-Cancelling ED



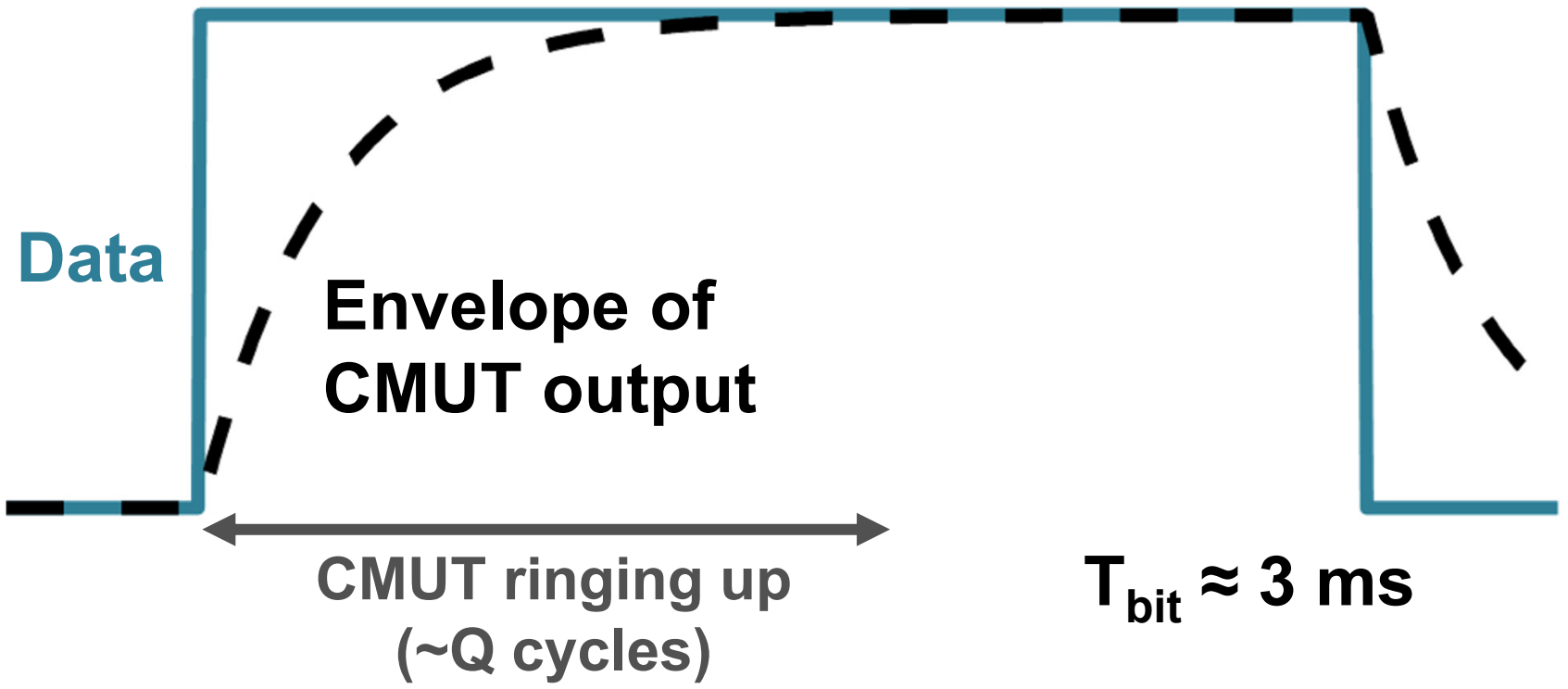
Hybrid CS-CG Ripple-Cancelling ED



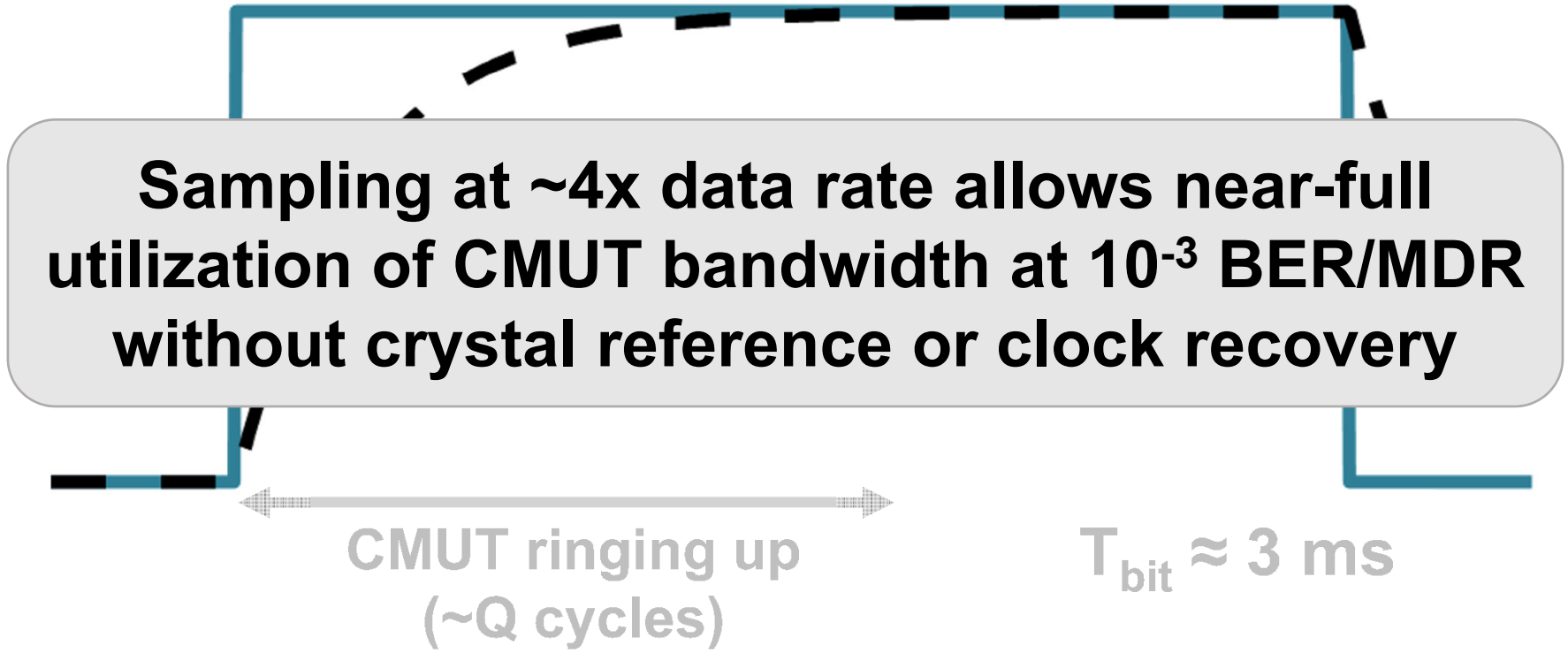
Hybrid CS-CG Ripple-Cancelling ED



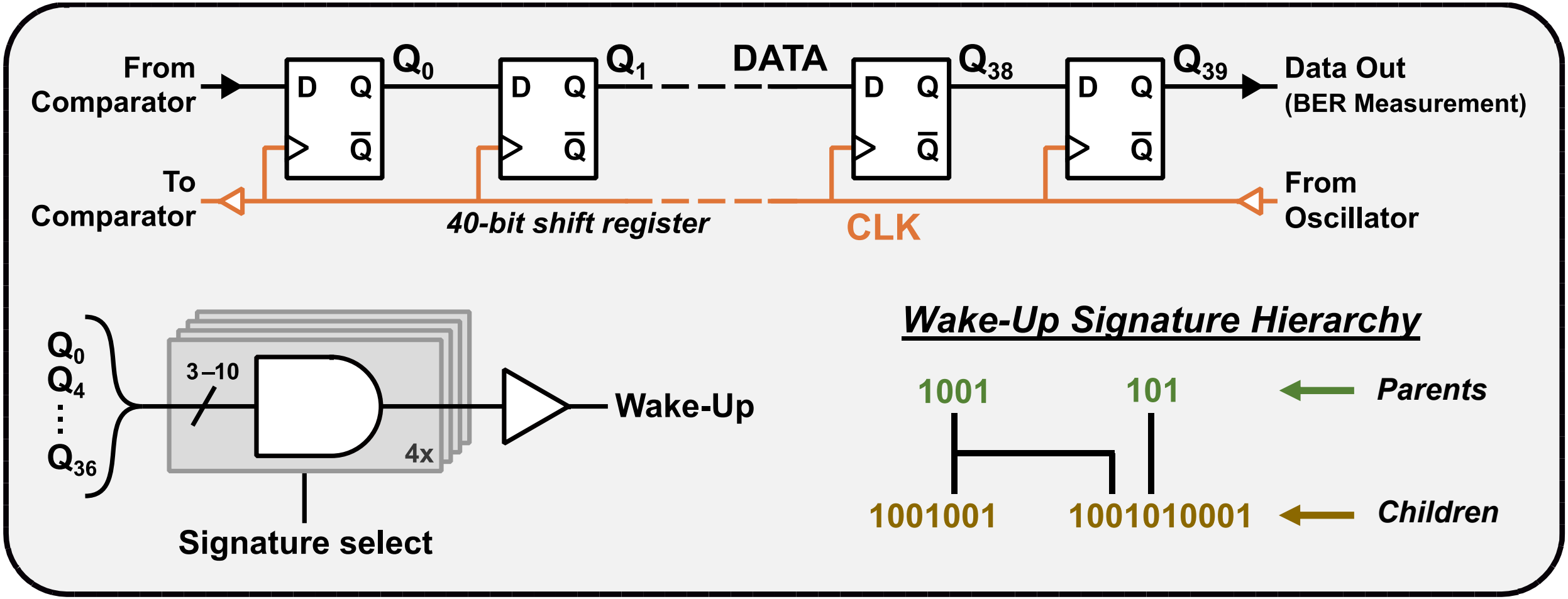
Sampling



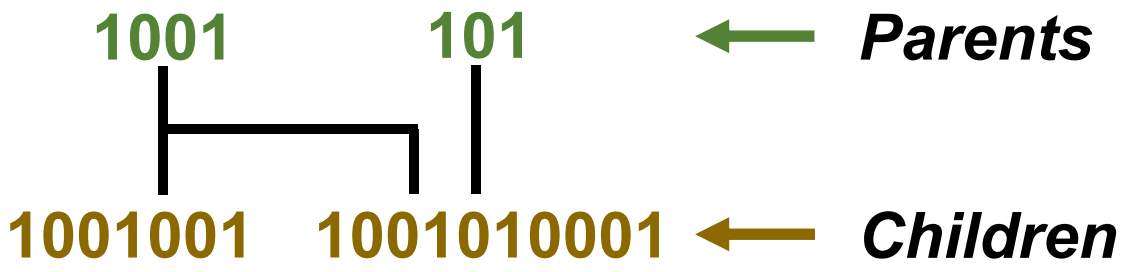
Sampling

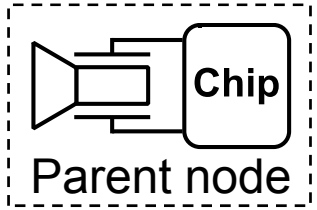
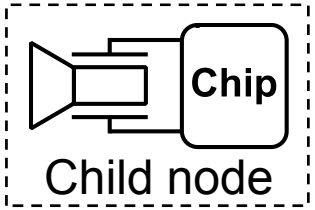


Configurable Signature Detector

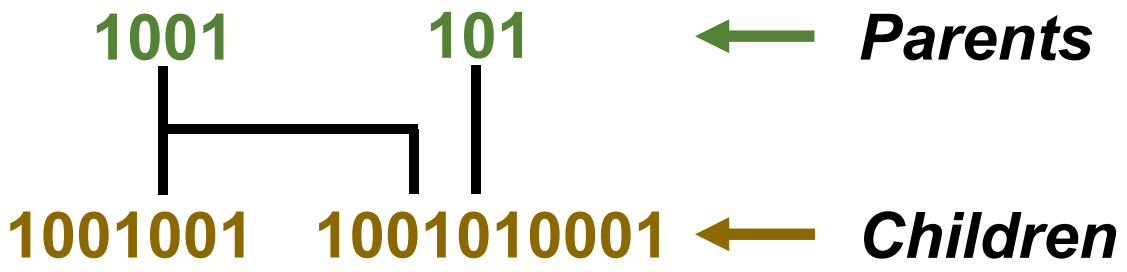


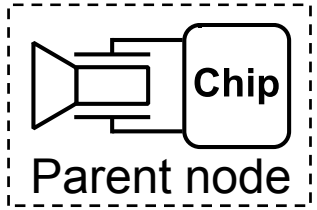
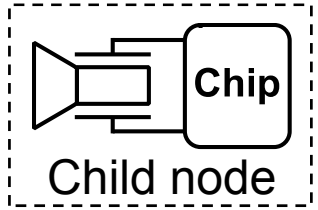
Configurable Signature Detector

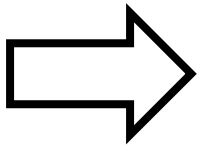


Transmitted Signature ⇩	 Parent node	 Child node
1001001 1001010001	✓	✓
101 1001	✓	X

Configurable Signature Detector

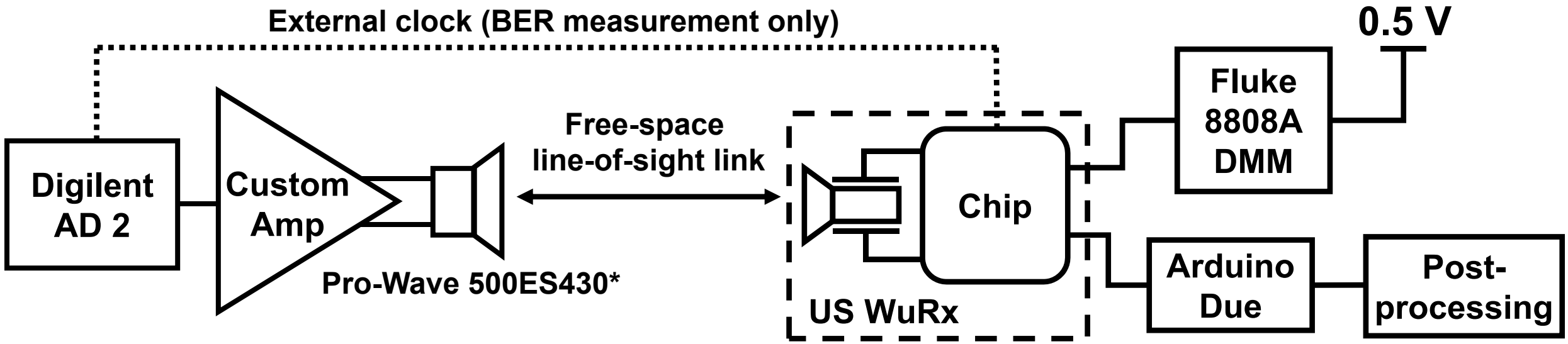


Transmitted Signature ⇩	 Parent node	 Child node
1001001 1001010001	✓	✓
101 1001	✓	X



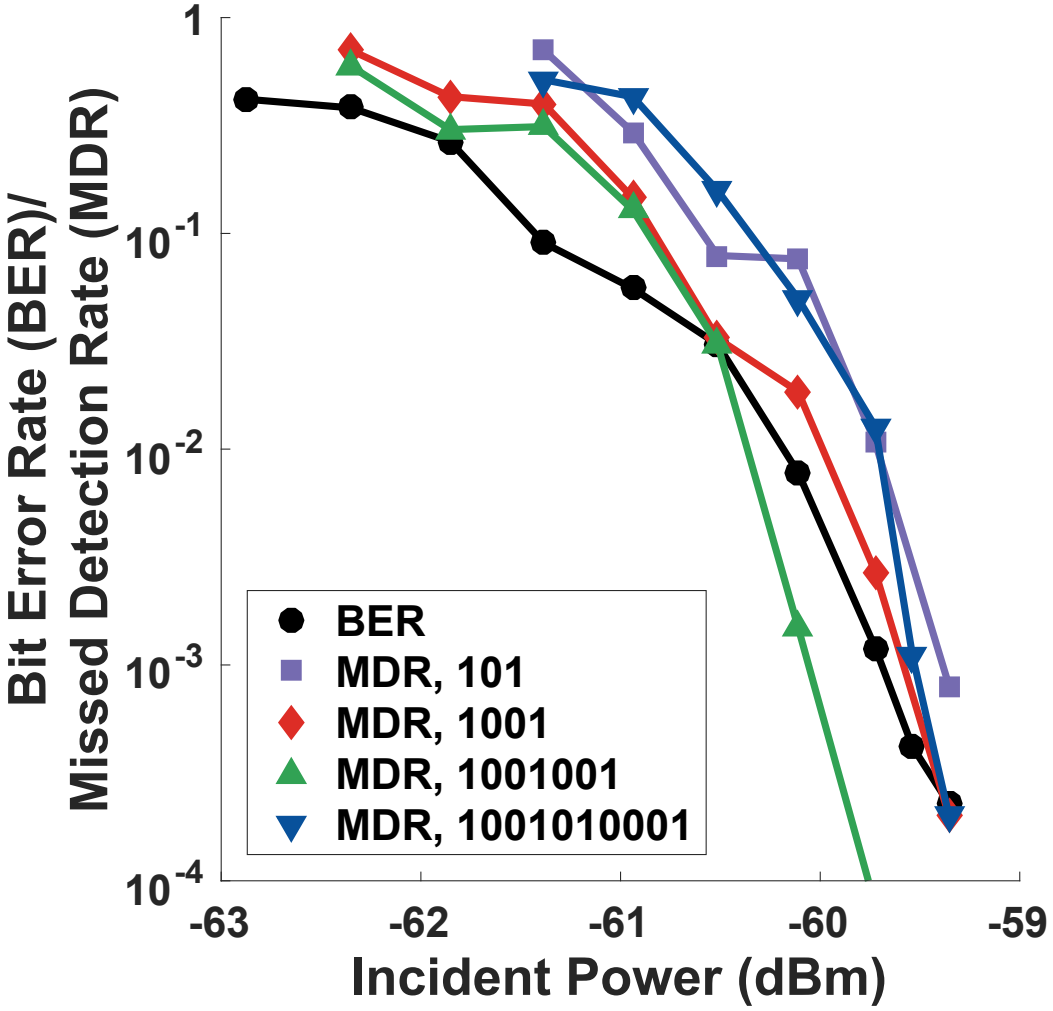
Children nodes cannot be awoken without also waking up all parents within range

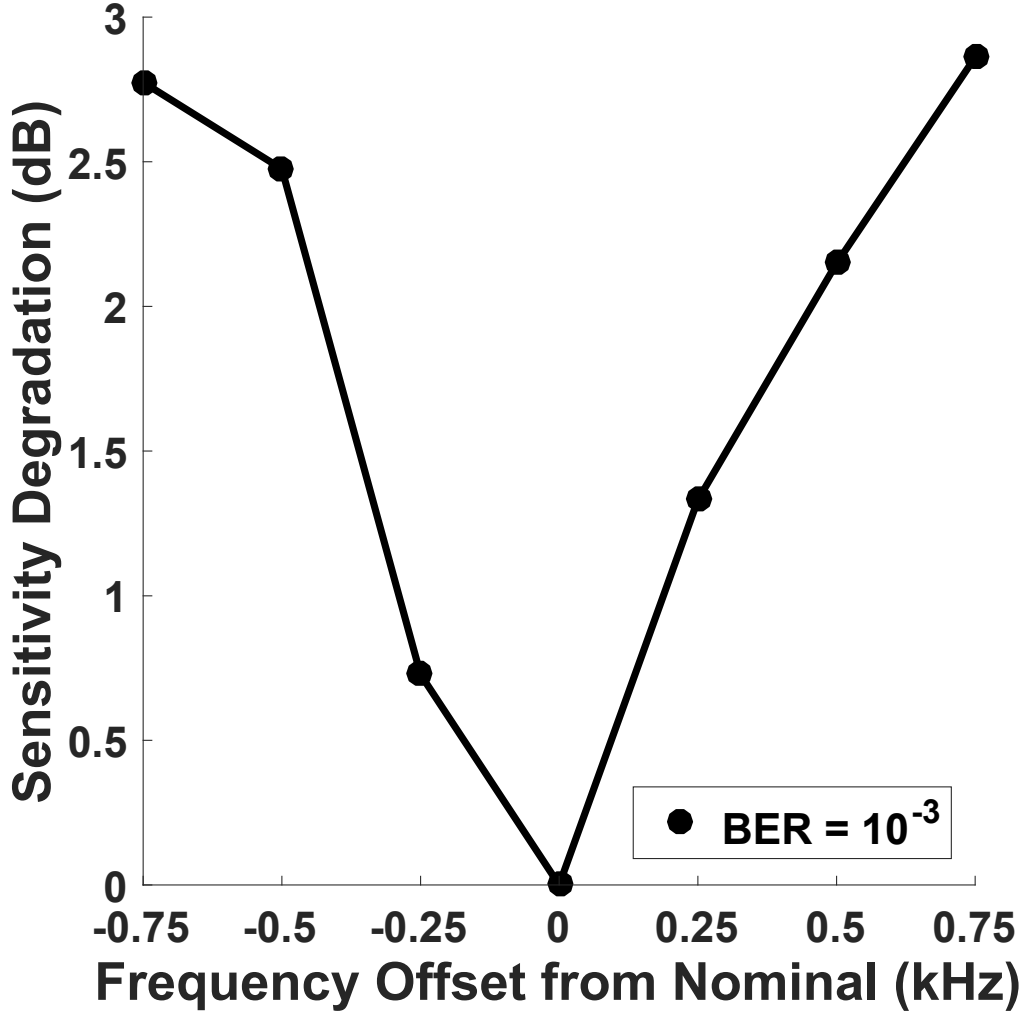
Wireless Characterization: Setup



*Off-the-shelf broadband ultrasonic transducer, not optimized for signature transmission

Wireless Characterization: Results





Interference Tests

CIR Test

Modulated carrier

CW interferer

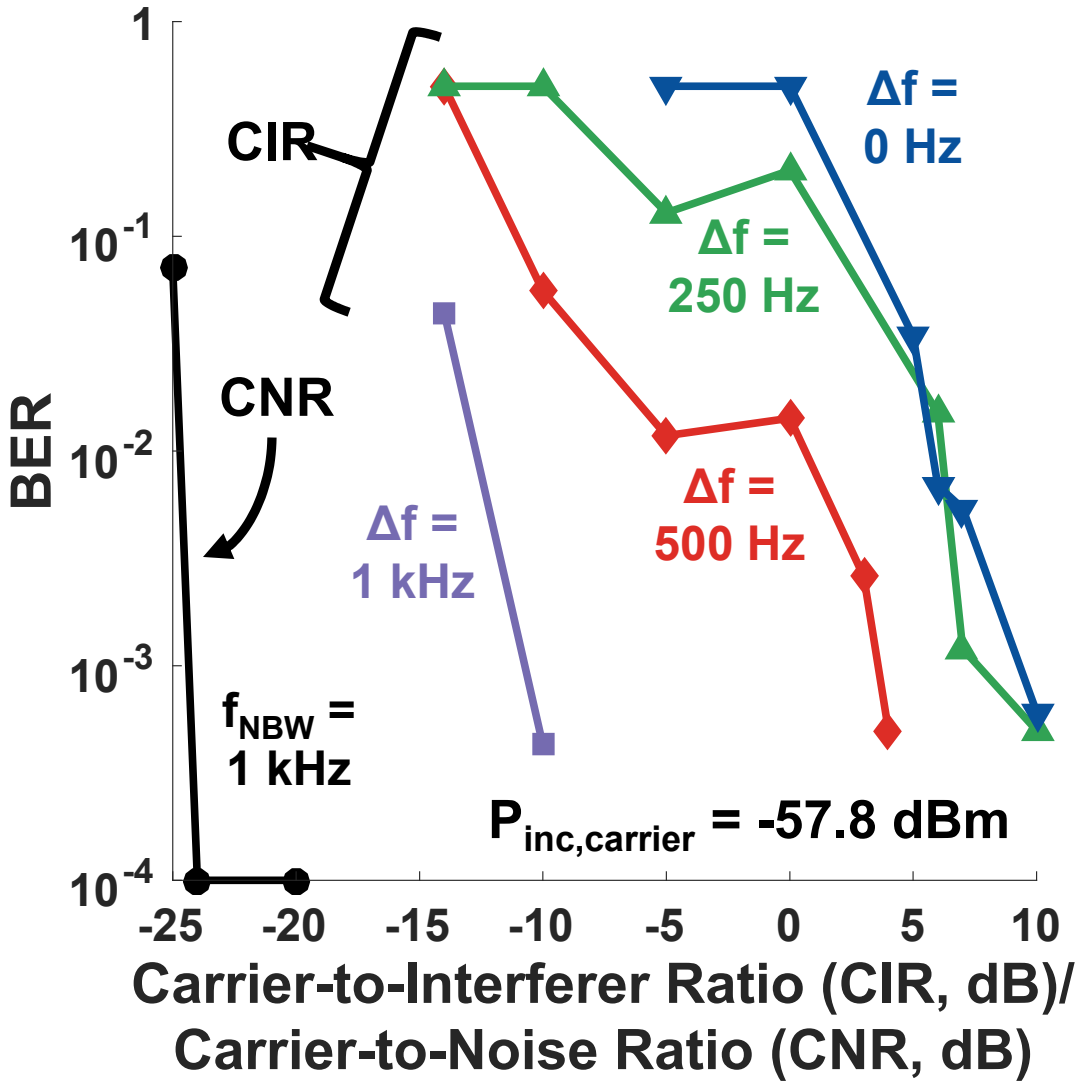
Δf

CNR Test

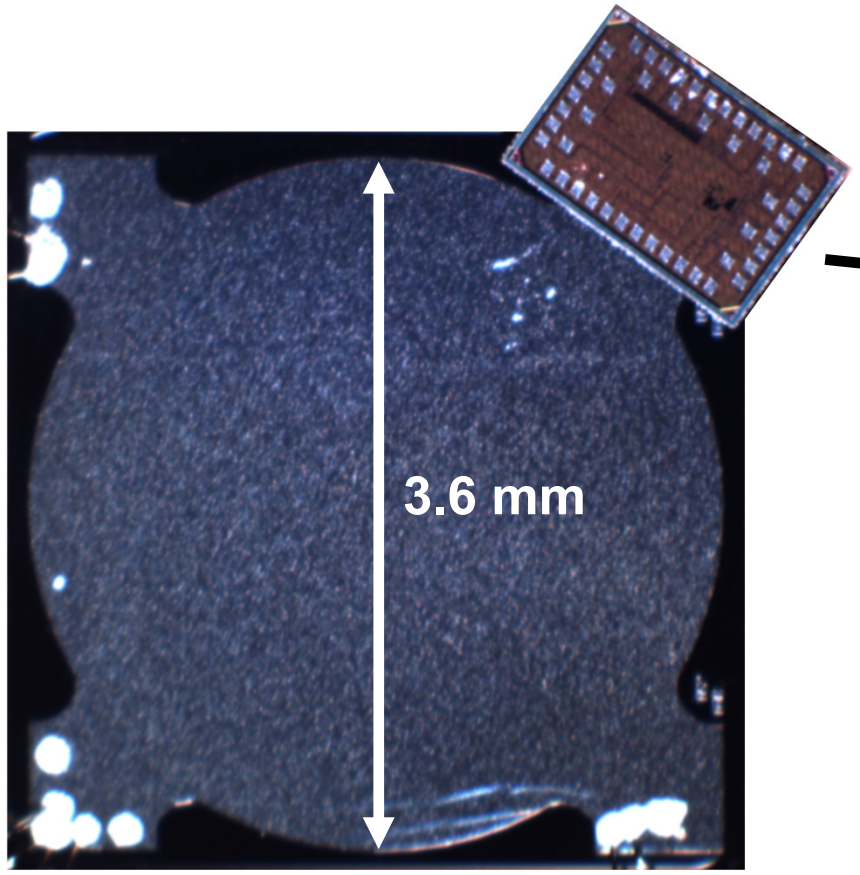
Modulated carrier

In-band noise

f_{NBW}

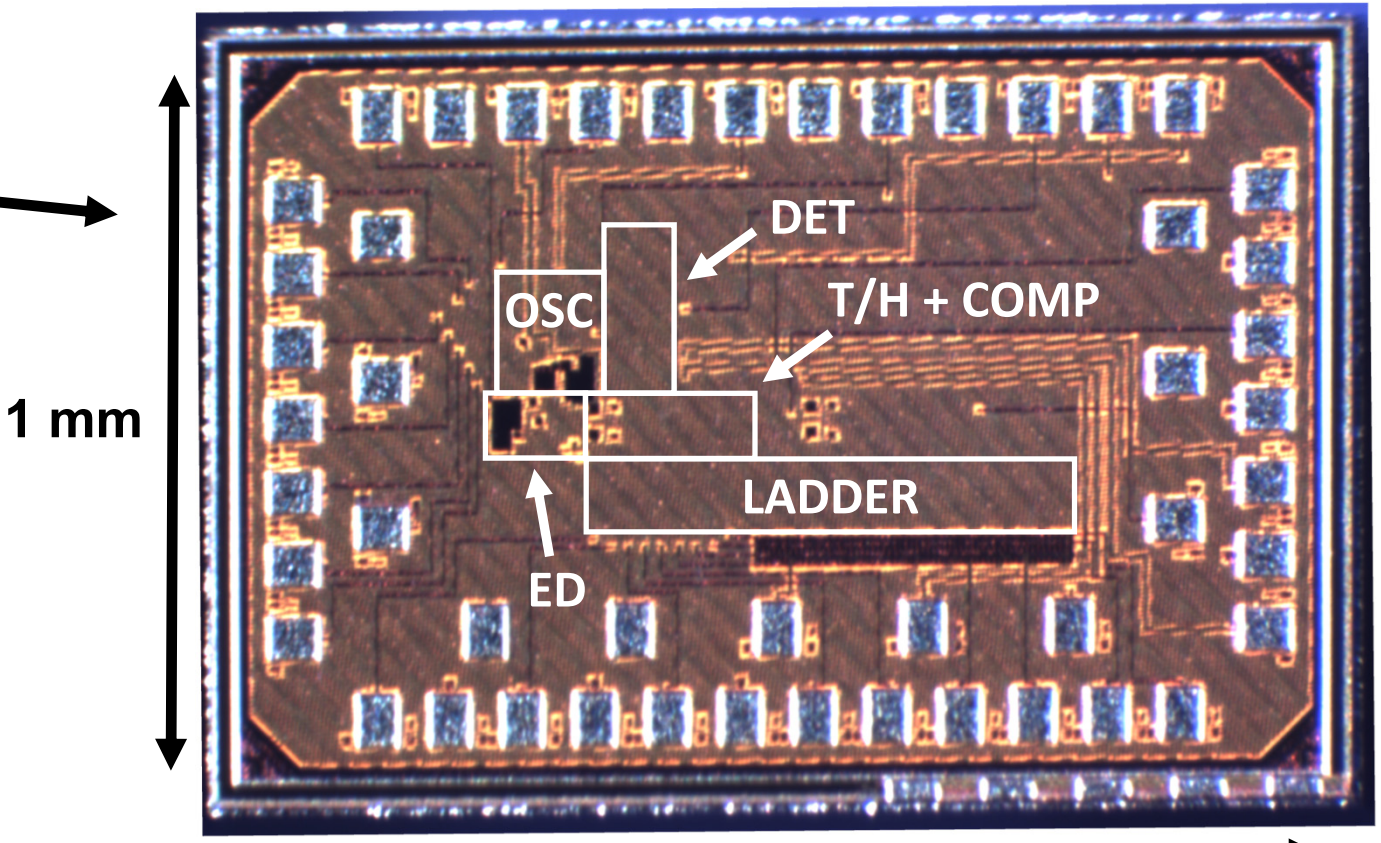


CMOS + CMUT Micrograph

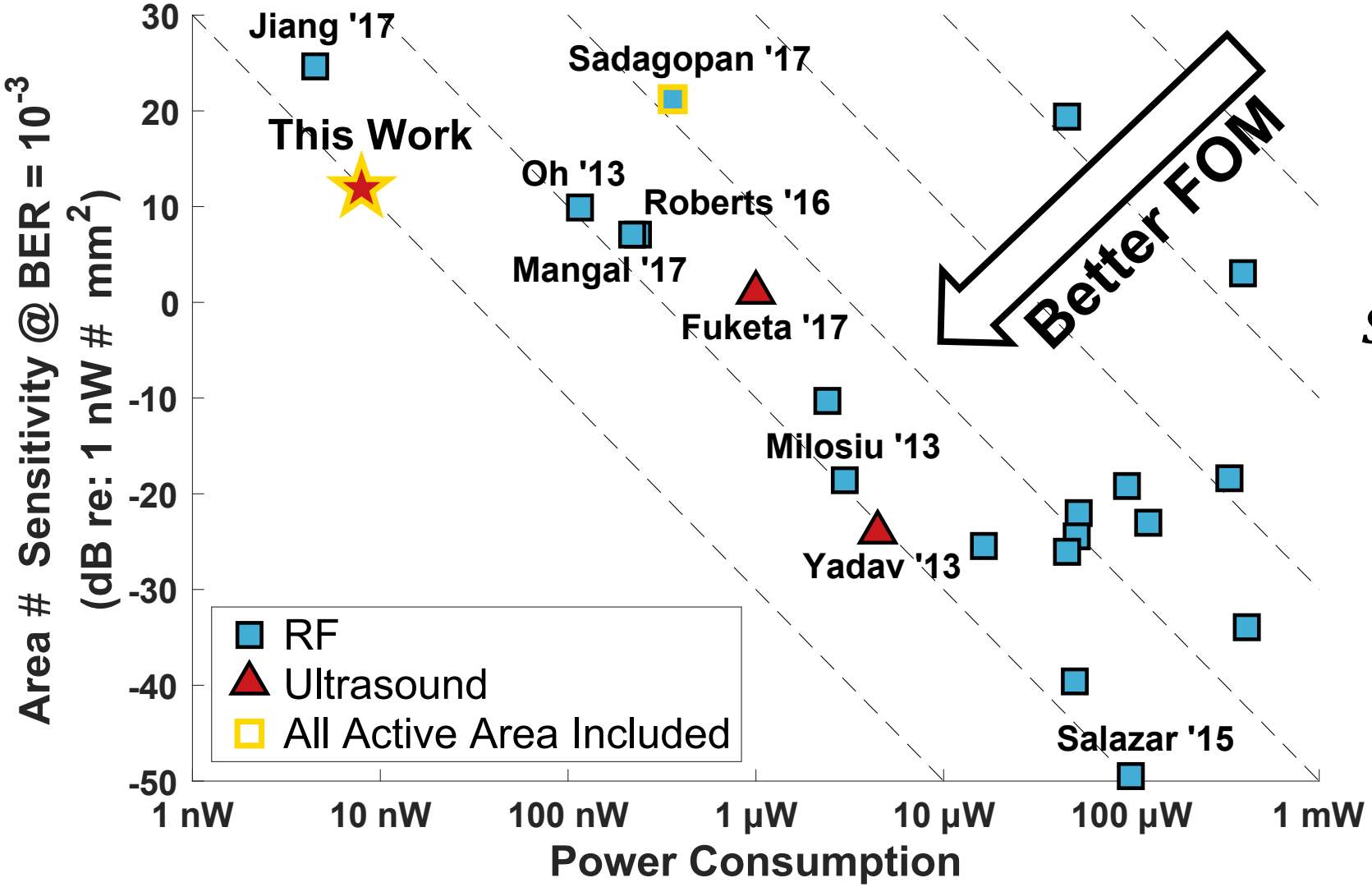


Precharged CMUT

CMOS chip



Comparison



$$FOM = Sensitivity \cdot Power^2 \cdot Area$$

- Large wake-up distance
- Long lifetime
- Unobtrusive, ubiquitous operation

Comparison

	Yadav JSSC '13	Salazar ISSCC '15	Roberts ISSCC '16	Fuketa TCAS-II '17	Jiang ISSCC '17	Sadagopan RFIC '17	**This Work**
Technology	65 nm	65 nm	65 nm	250 nm	180 nm	65 nm	**65 nm**
Wake-Up Medium	US	RF	RF	US	RF	RF	**US**
Carrier Frequency	40 kHz	2.4 GHz	2.4 GHz	41 kHz	114 MHz	2.4 GHz	**~57 kHz**
Data Rate	250 bps	10 kbps	~8.2 kbps	250 bps	300 bps	2.5 kbps	**336 bps**
Power	4.4 µW	99 µW	236 nW	1 µW	4.5 nW	365 nW	**8 nW**
Sensitivity*	-85 dBm	-97 dBm	-56.5 dBm††	-82.1 dBm#	-65 dBm	-61.5 dBm	**-59.7 dBm**
Area	1.24 mm^2	0.06 mm^2	2.25 mm^2	201 mm^2	906 mm^2	187.5 mm^2	**14.5 mm^2**
FOM**	48.8 dB	50.5 dB	54.5 dB	60.9 dB	37.6 dB	72.5 dB	**30.0 dB**
Wireless Test?	Yes	Not shown	Yes	Yes	Not shown	Yes	**Yes**
Interference Test?	Yes†	Yes	Not shown	No	No	Yes	**Yes**
Multiple Chips Measured?	Not shown	Not shown	Not shown	Not shown	Not shown	Not shown	**Yes 2 (wireless) 20 (electrical)**
Not Included in Area	Transducer, matching, DSP	Antenna, SMD inductors	Antenna, matching	Off-chip L/C/R##	Antenna		

***BER = 10^{-3}, no coding/correlation, where available **Sensitivity·Power^2·Area, dB re: 1 nW^3 mm^2; lower FOM is better**
†Limited to interference present in ambient environment ††With coding
#Estimated ##Transducer area included

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#Estimated ##Transducer area included

Conclusion

Ultrasonic wake-up enables:

High-impedance interface → **competitive sensitivity**

No active gain at carrier → **low-power operation**

Small operation wavelength → **mm-sized system**

Narrowband US w/ signature → **robust to interference**

14.5mm^2 8nW -59.7dBm ultrasonic wake-up receiver for the next-generation IoT

Acknowledgment

- We thank Prof. Pierre Khuri-Yakub and Min-Chieh Ho for fabrication and provision of precharged CMUTs
- We thank Mentor Graphics for use of the Analog FastSPICE (AFS) Platform
- Research conducted with US Govt. support under DoD/AFOSR (NDSEG Fellowship), 32 CFR 168a

A 5.8GHz Power-Harvesting 116μmx116μm "Dielet" Near-Field Radio with On-Chip Coil Antenna

Bo Zhao, Nai-Chung Kuo, Benyuanyi Liu, Yi-An Li, Lorenzo Iotti, Ali M. Niknejad

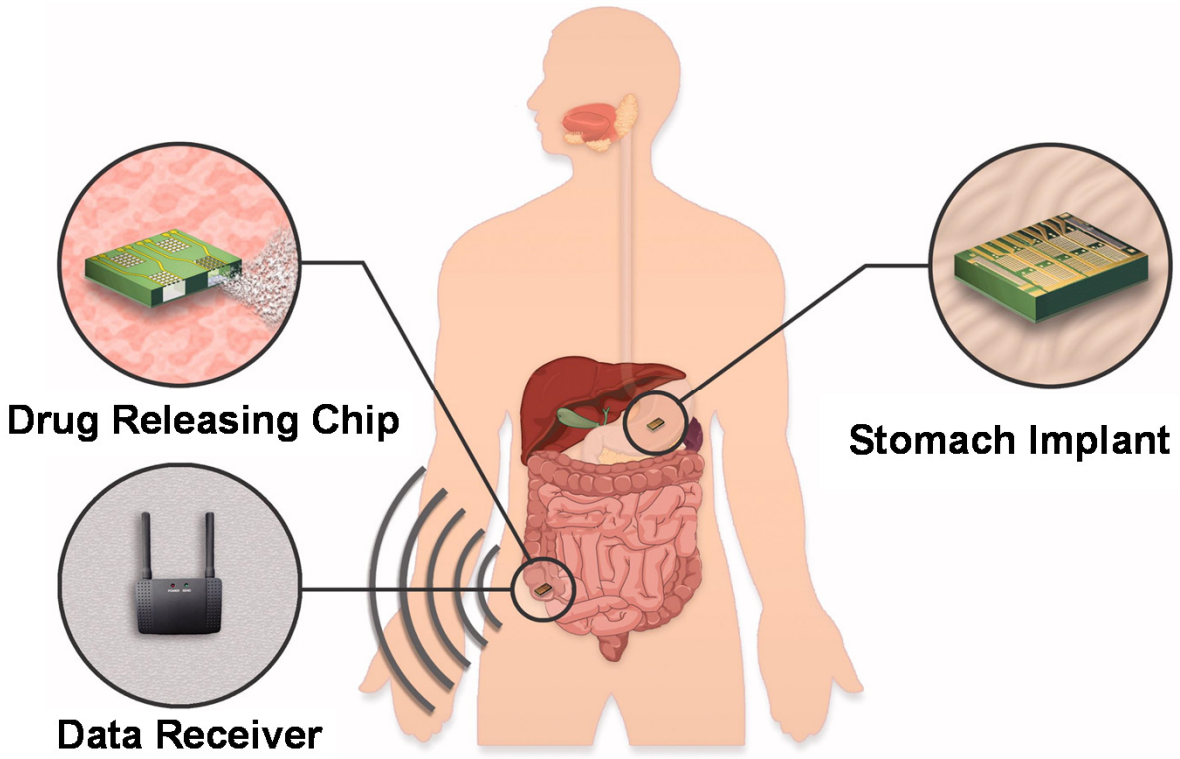
Berkeley Wireless Research Center (BWRC)
University of California, Berkeley
Email: zhaobo@berkeley.edu

Outline

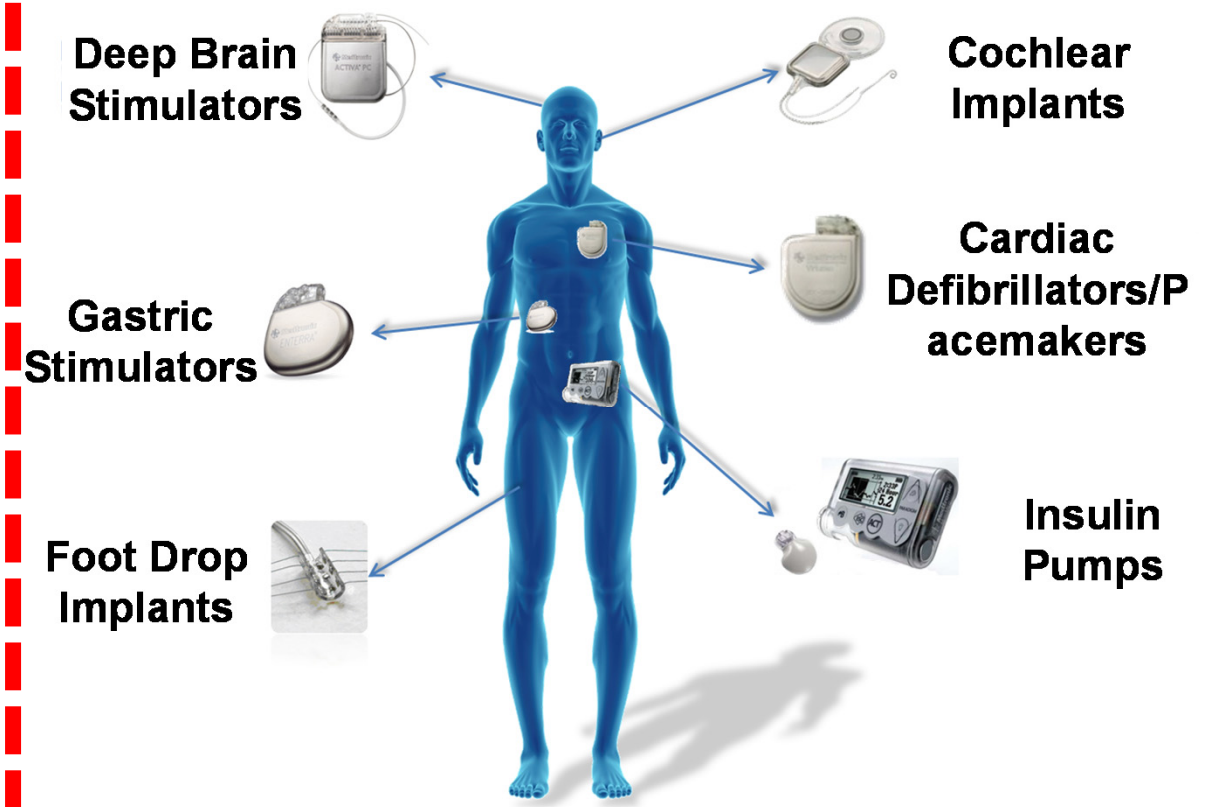
- ❑ **Design Motivation**
- ❑ Proposed Radio System
- ❑ Circuit Details
- ❑ Measurement Results
- ❑ Summary
- ❑ Acknowledgements

Application Scenario

Drug Delivery



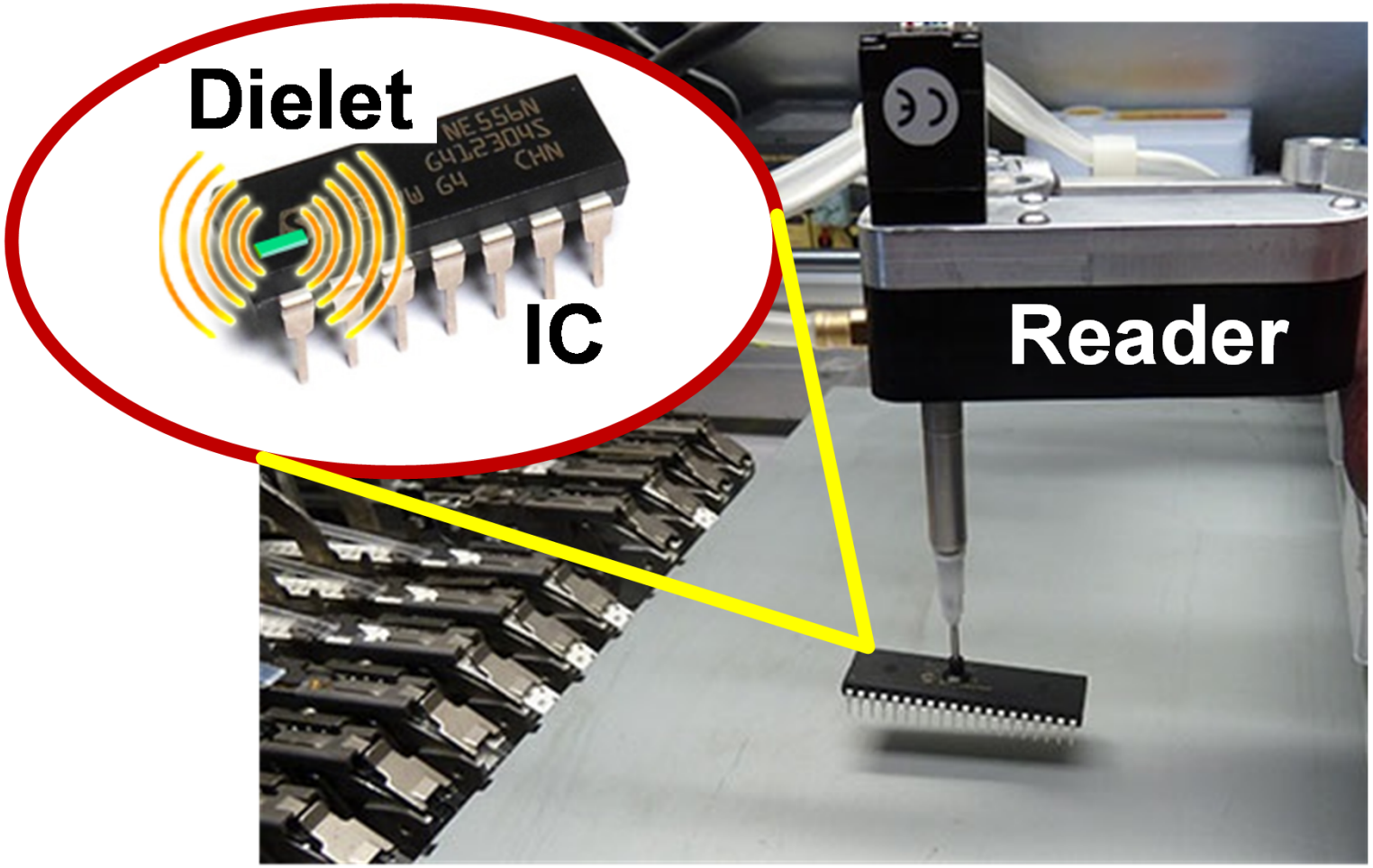
Medical Implants



- ❑ Access to tiny spaces
- ❑ Alleviate surgical pain

Picture Sources: [1,2]

DARPA SHIELD (Kerry Bernstein)



- ❑ The “Dielet”:
  - ➢ Hardware root of trust
  - ➢ Inserted into IC packaging
  - ➢ Checked by Reader Machine
  - ➢ Short range (~1mm)
  - ➢ Tiny, cheap, and foolproof

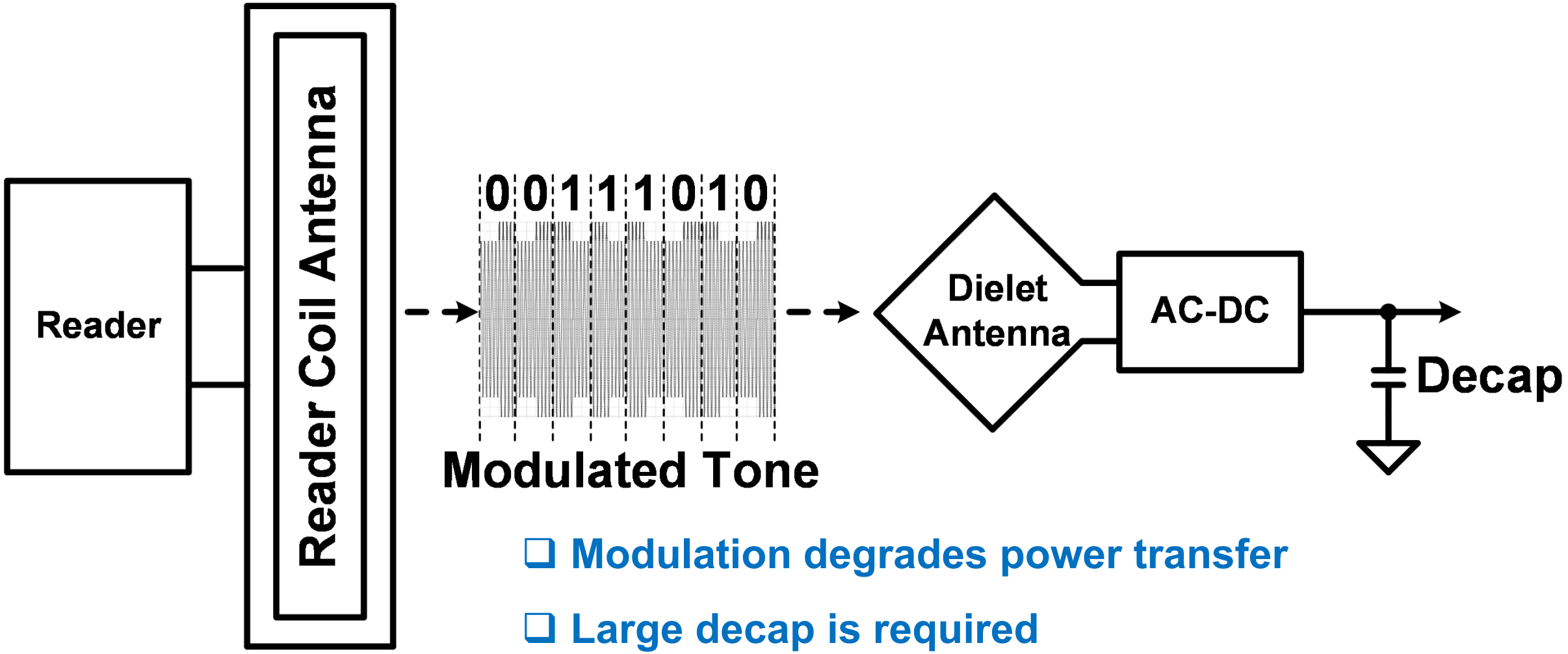
Picture Sources: [3-5]

Design Challenges -- Power Transfer

- 1/10 smaller means 1/100 power efficiency

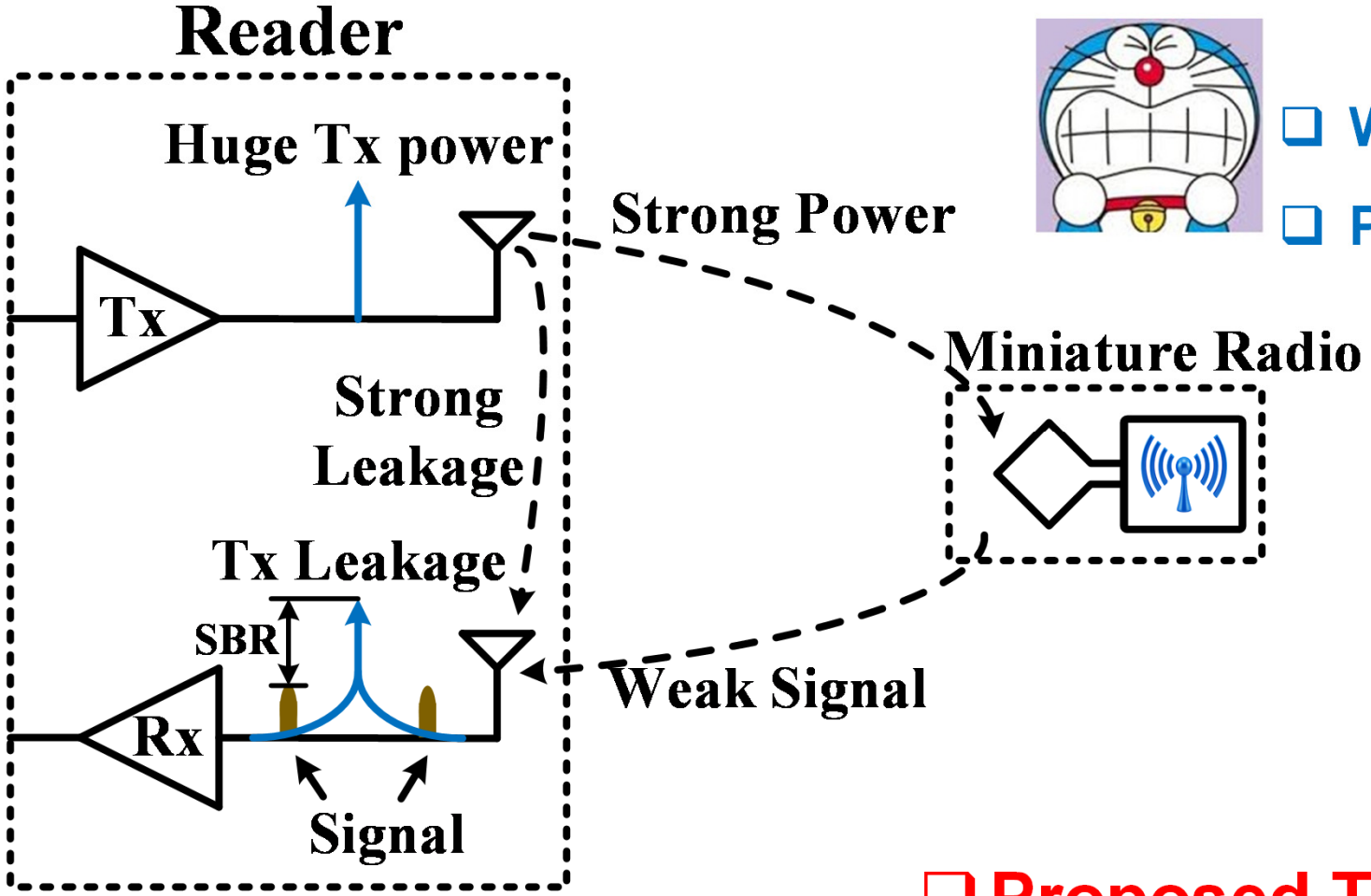
Picture Sources: [6,7]

Design Challenges -- Downlink



- ❑ Modulation degrades power transfer
- ❑ Large decap is required
- ❑ Proposed Technique: Channel Reuse

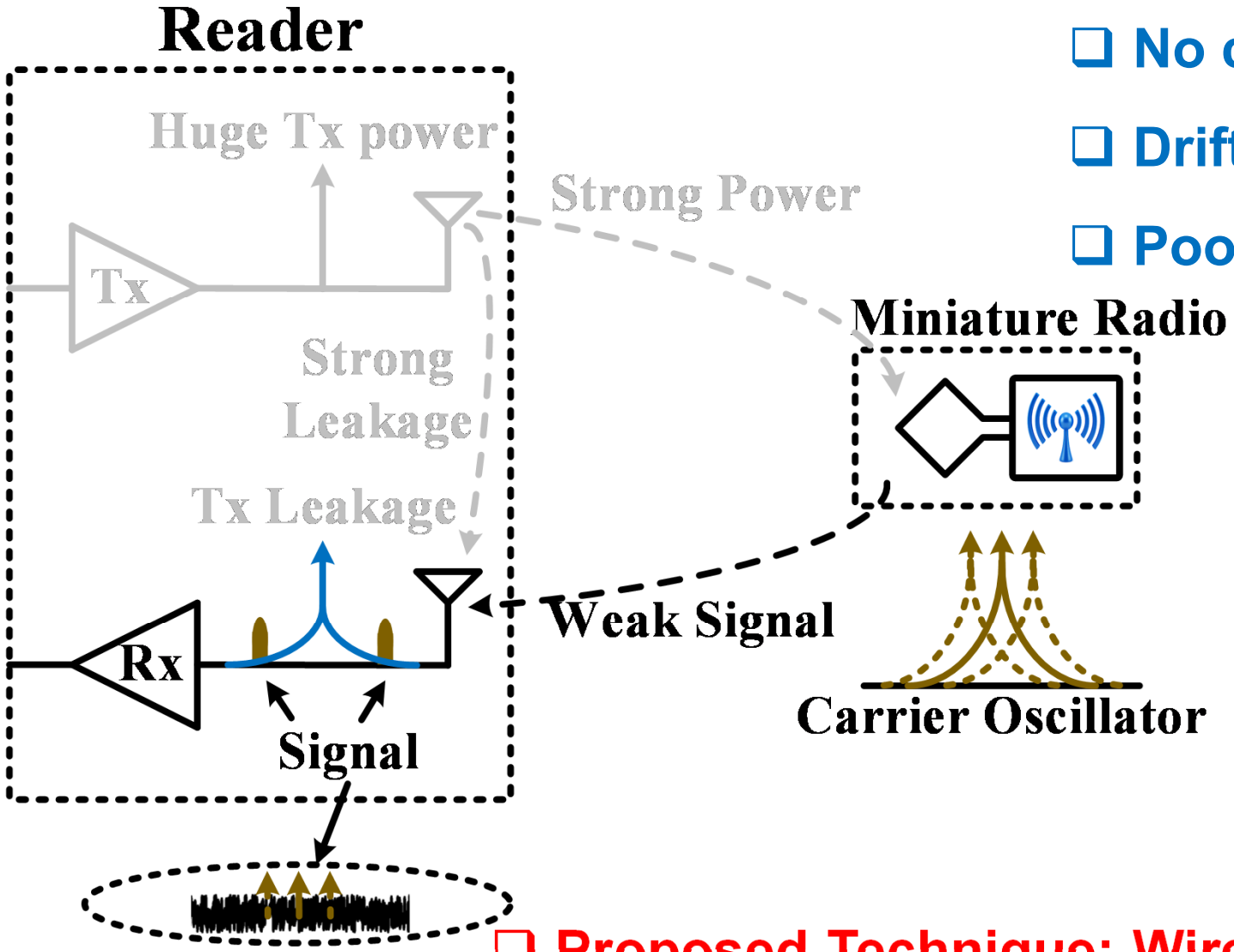
Design Challenges -- Uplink (1/2)



- Weak signal-to-blocker ratio (SBR)
- Poor signal-to-noise ratio (SNR)

- Proposed Technique: IM3 Isolation

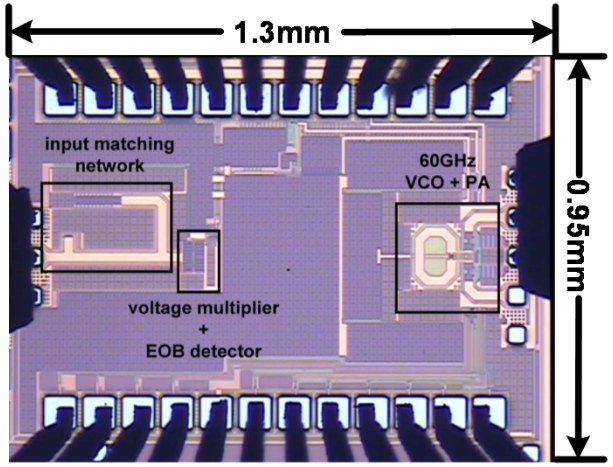
Design Challenges -- Uplink (2/2)



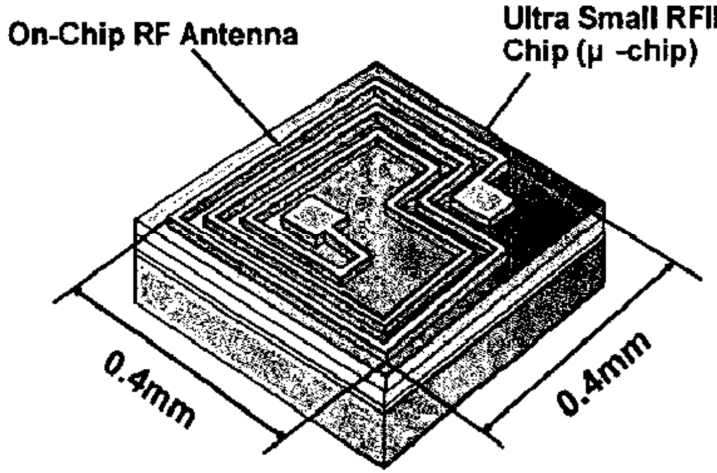
- ❑ No crystal
- ❑ Drifting noisy on-die oscillator
- ❑ Poor signal-to-noise ratio (SNR)

❑ Proposed Technique: Wireless IM2-Injection-Lock (IM2-IL)

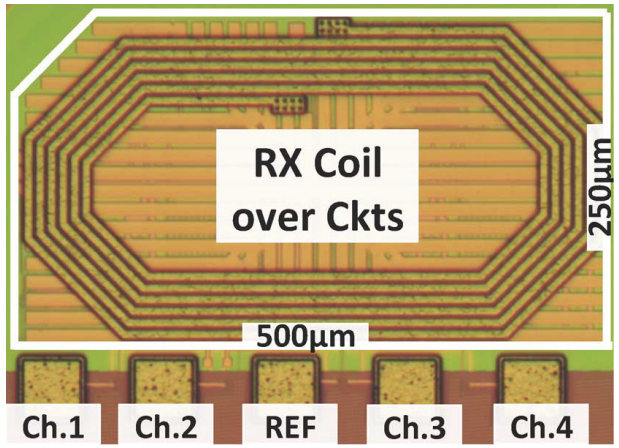
State of the Arts



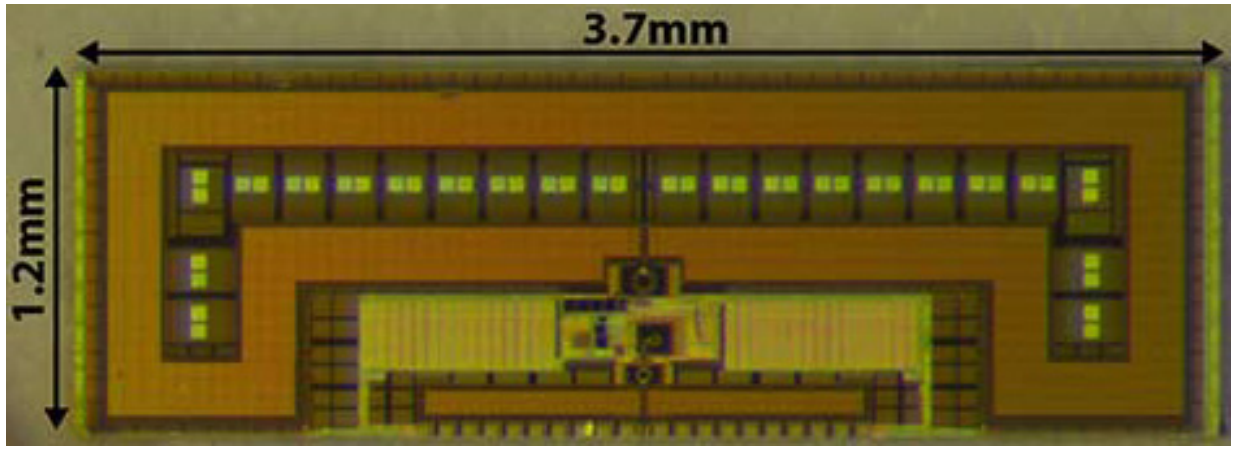
[Pellerano,JSSC,2010]



[Usami,RFIC,2004]



[Biederman,JSSC,2013]



[Tabesh,JSSC,2015]

Targeting Radio Size

Picture Source: [13]

~100um x ~100um Dielet

Outline

- ❑ Design Motivation
- ❑ **Proposed Radio System**
- ❑ Circuit Details
- ❑ Measurement Results
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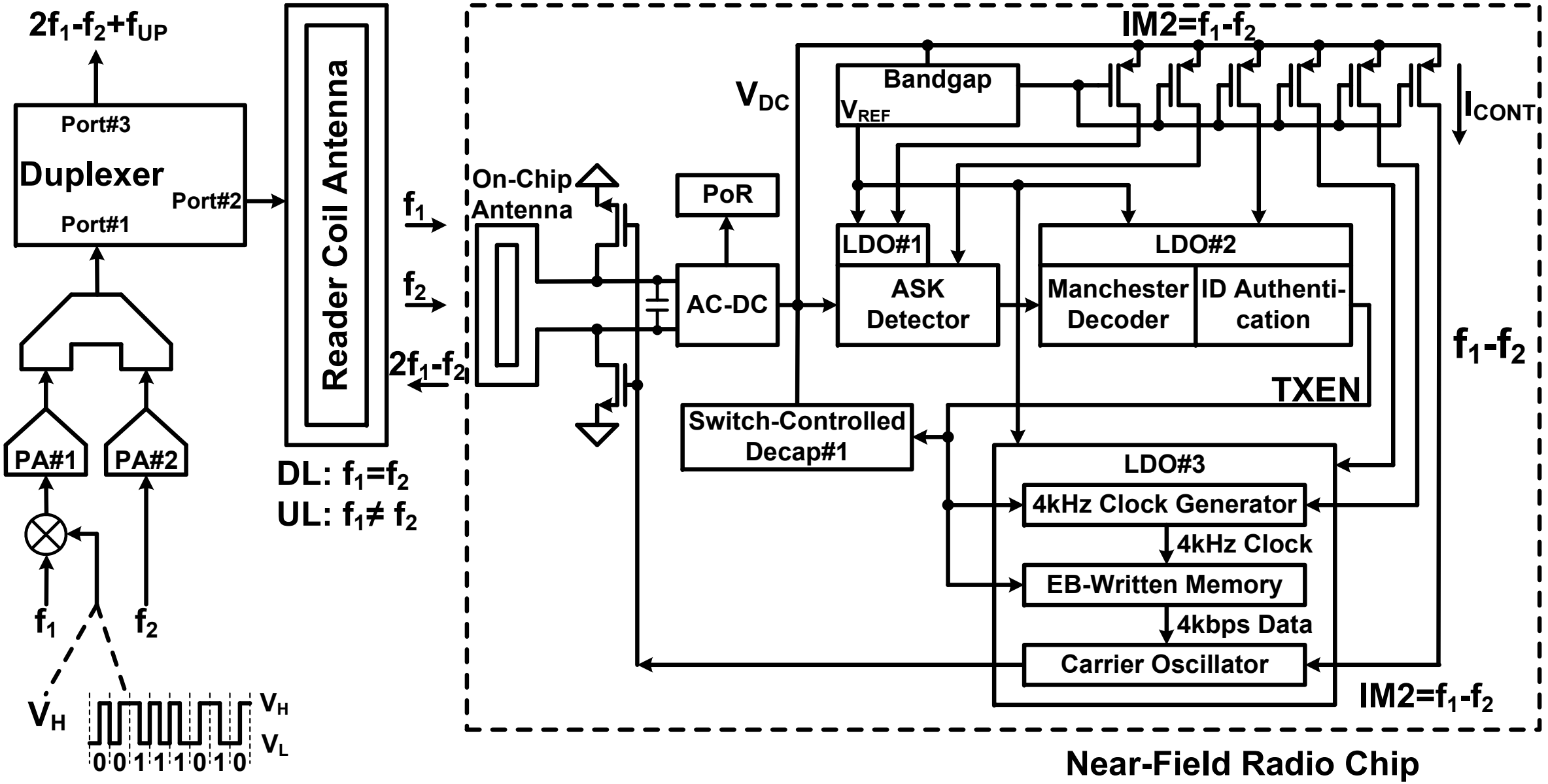
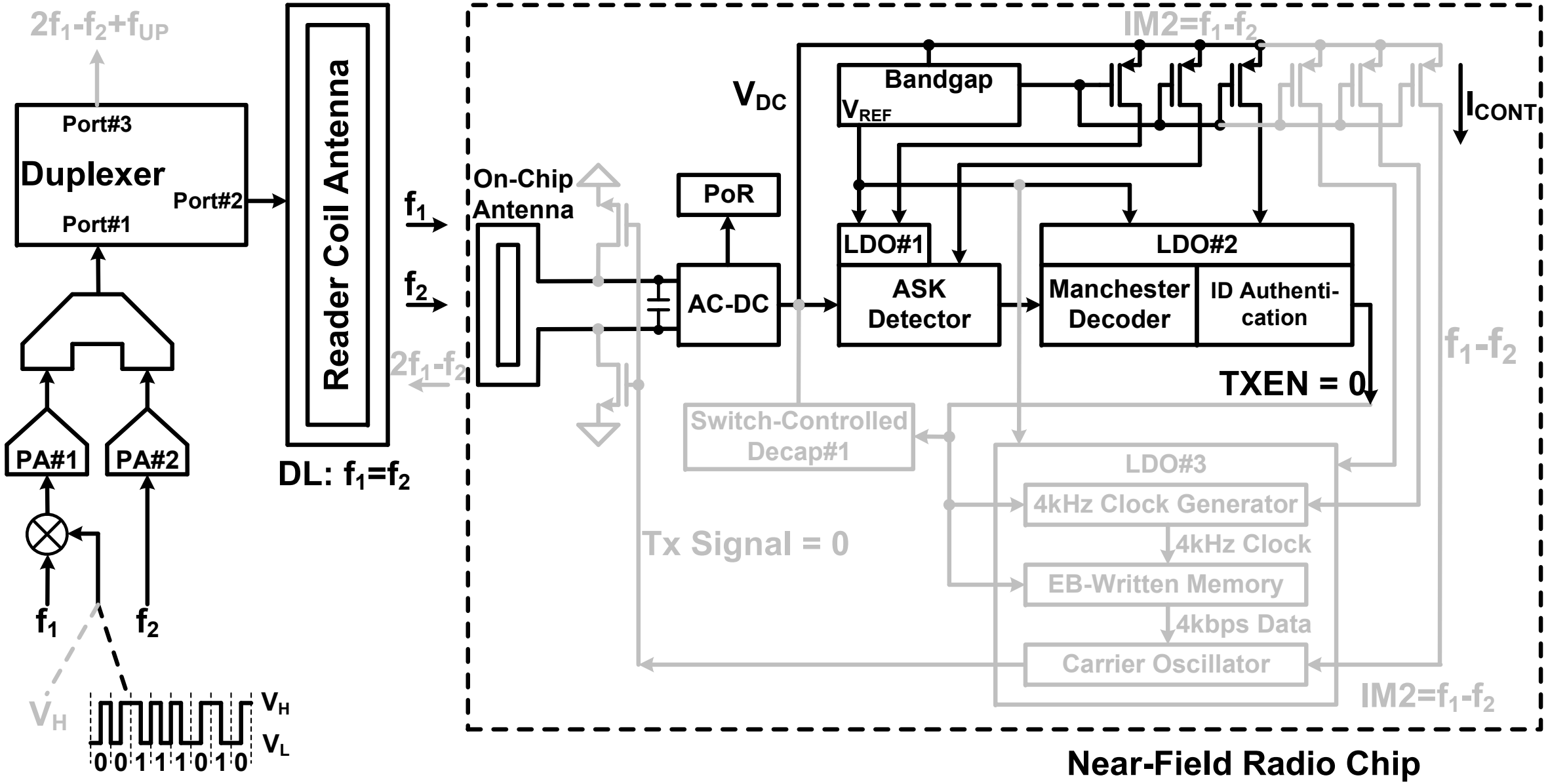
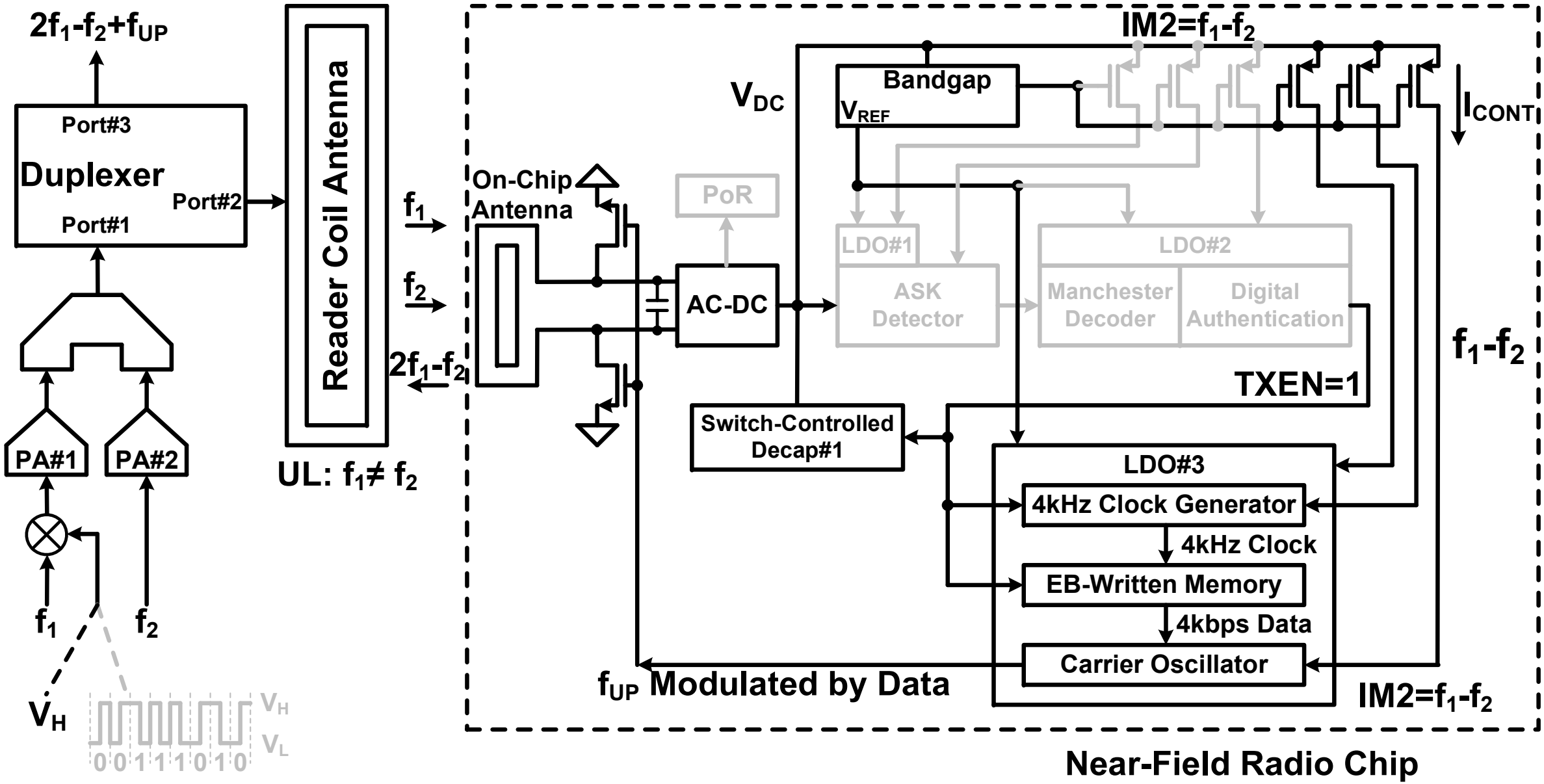
System Architecture



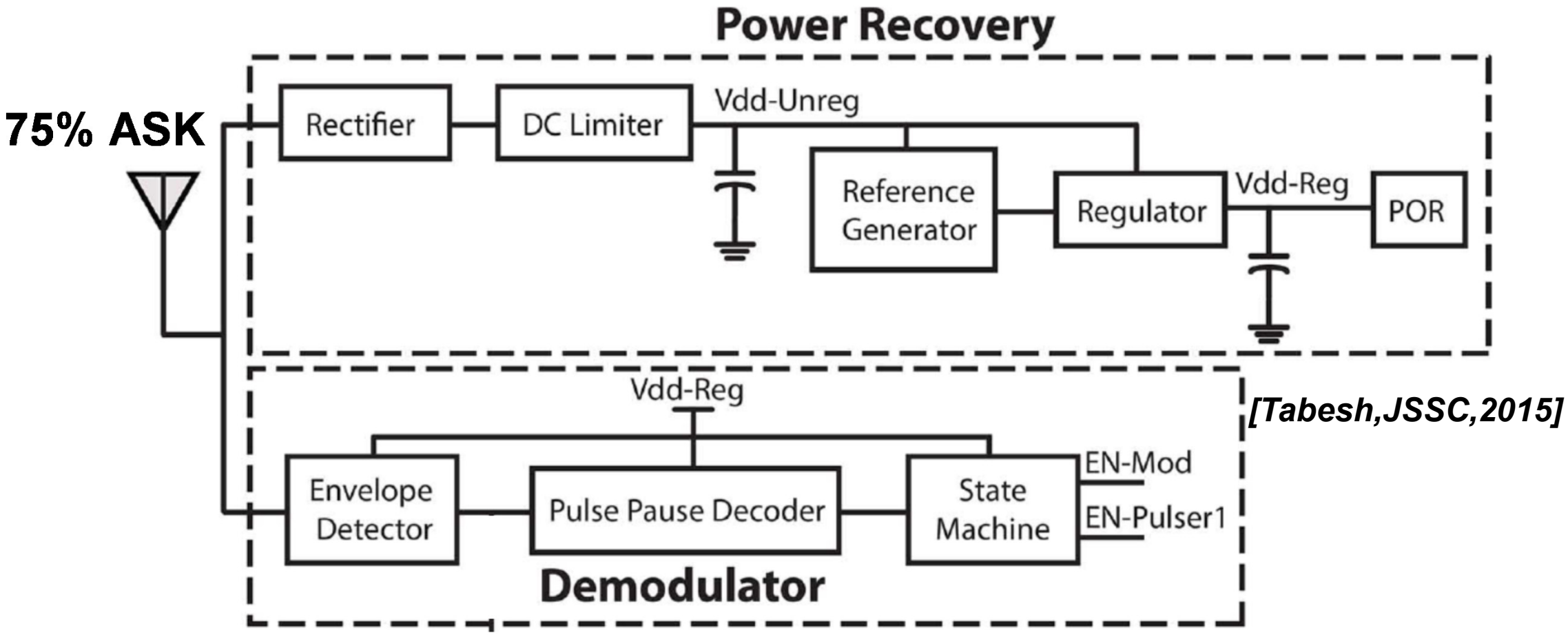
Working Flow -- Downlink



Working Flow -- Uplink



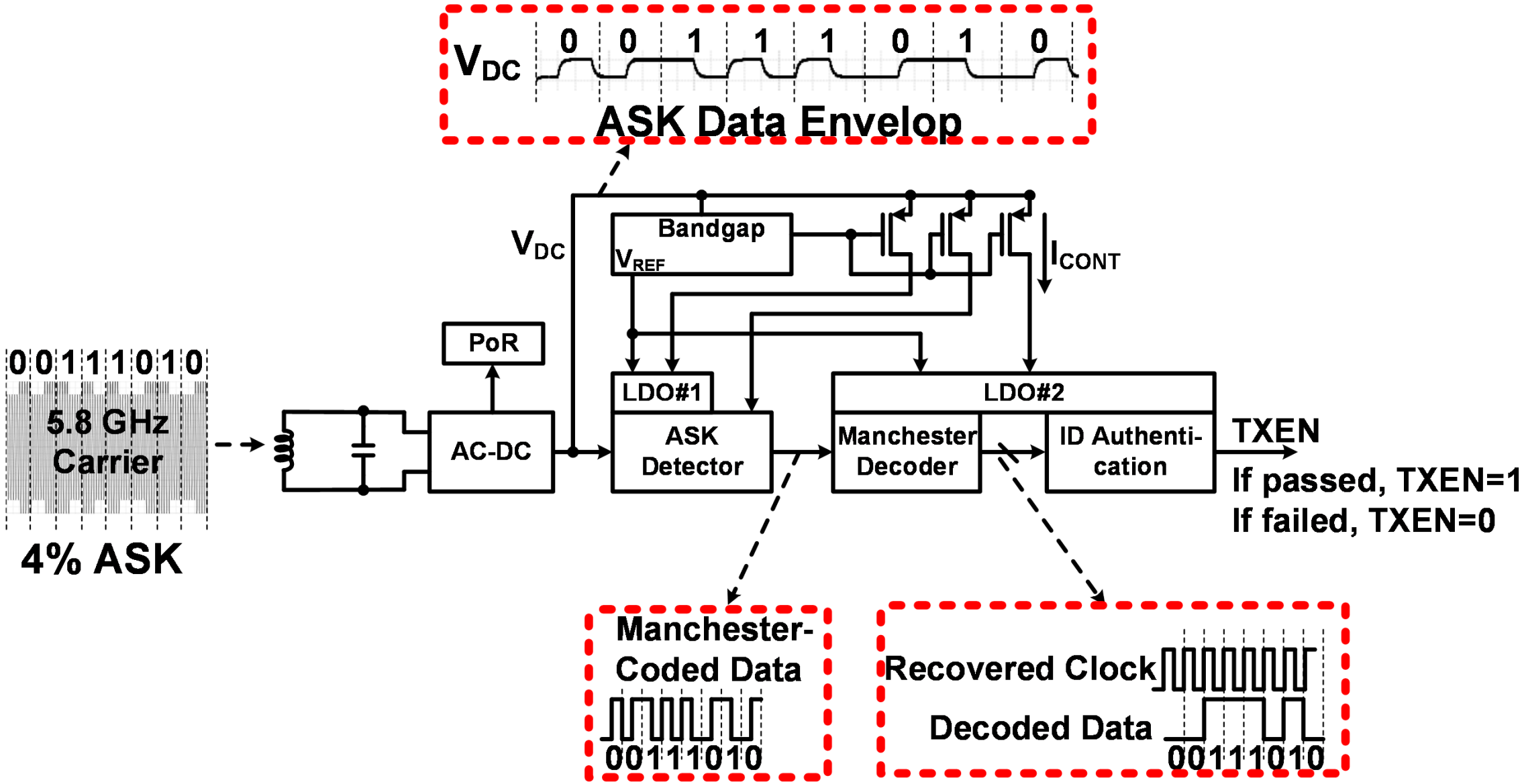
Conventional RFID Downlink



[Tabesh,JSSC,2015]

- Large decap
- For loosely coupling: Low data rate & Low power efficiency

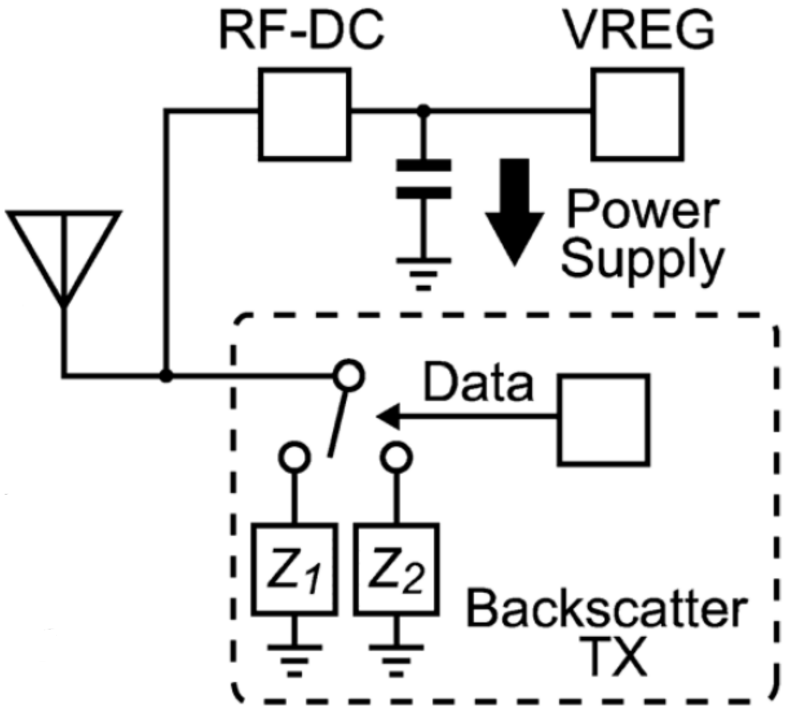
Channel Reuse Technique



Conventional Uplinks

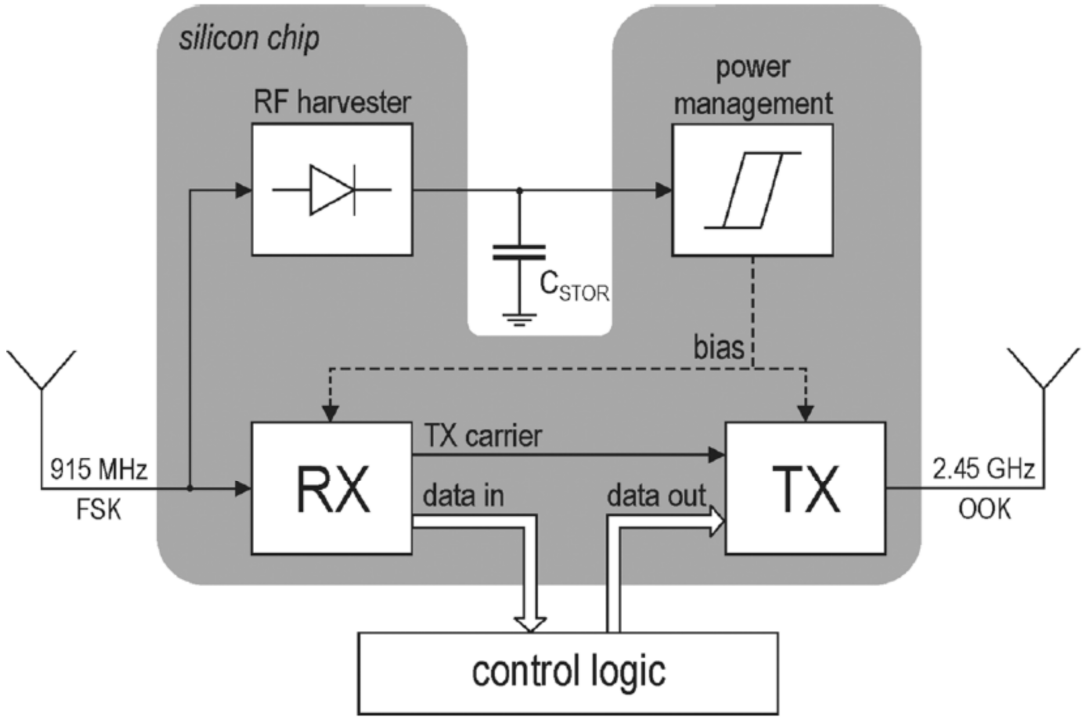
Backscattering

[Shirane,JSSC,2015]



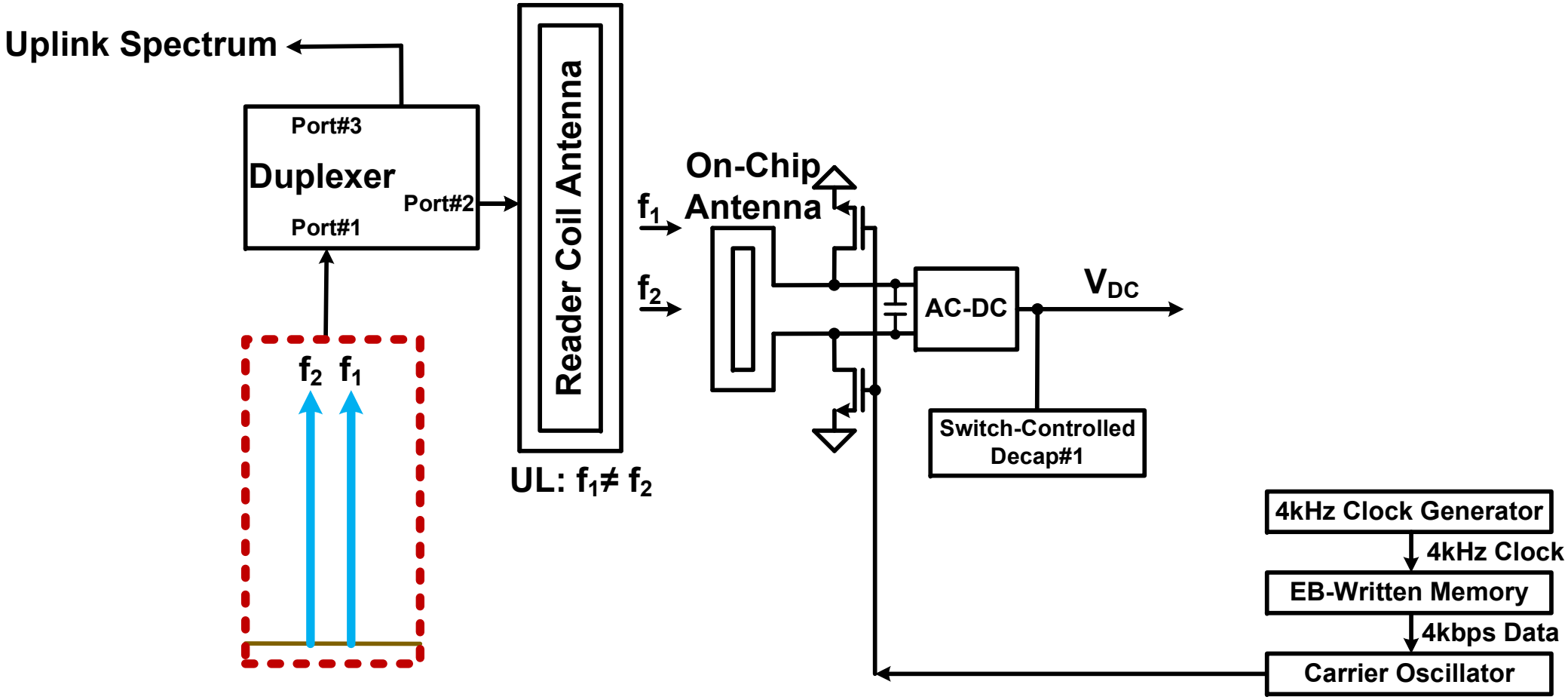
Dual Antennas

[Dagan,JSSC,2014]

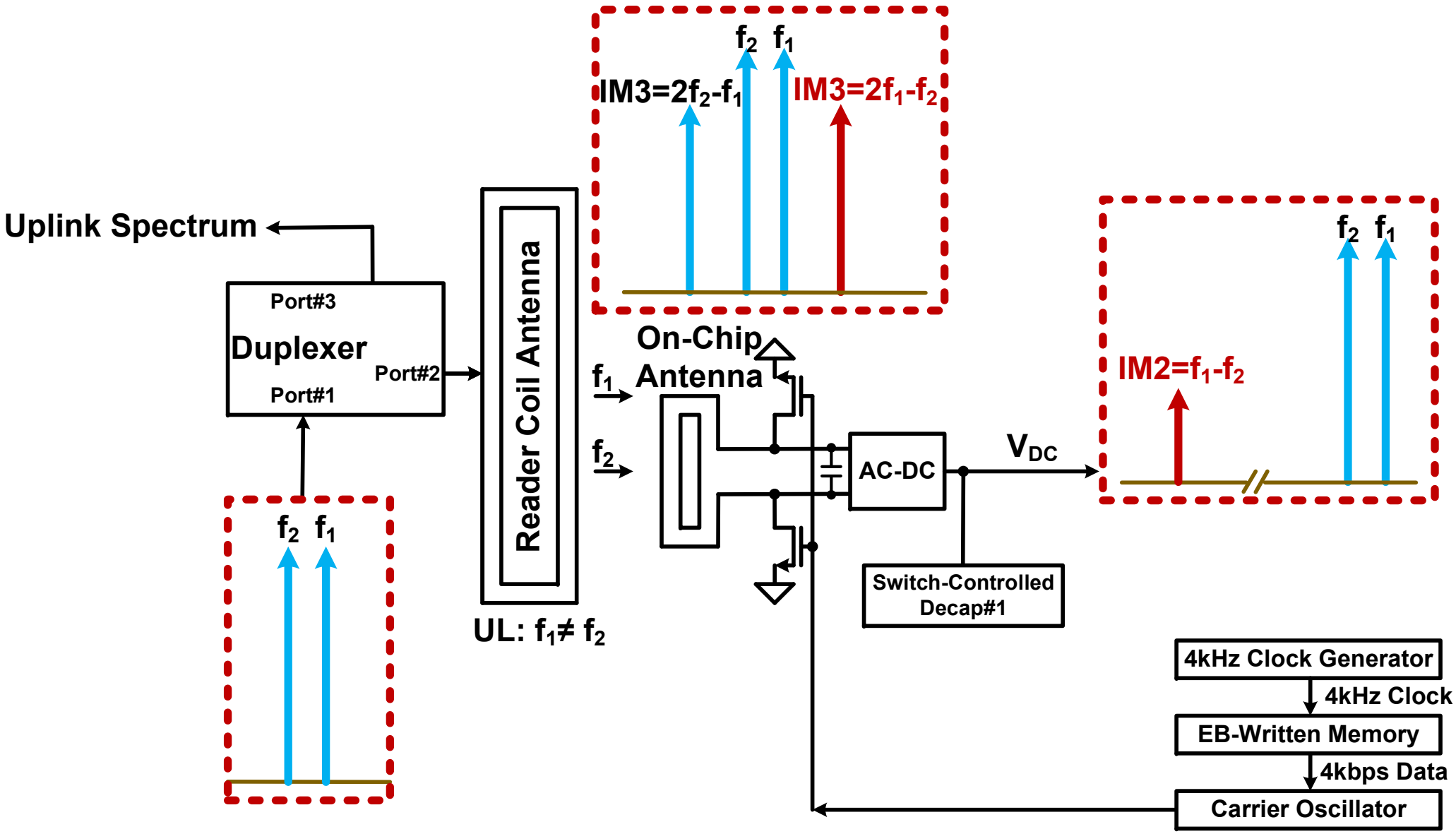


- Backscattering results in poor SBR and SNR
- Dual antennas take a large die area

Proposed Two-Tone Technique



Proposed Two-Tone Technique



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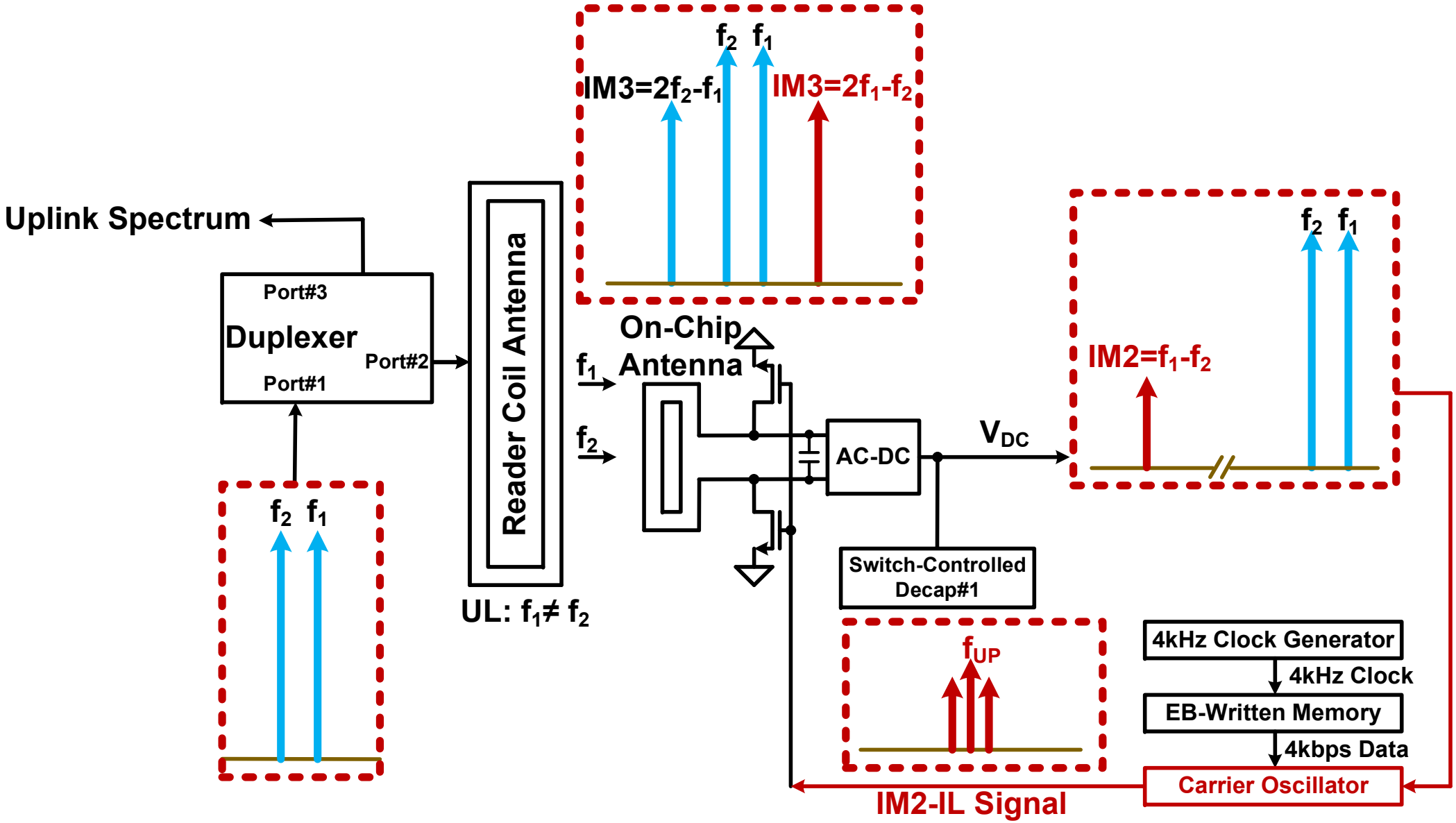

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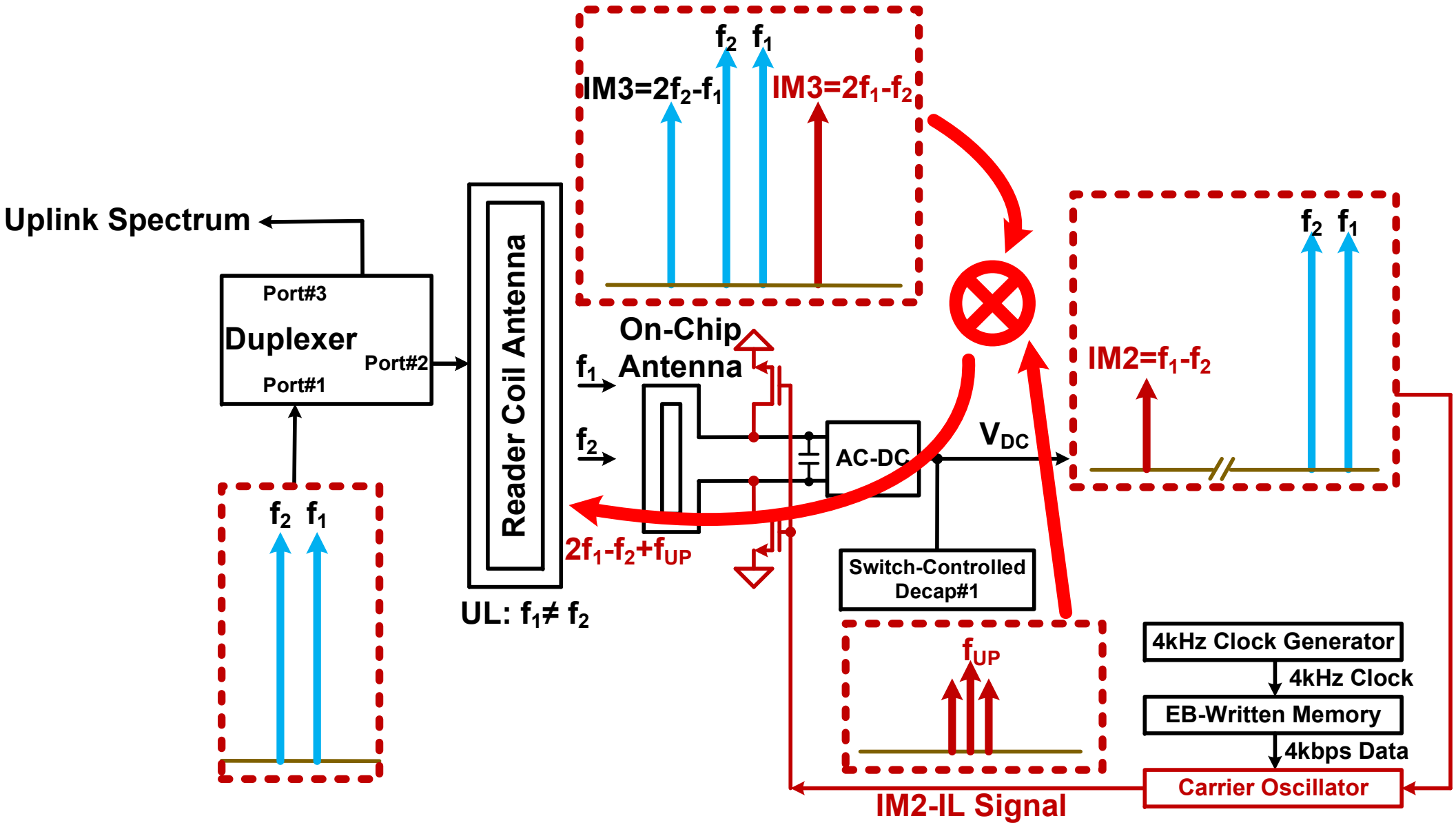

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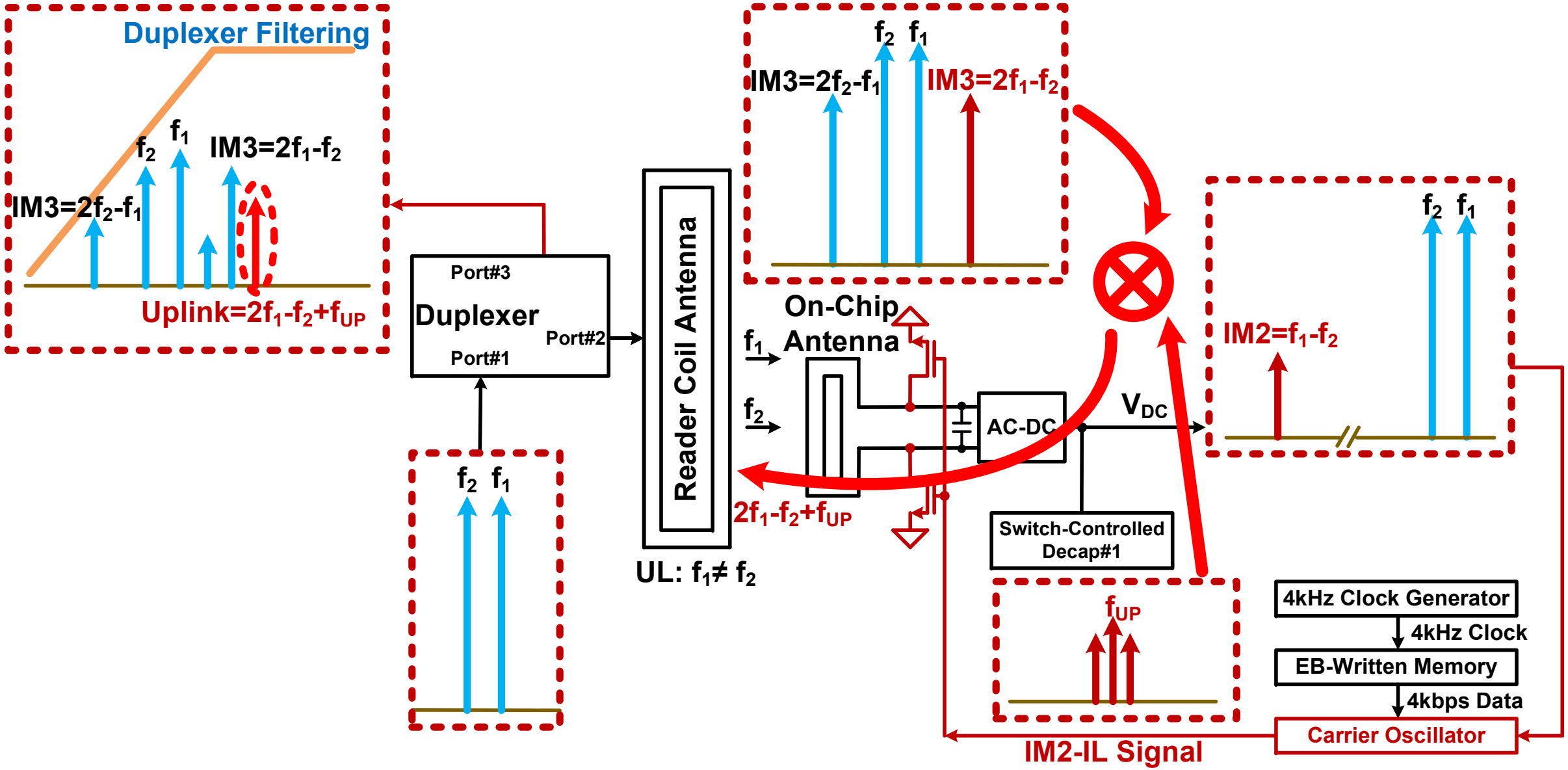

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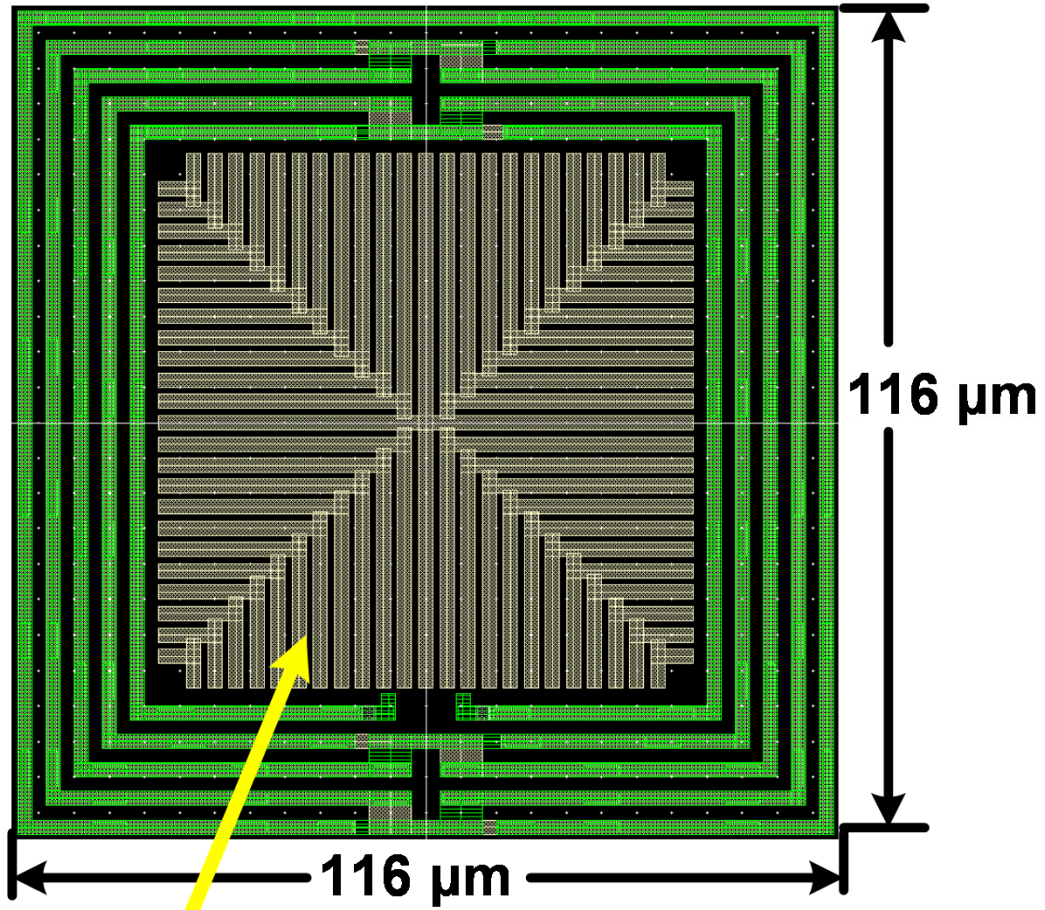
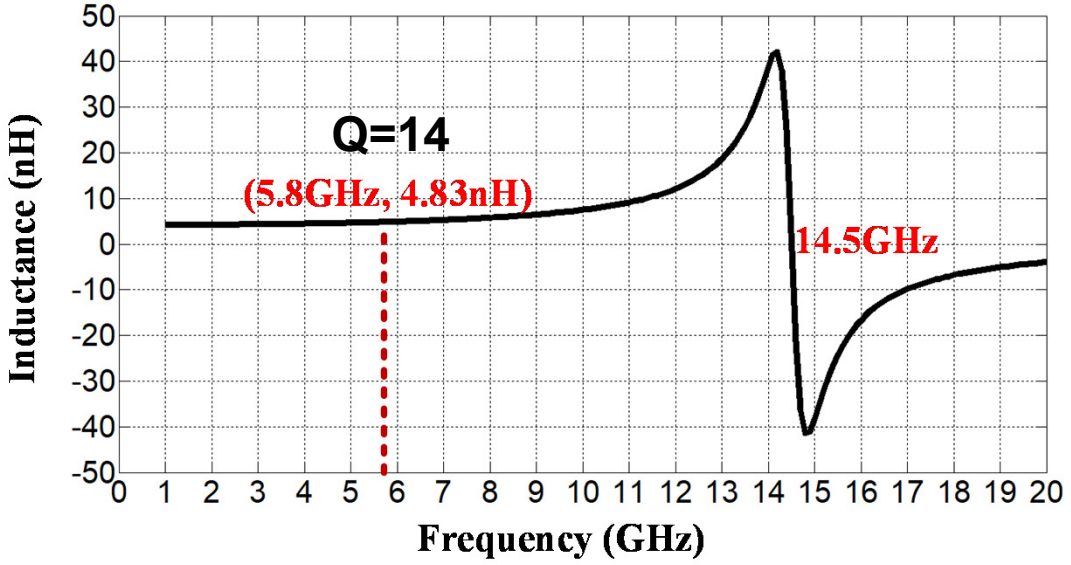
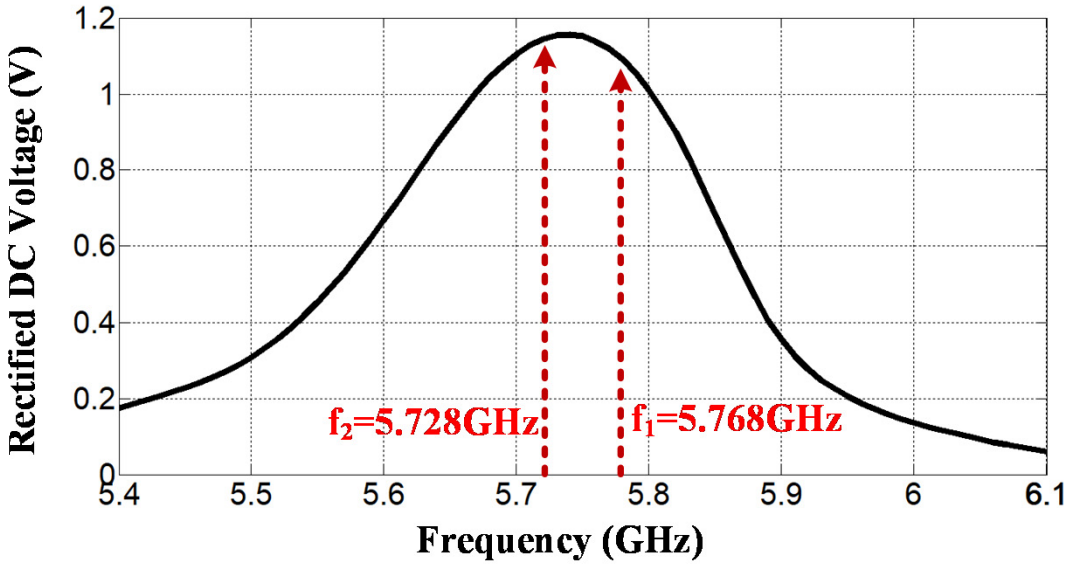
On-Chip Antenna

On-Chip Coil Antenna

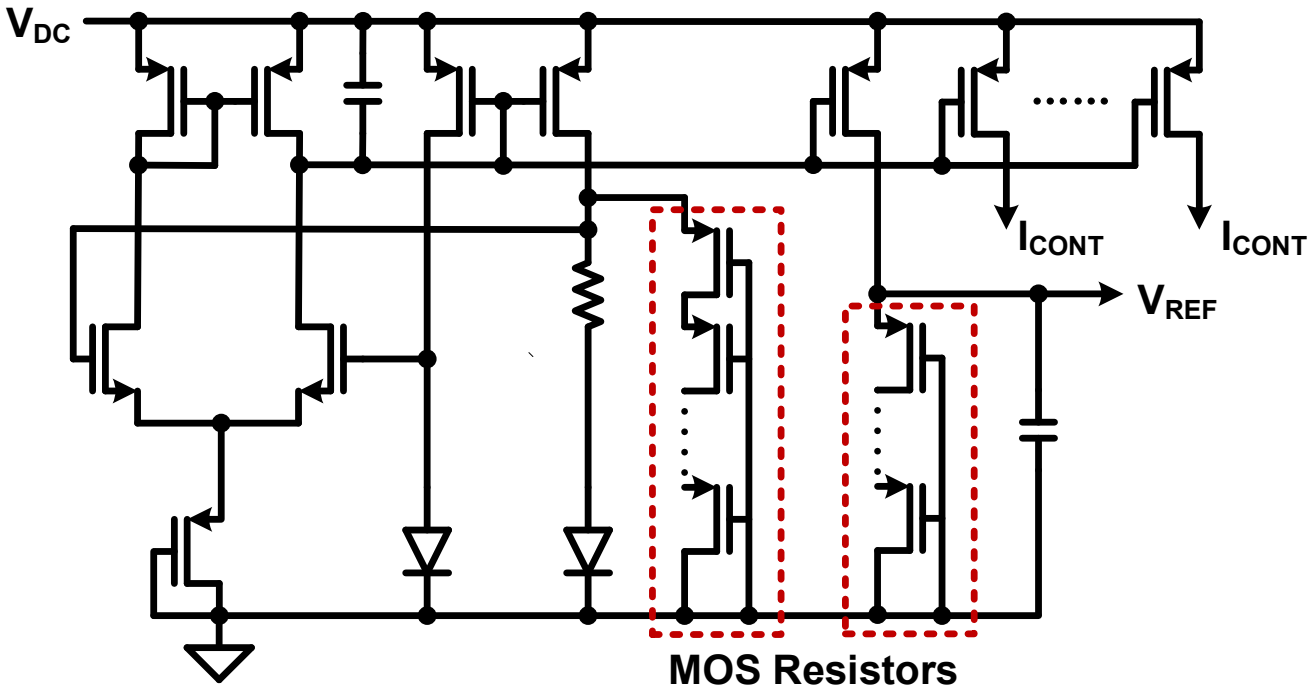


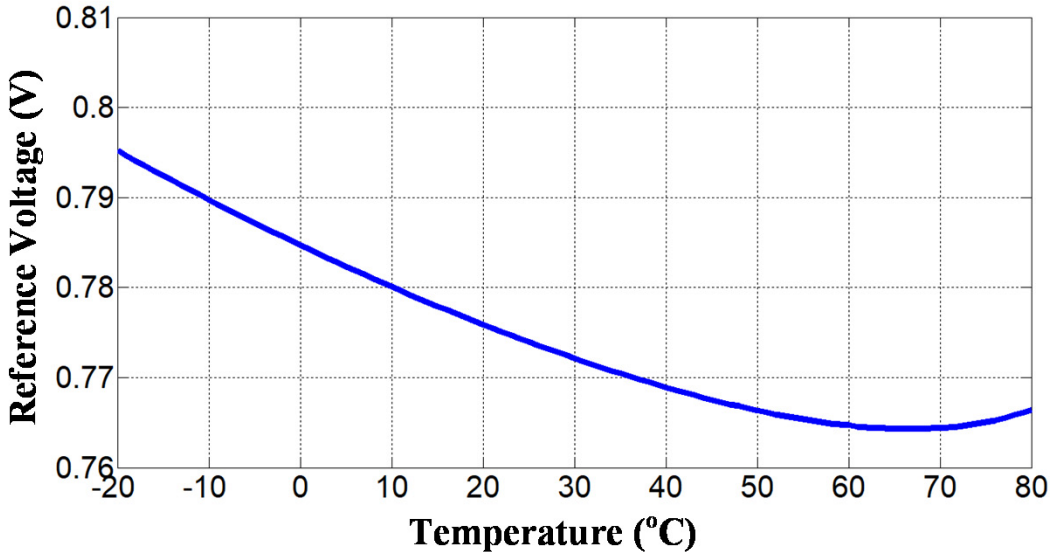
Ground Tree

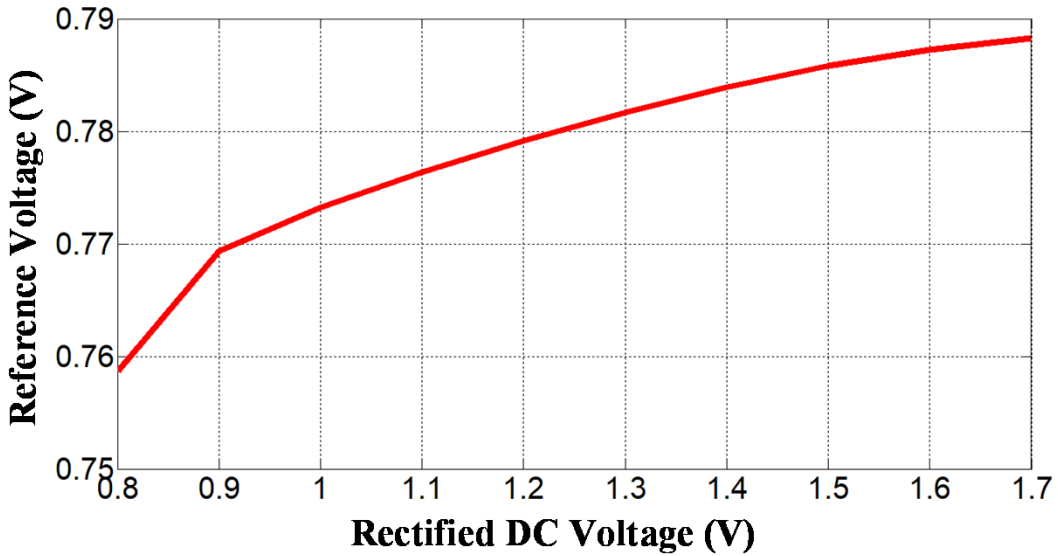




Miniature Bandgap

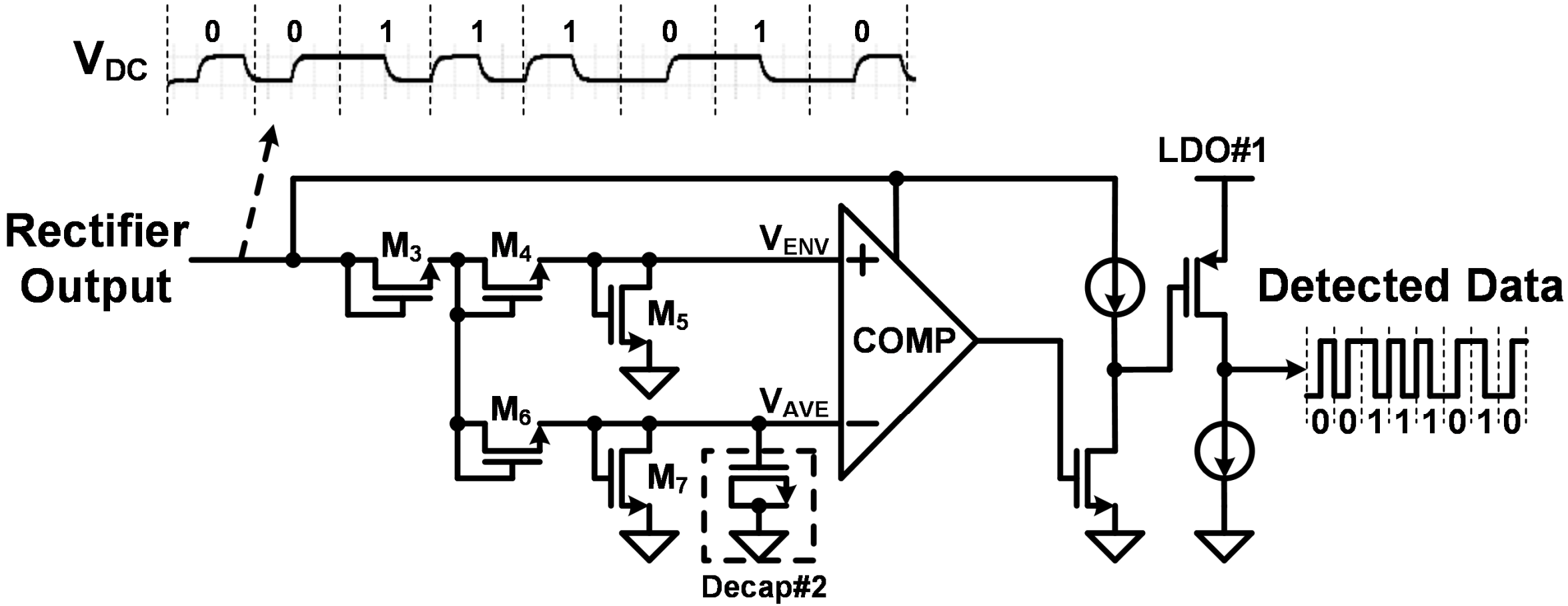




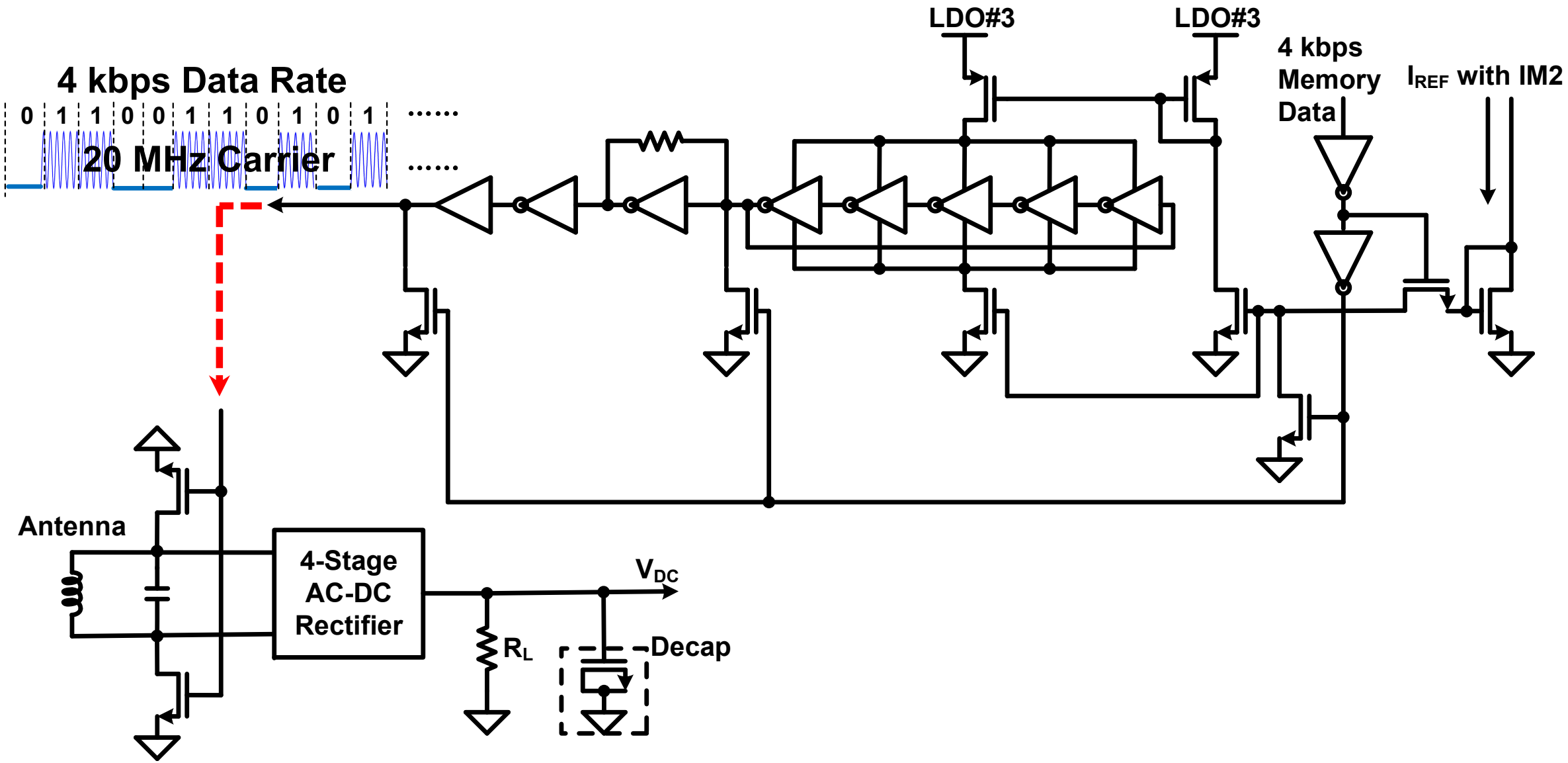


- ❑ <0.03V variation vs. temperature
- ❑ <0.03V variation vs. V_{DC}
- ❑ Robust over PVT

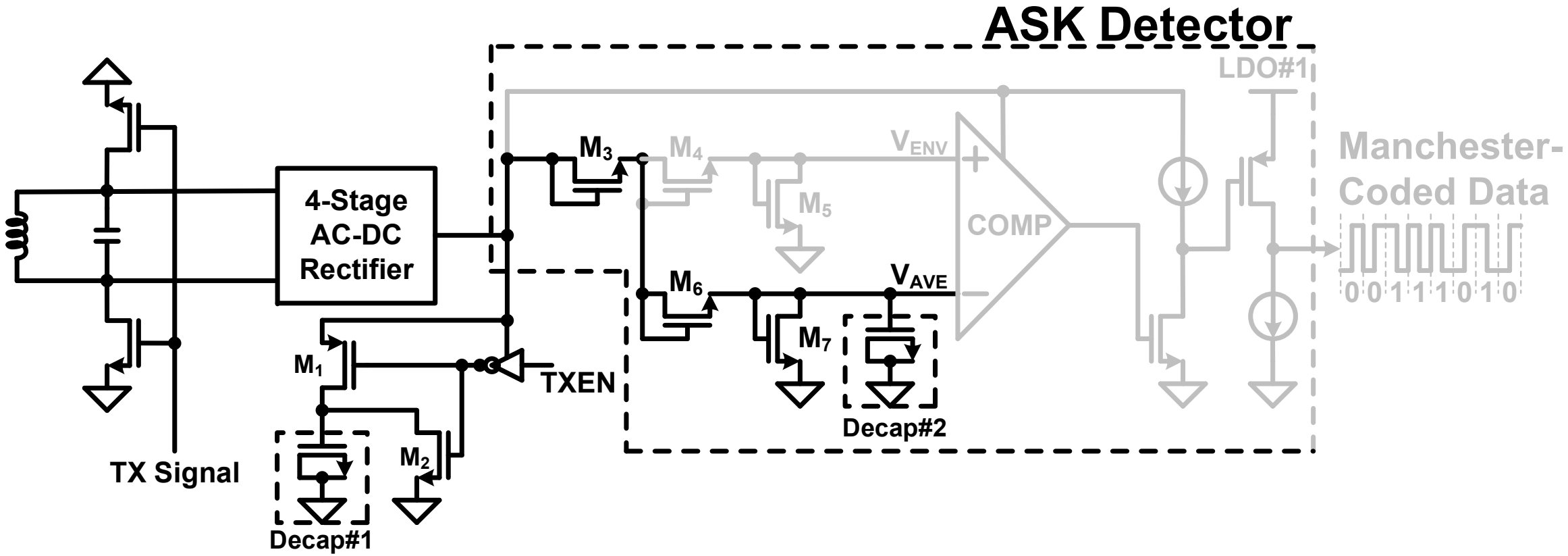
ASK Detector



Carrier Oscillator



Decap Optimization



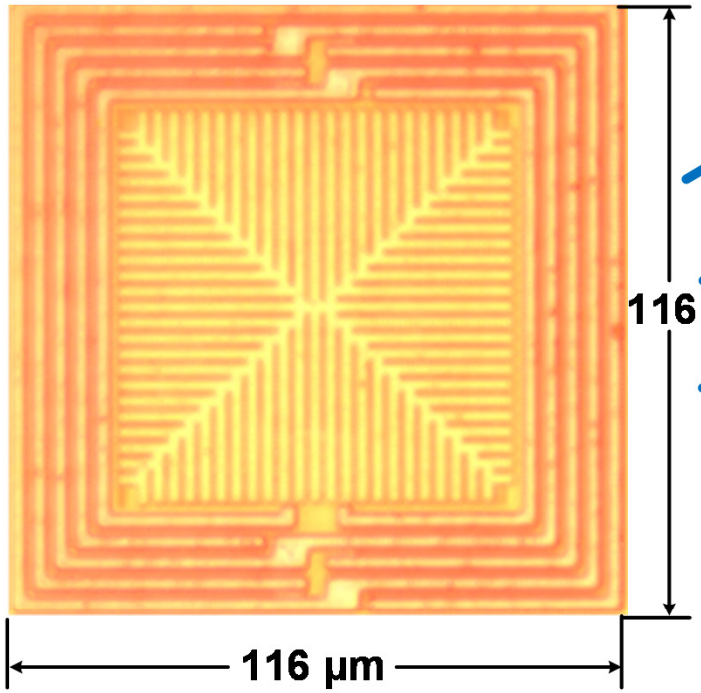
- Downlink: TXEN=0, Decap#1 Off
- Uplink: TXEN=1, Decap#1 On

Outline

- ❑ Design Motivation
- ❑ Proposed Radio System
- ❑ Circuit Details
- ❑ **Measurement Results**
- ❑ Summary
- ❑ Acknowledgements

Radio Chip

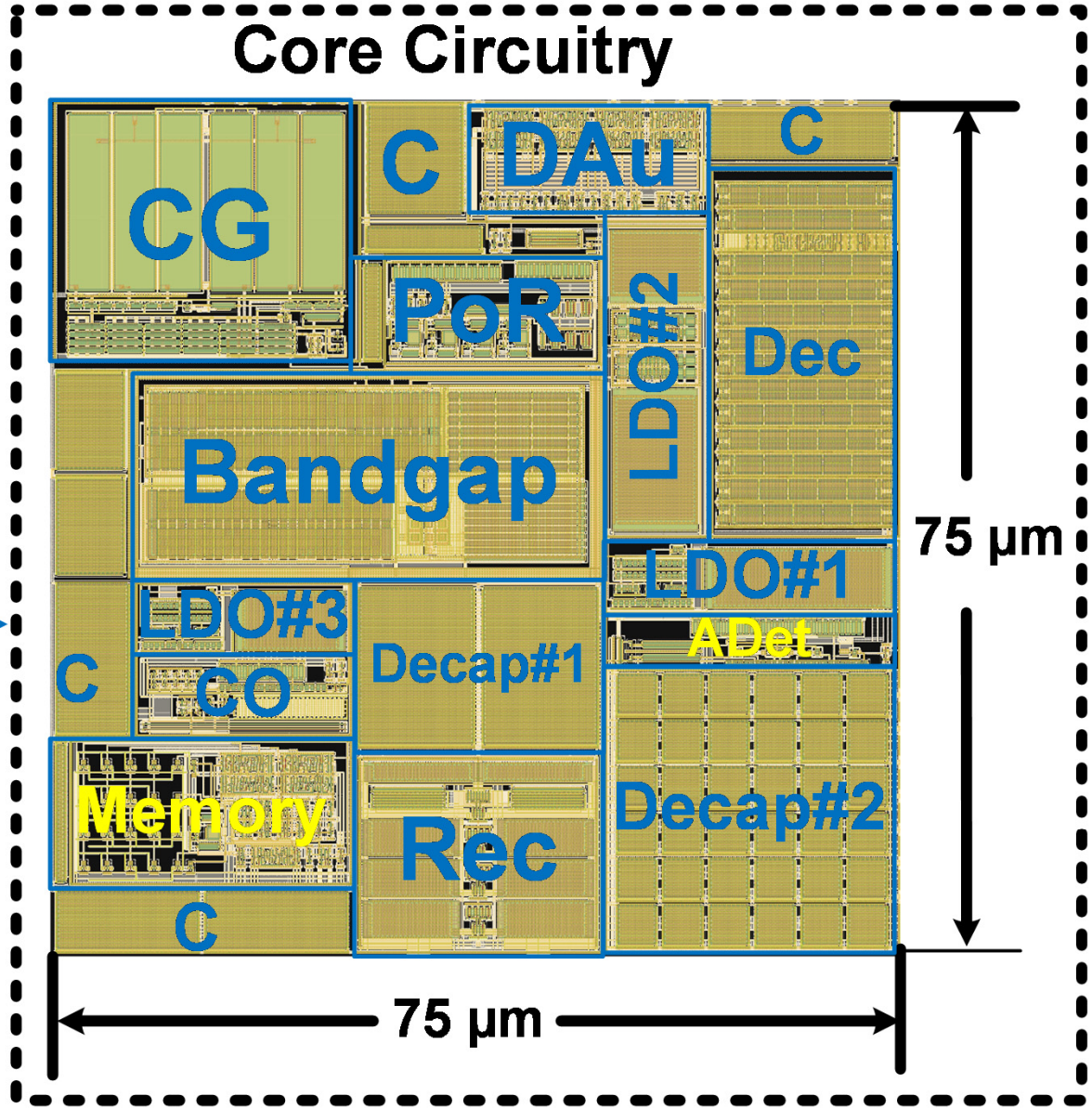
65nm CMOS (w/ UTM)



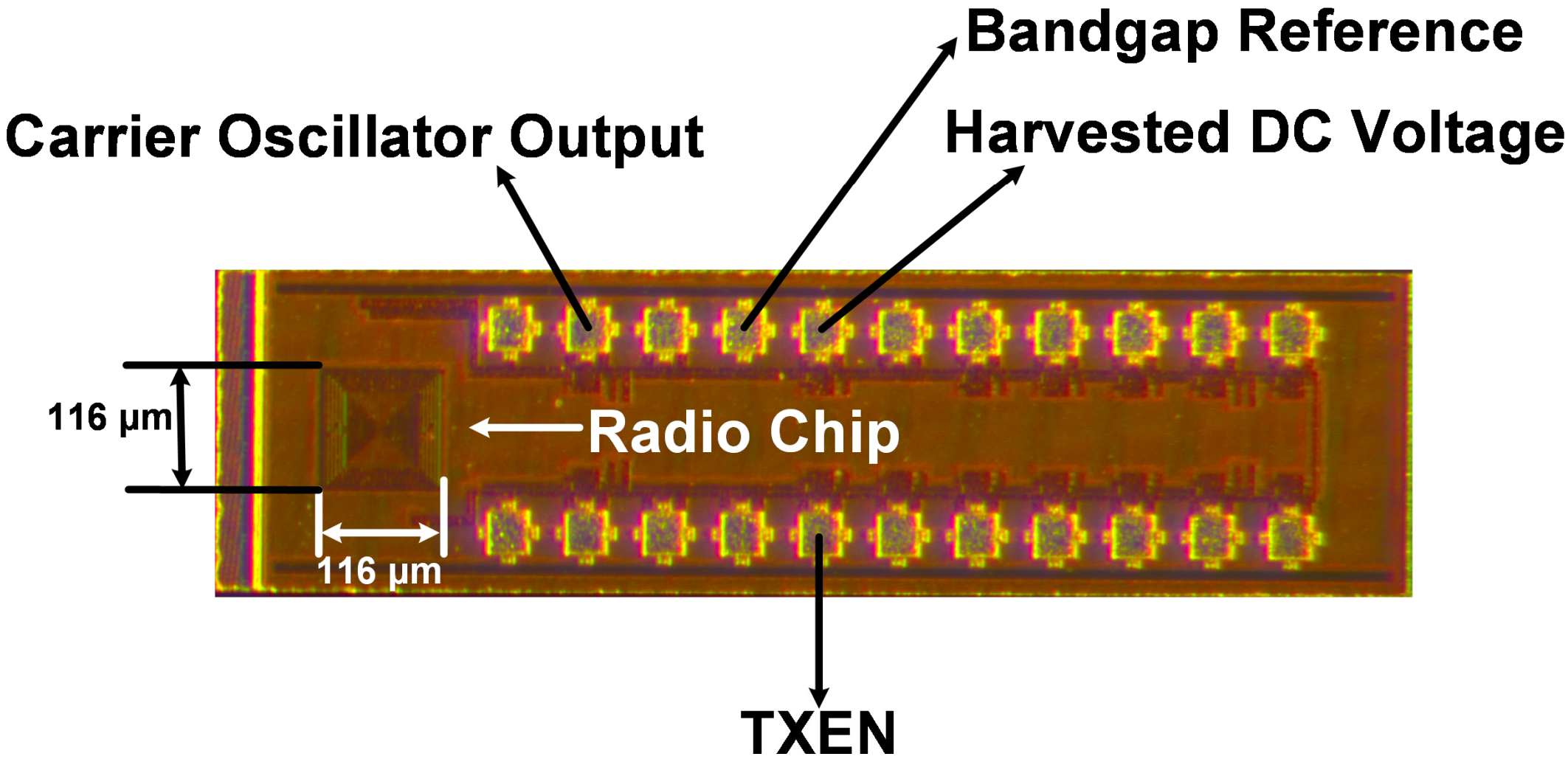
Coil Antenna

Ground Tree

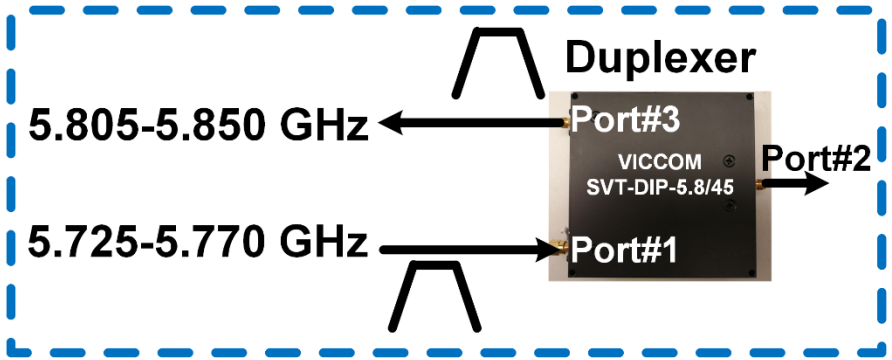
CG: Clock Generator
Rec: AC-DC Rectifier
ADet: ASK Detector
CO: Carrier Oscillator
Dec: Manchester Decoder
PoR: Power-on Reset
DAu: Digital Authentication
C: Other Decaps

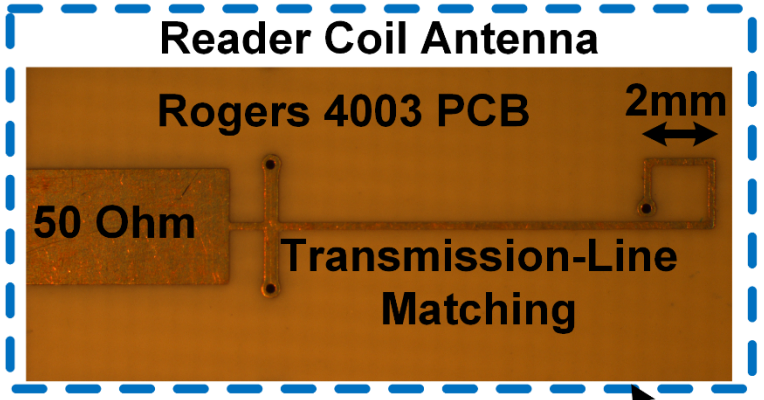


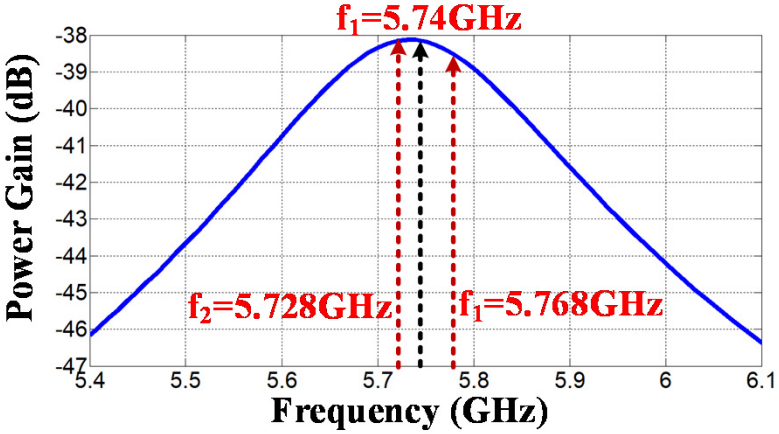
Testing Chip

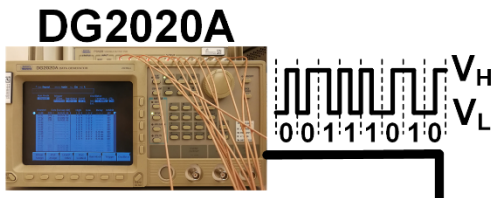


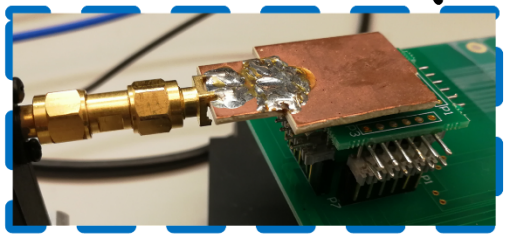
Tx-Rx System

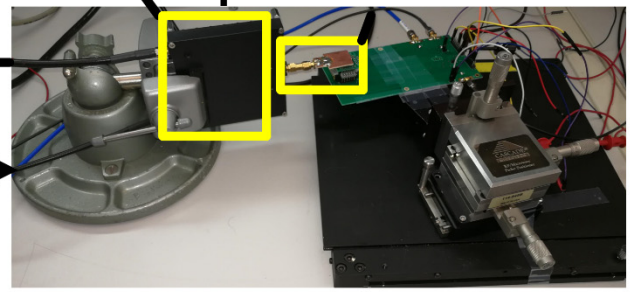








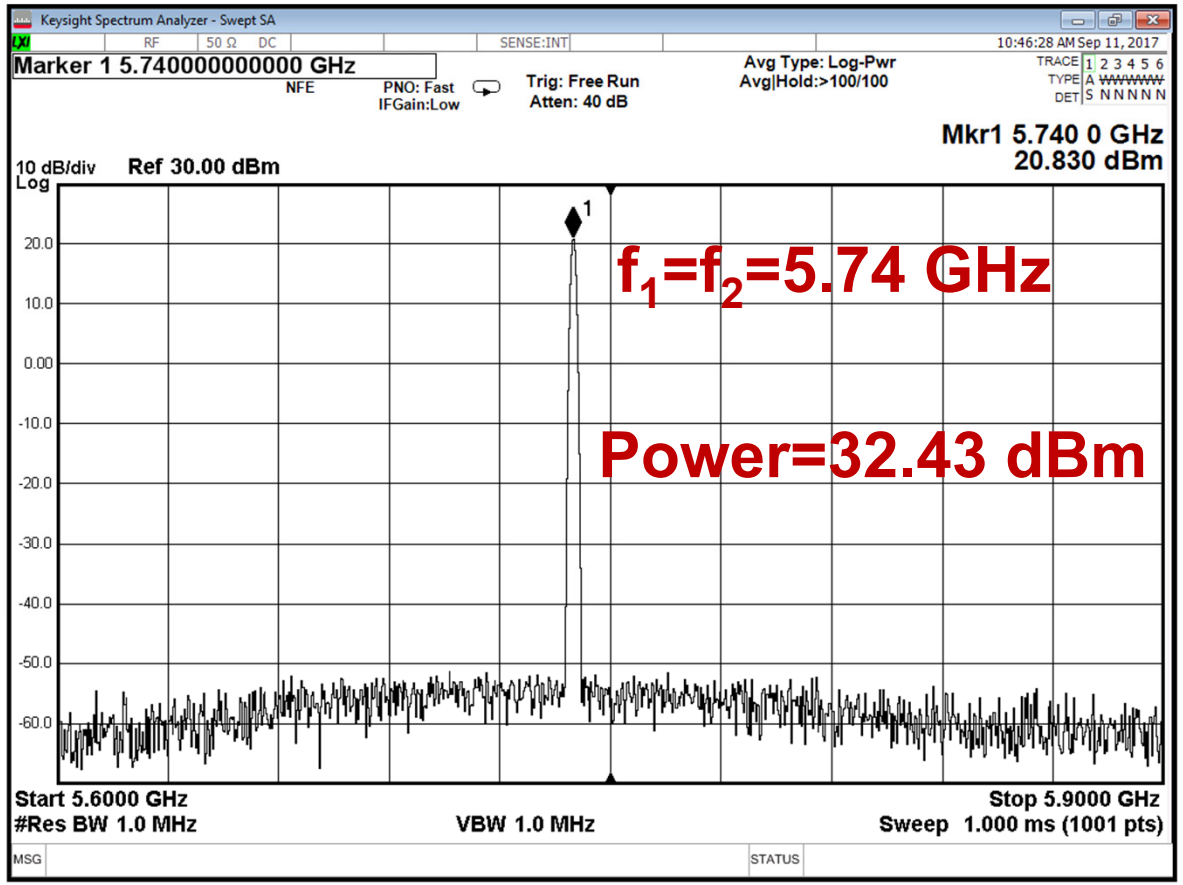




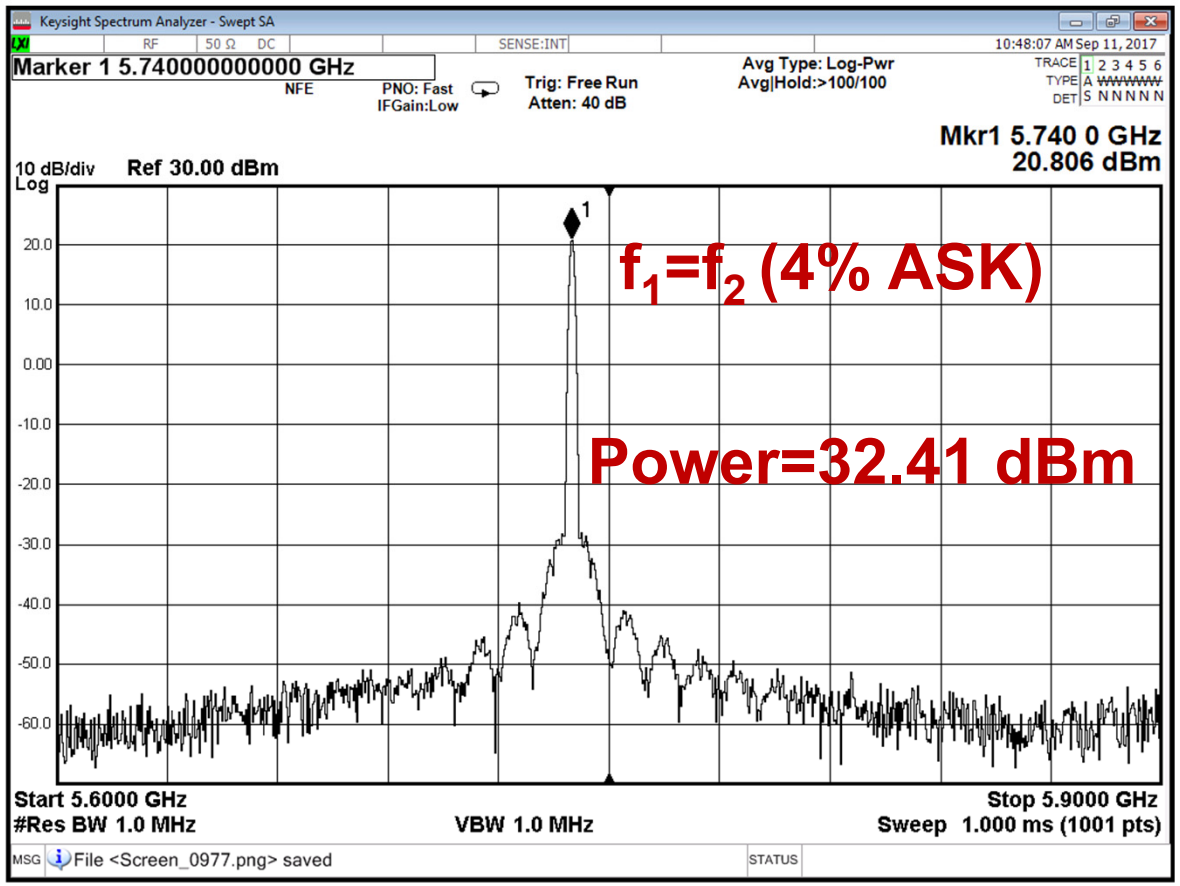
- ❑ **Downlink:**
  - ➢ $f_1=f_2=5.74$GHz (in phase)
- ❑ **Uplink:**
  - ➢ $f_1=5.768$GHz & $f_2=5.728$GHz
  - ➢ Uplink=5.828GHz
  - ➢ Blocker=5.808GHz

Downlink Reader Signals

Signal Tone W/O ASK Modulation

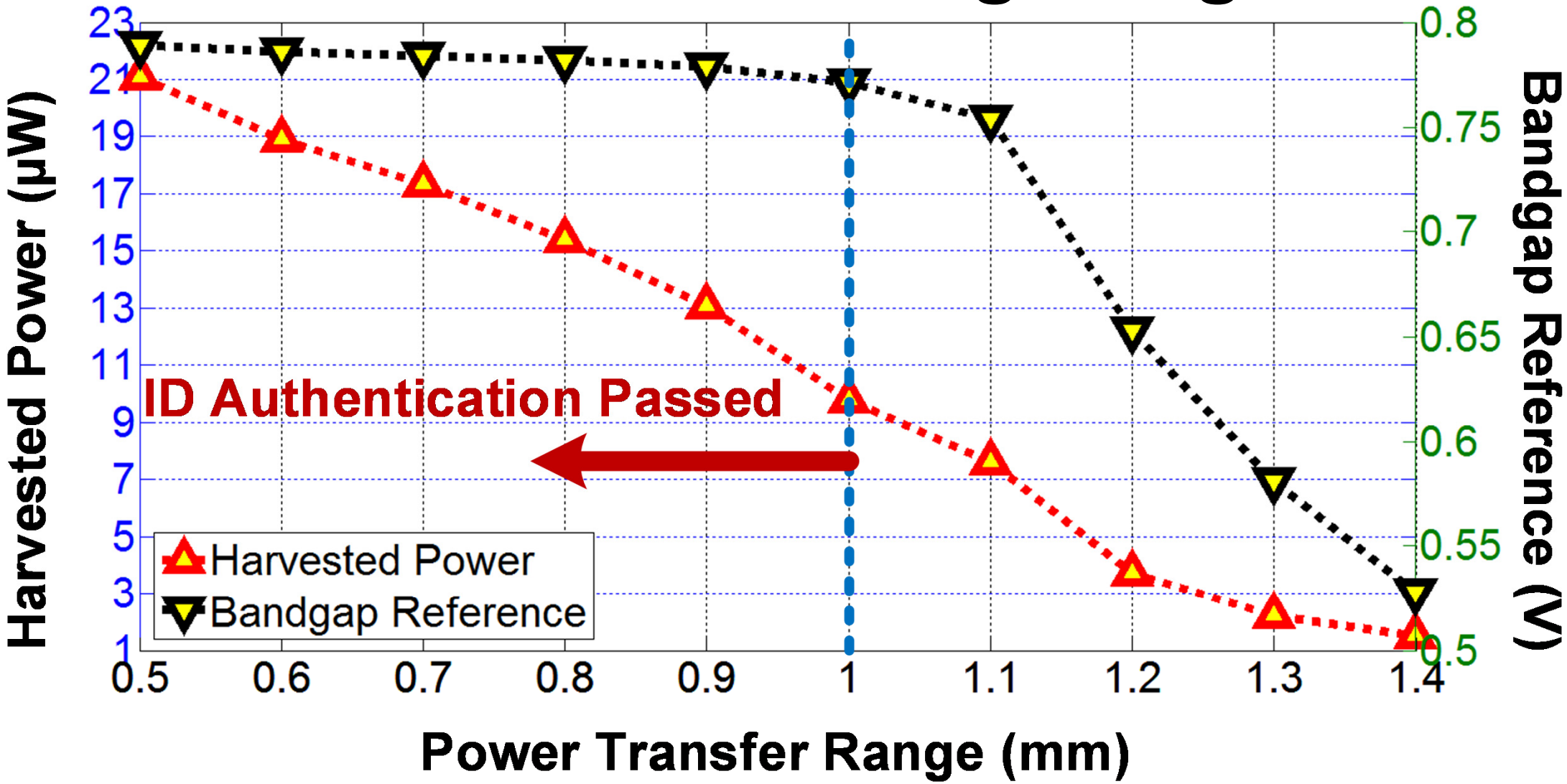


Signal Tone W/ ASK Modulation



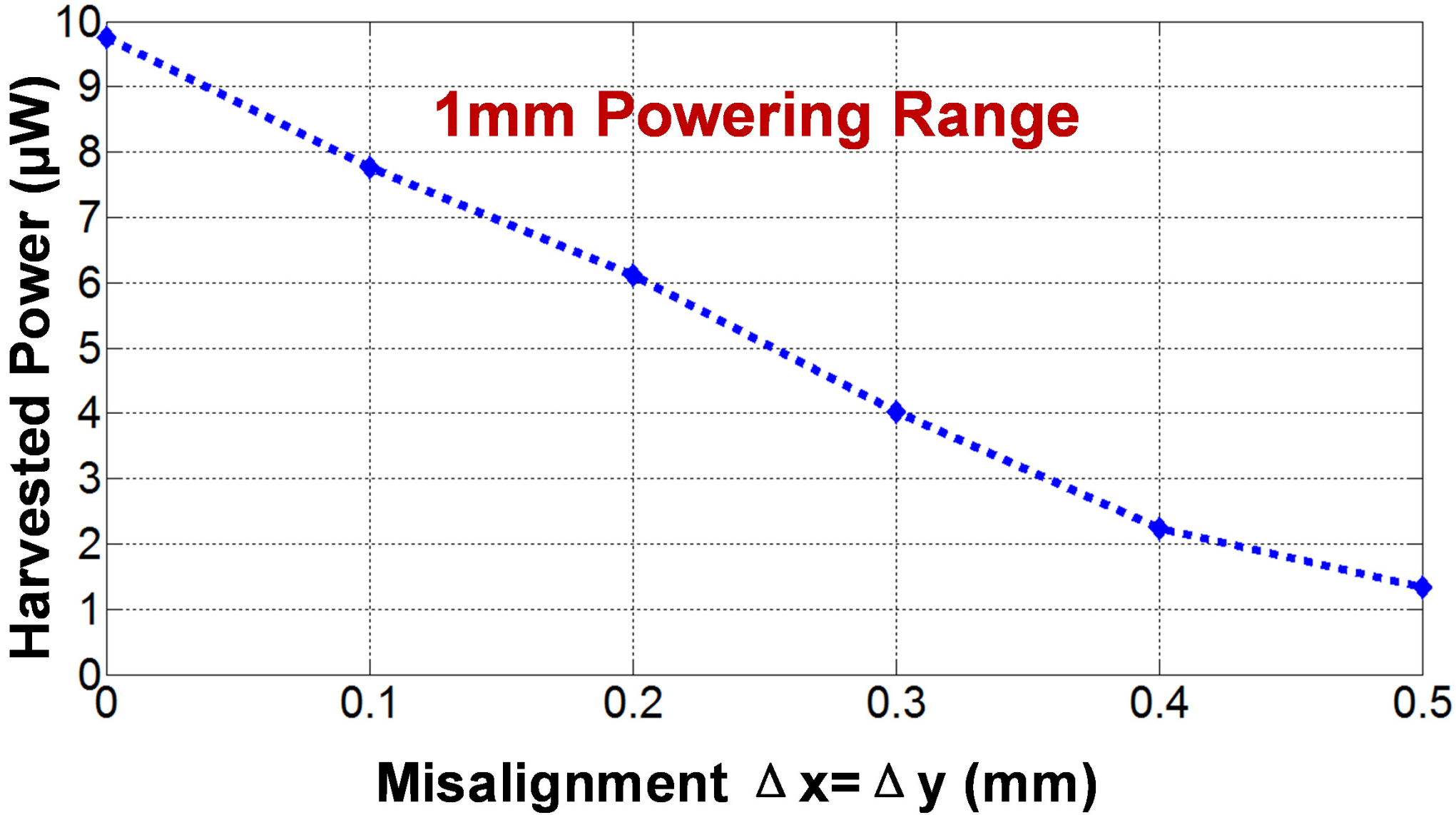
- Note: The results include 11.6 dB attenuator for the safety of N9030A

Downlink Powering Range

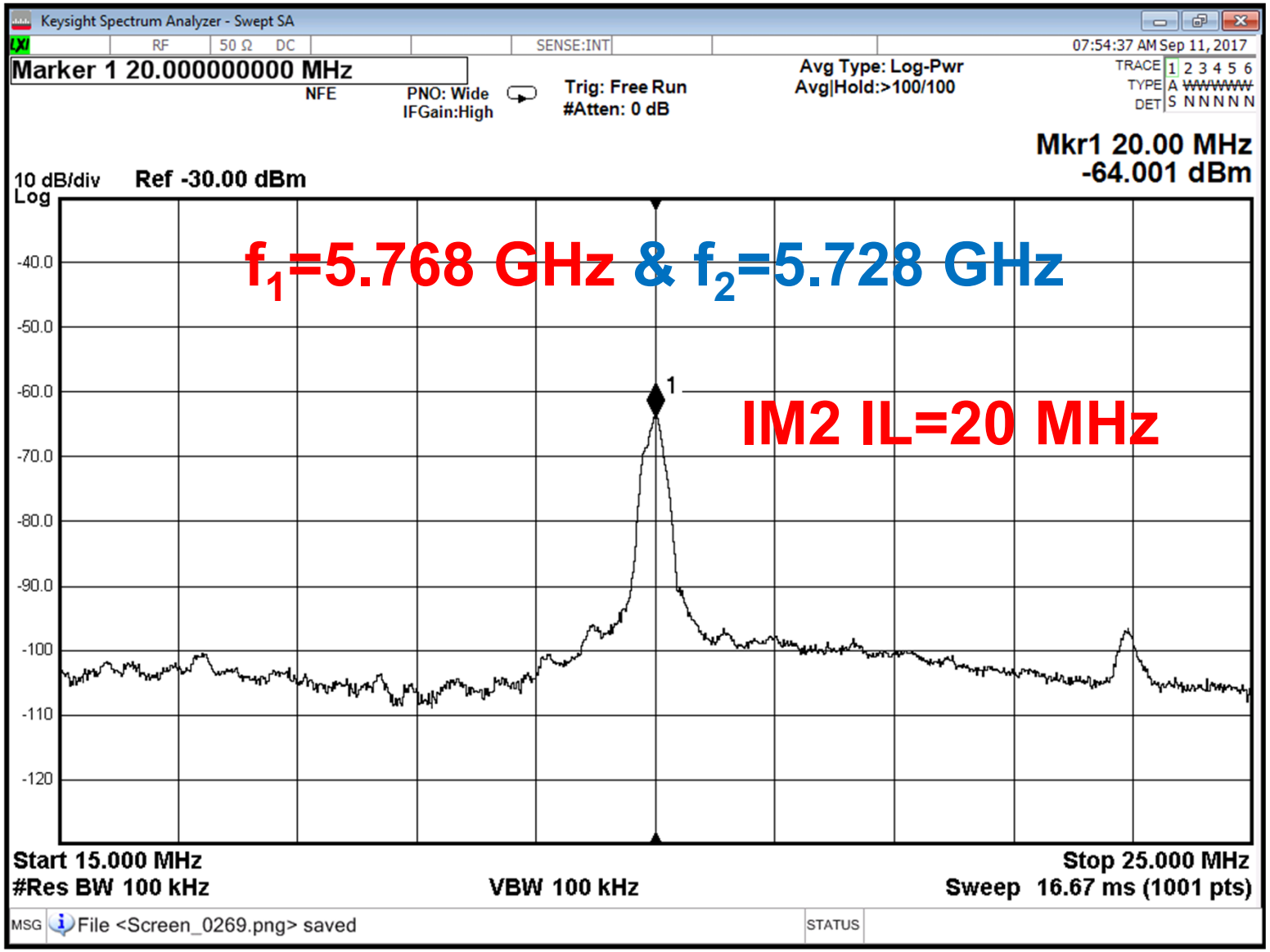


- Power Efficiency@1mm Range: 5.6 x 10^{-6}

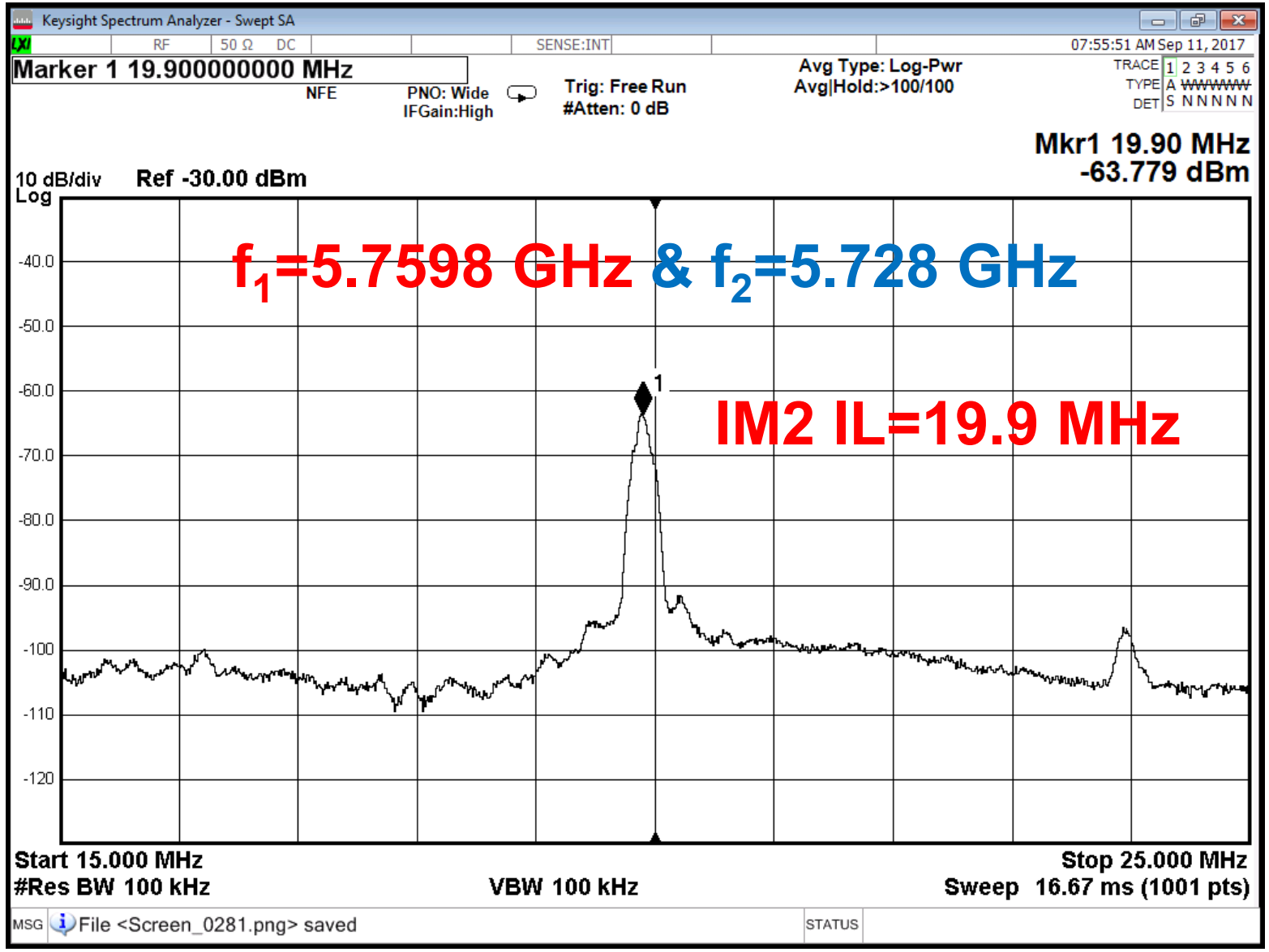
Harvested Power vs. Misalignment



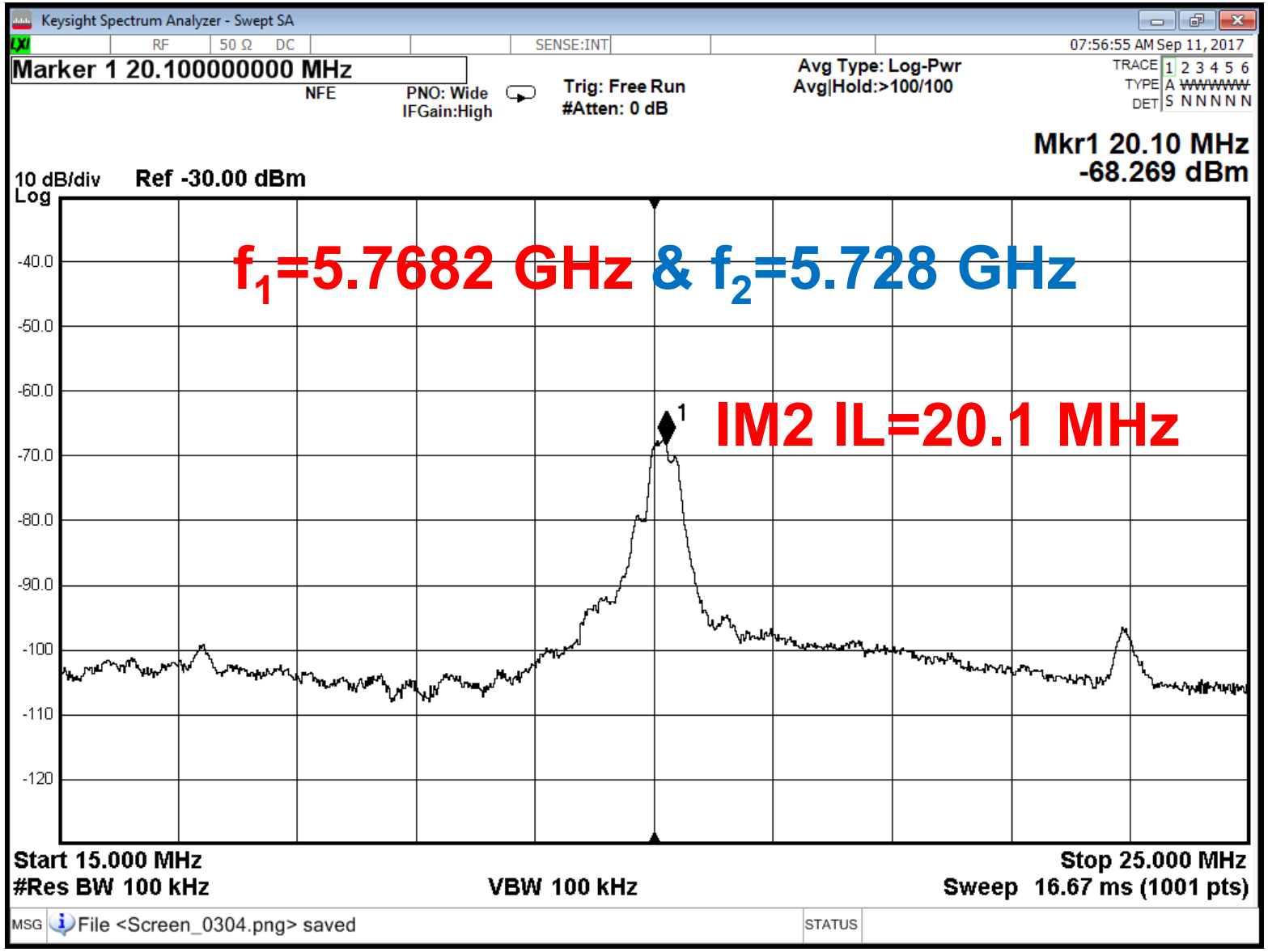
Carrier Oscillator w/ Wireless IM2-IL



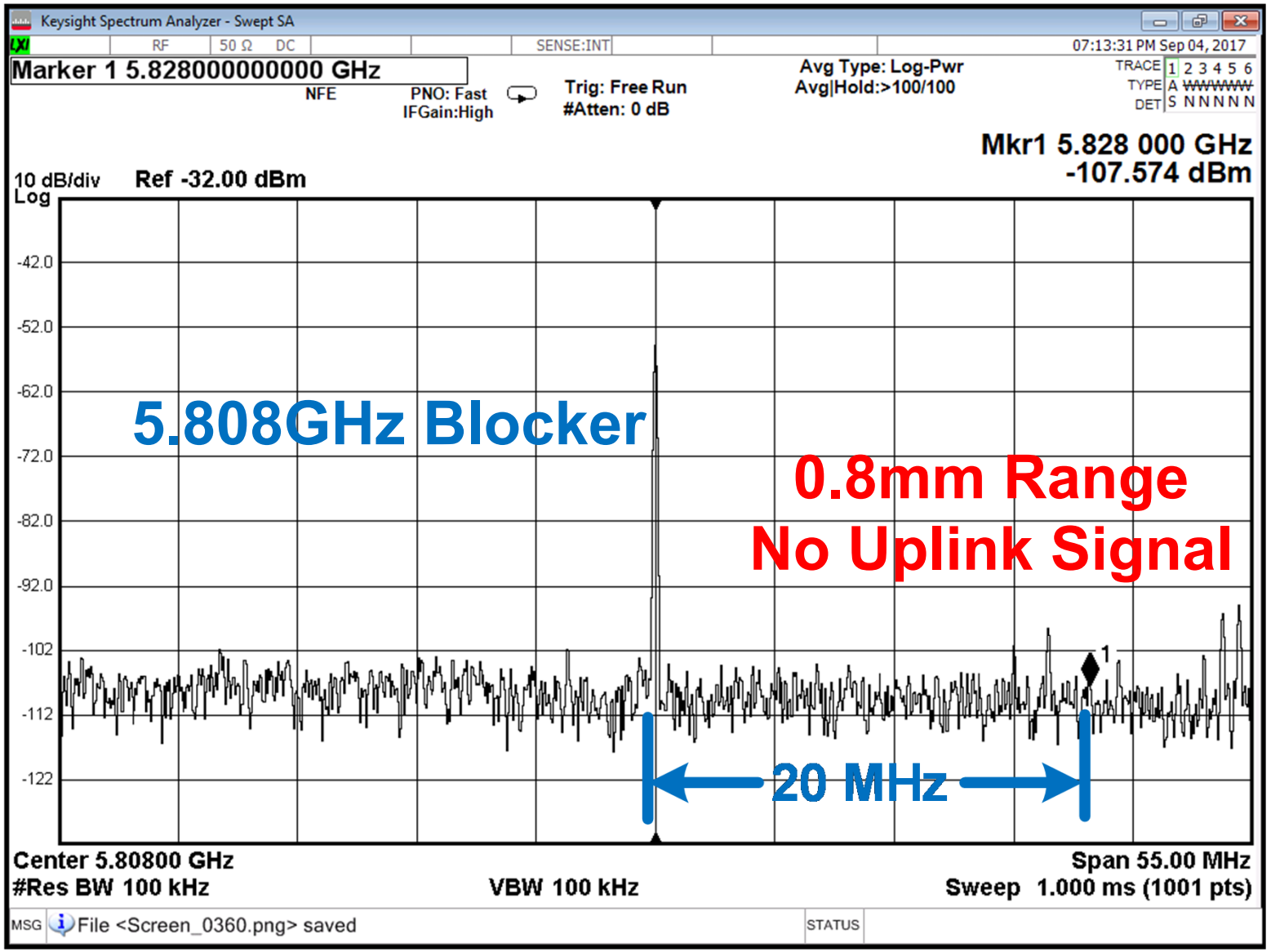
Carrier Oscillator w/ Wireless IM2-IL



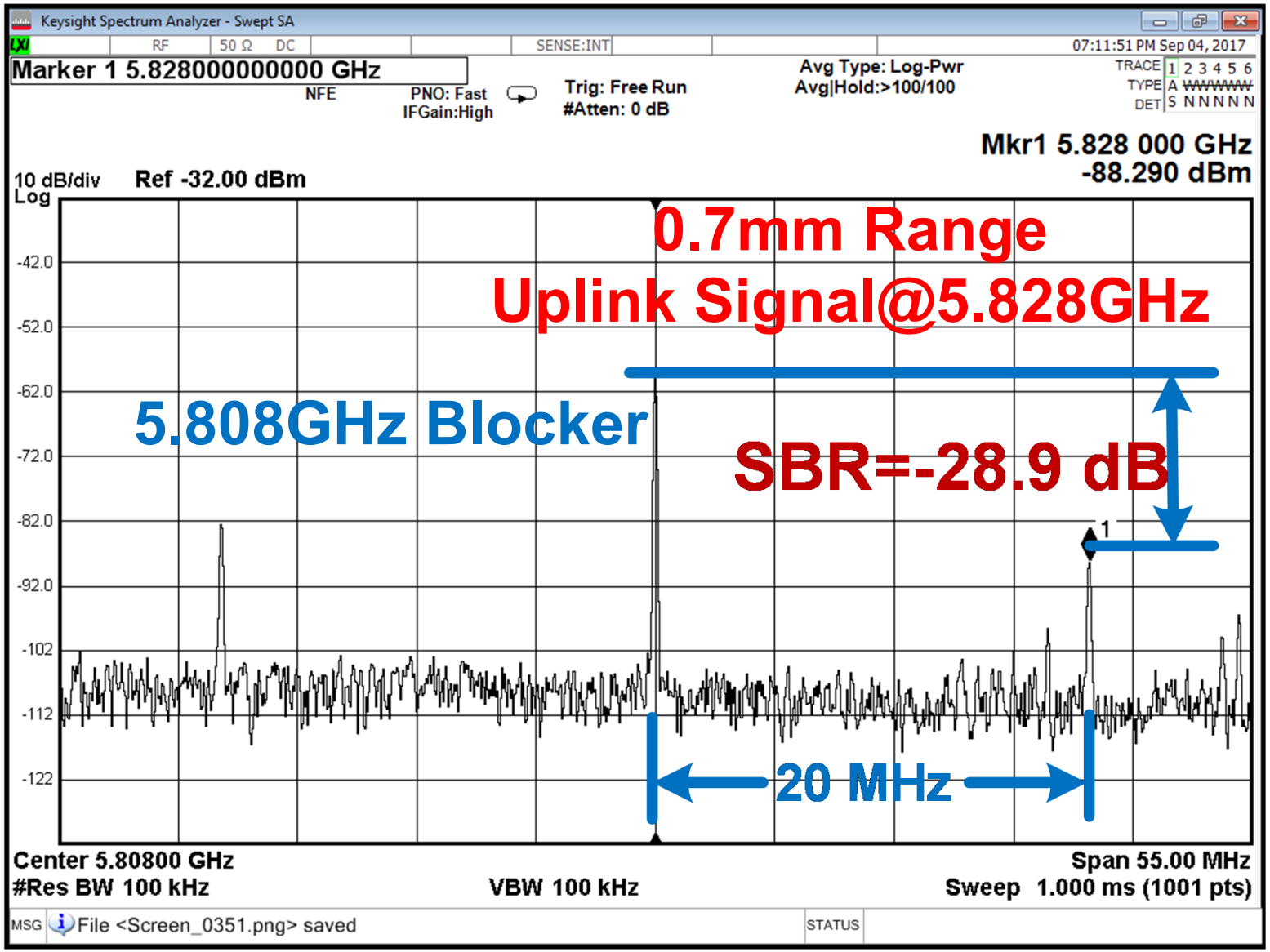
Carrier Oscillator w/ Wireless IM2-IL



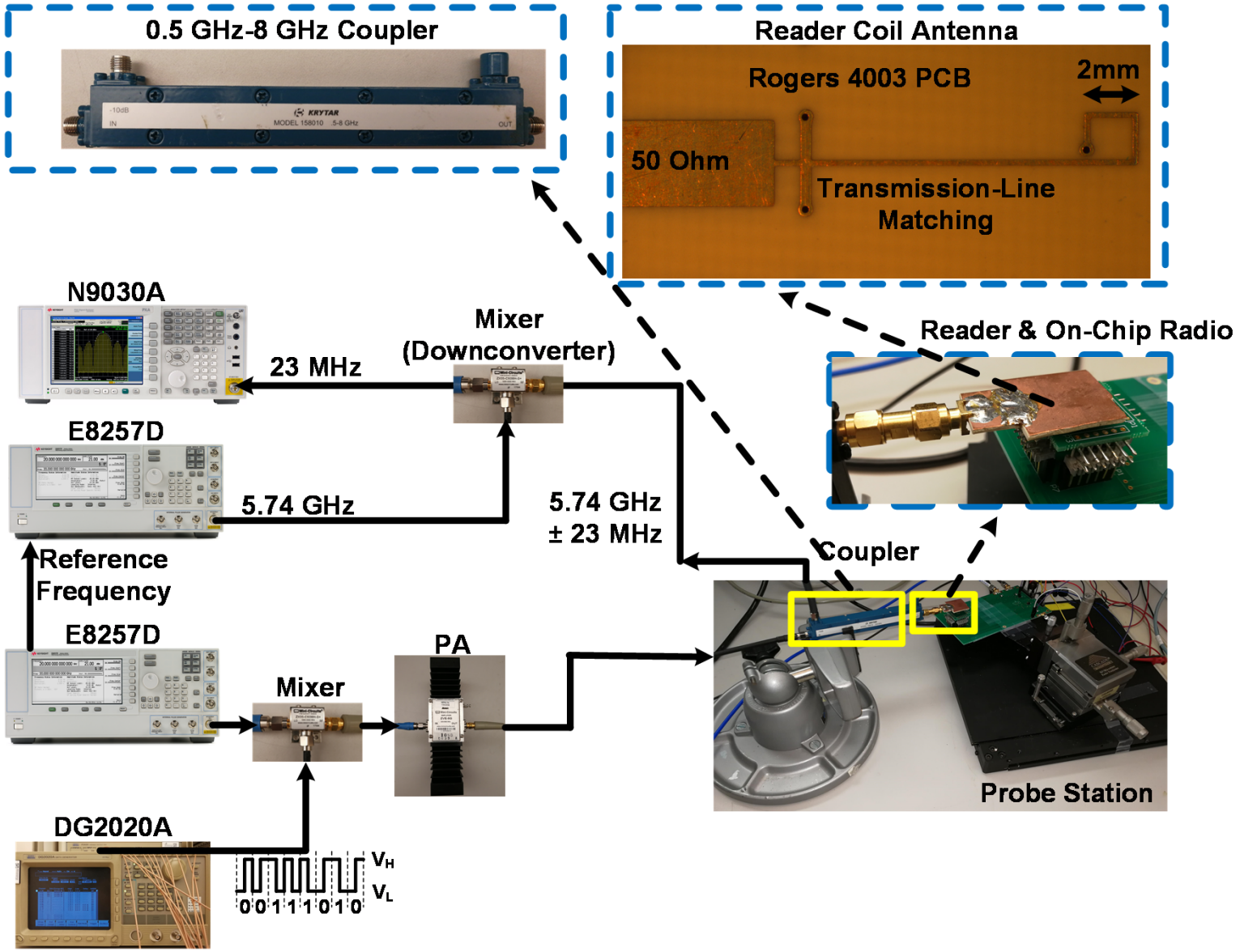
Uplink w/o Wireless IM2-IL



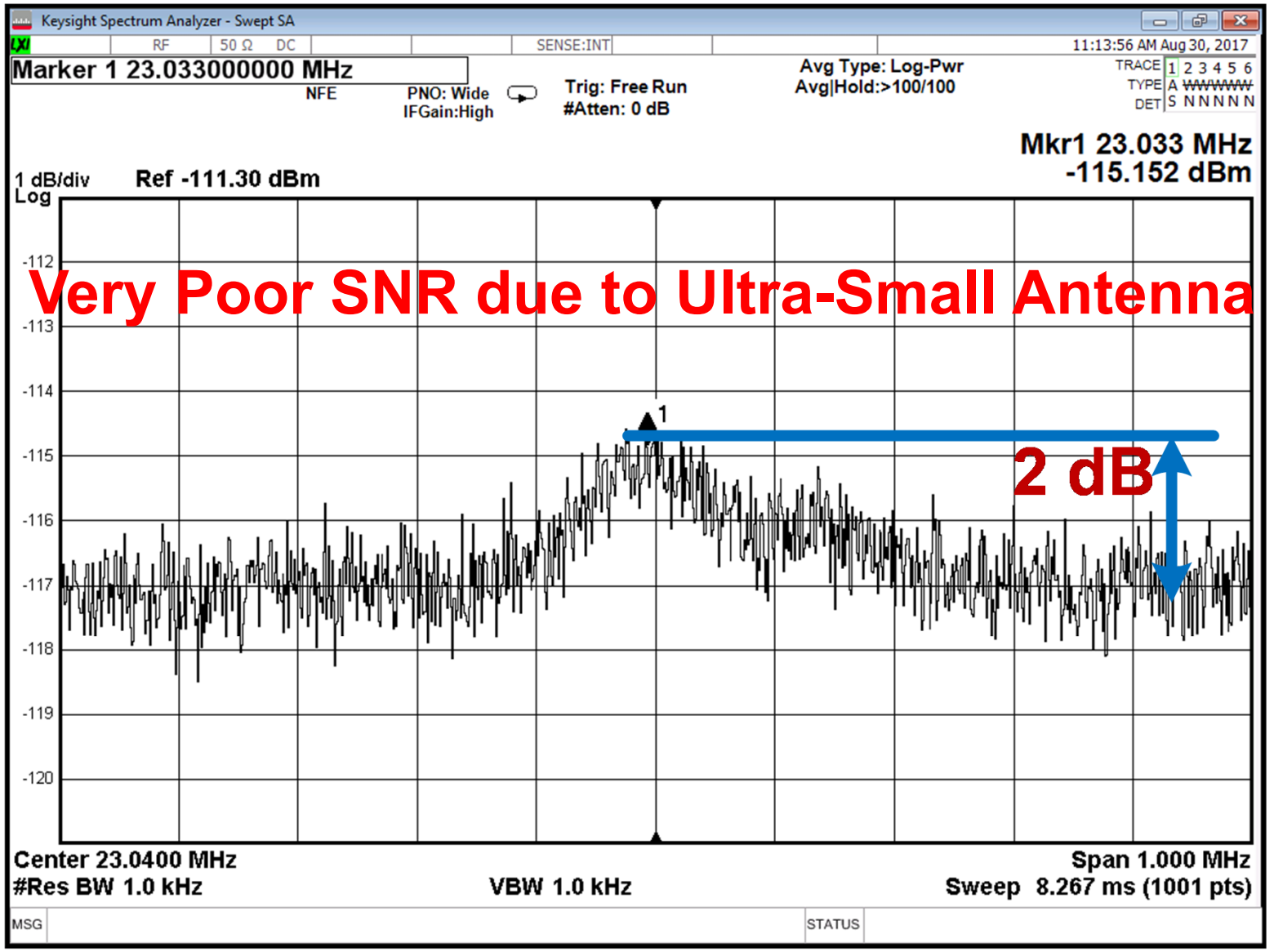
Uplink w/ Wireless IM2-IL



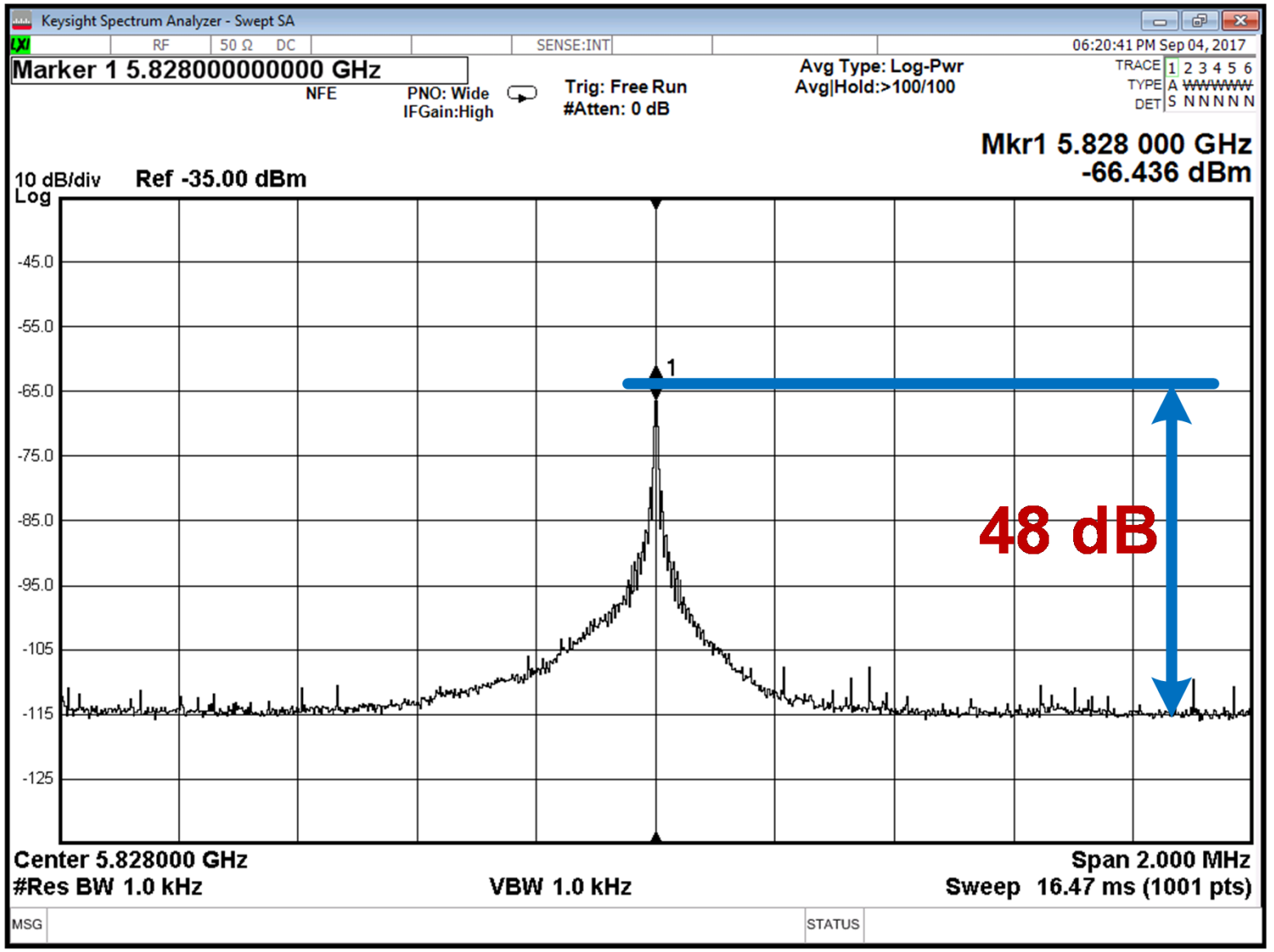
Setup of Backscattering



Uplink by Direct Backscattering



Uplink w/ Proposed 2-Tone Technique



Performance Comparison

Radios	This Work	JSSC'10[8]	RFIC'04[9]	JSSC'13[10]	JSSC'15[11]	ISSCC'17[16]	JSSC'14[17]
CMOS Process	65nm	90nm	180nm	65nm	65nm	180nm	180nm
Frequency (GHz)	5.8 GHz	47 GHz	2.45 GHz	1.5 GHz	DL[(1)]: 24 GHz UL[(1)]: 60 GHz	915 MHz	24 GHz
Near- or Far-Field?	Near-Field	Far-Field	Near-Field	Near-Field	Far-Field	Far-Field	Far-Field
Antenna Type	On-Chip (Inductive)	Off-Chip	On-Chip (Inductive)	On-Chip (Inductive)	On-Chip (Dipole)	Off-Chip (3D Magnetic)	On-Chip (Dipole)
Off-Chip Components	NO	NO	NO	YES	NO	YES	NO
Modulation	DL:<4% ASK UL: 2-Tone	DL: None UL: PWM[(2)]	DL: 100% ASK UL:Backscatter	Miller (100% ASK)	DL: 75% ASK UL: PPM	PPM[(3)] (100% ASK)	100% ASK
Data Rate	DL: 5 Mb/s UL: 4 kb/s	DL: None UL: 5-50 kbps	DL: N/A UL: 12.5 kbps	DL: 1 Mb/s UL: 1 Mb/s	DL: 6.5 Mbps UL: 12 Mbps	DL:7.8-62.5kbps UL: 0.03-30.3kbps	None
Uplink SNR	42 dB (4kbps data)	N/A	N/A	10 dB	N/A	N/A	40 dB (No data)
Uplink SBR	-28.9 dB @20 MHz	N/A	N/A	N/A	N/A	N/A	-50 dB @4 kHz
Overall Size	116x116um^2	1.3x0.95mm^2 (W/O Antenna)	400x400um^2	500x250um^2	3.7x1.2mm^2	2.23x1.2mm^2 (W/O Antenna)	3.74x1.86mm^2

<11% State-of-the-Art

[(1)]DL: Downlink, UL: Uplink [(2)]PWM: Pulse-Width Modulation [(3)]PPM: Pulse-Position Modulation

Outline

- ❑ Design Motivation
- ❑ Proposed Radio System
- ❑ Circuit Details
- ❑ Measurement Results
- ❑ **Summary**
- ❑ Acknowledgements

Summary

- ❑ Dual-Channel Downlink
  - ➢ Low Data Rate
  - ➢ Large Decap

→ Channel-Reuse → x5 Faster, Reduced Area

- ❑ Backscattering
  - ➢ Blocker Issue
- ❑ Dual-Antenna
  - ➢ Large Size
- ❑ No Crystal
  - ➢ Poor SNR

→ Two-Tone → 46 dB SNR Improvement, Reduced Area

- ❑ 500µm x 250µm

→ Channel-Reuse, Two-Tone, Separate LDOs, Optimized Decap, Miniaturized Circuits → 116µm x116µm

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Acknowledgements

- DARPA SHIELD Program (Kerry Bernstein)
- The students, faculty and sponsors of the Berkeley Wireless Research Center (especially Prof. Borivoje Nikolić, Ajith Amerasekera, Angie Wang, and Andrew Townley)
- TSMC University Shuttle Program

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